ECE290 Fall 2012
Lecture 19

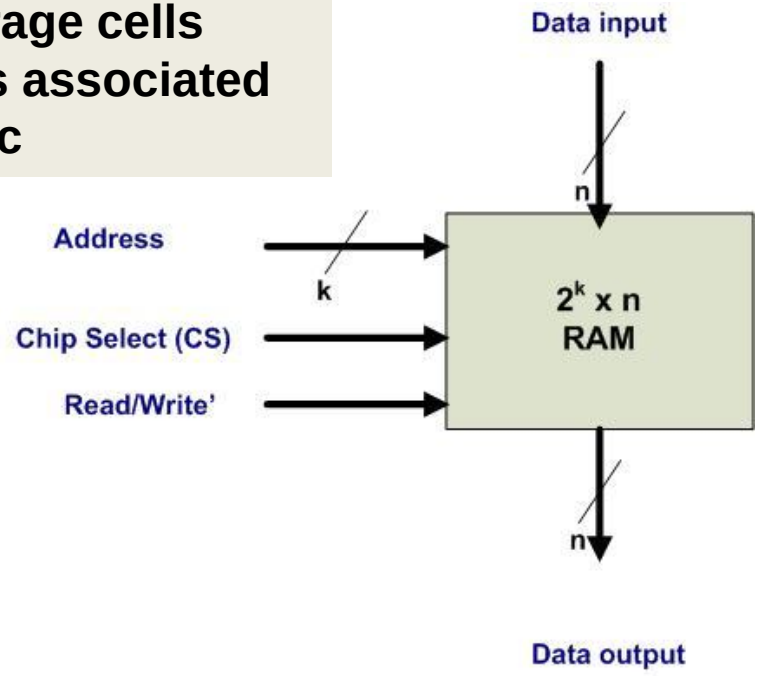
Dr. Zbigniew Kalbarczyk

Today

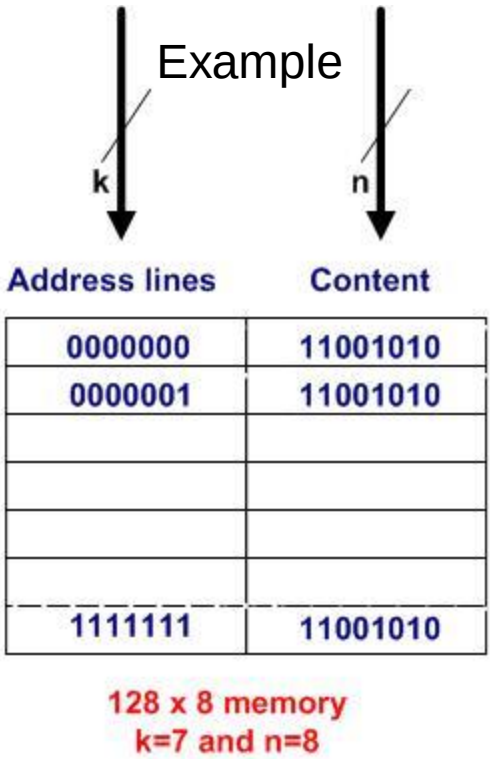
- Random Access Memory
- RAM cell model
- Memory timing
- Memory Addressing

RAM Memory Model

Memory refers to storage cells plus associated logic



CS	R/W'	Operation
0	X	No operation
1	0	write
1	1	read



Memory Capacity:
(a) k=7 & n = 8 => 128B
(b) 1GB => k =30 & n =8 or
k=29 & n =16

RAM Memory Access

- **Memory read** (from memory cells)
  - 1. put address on address lines
  - 2. set CS=1, R/W’ = 1
  - 3. collect data available on data outputs
  - Note: content of selected word is not changed by reading
- **Memory write** (to memory cells)
  - 1. put address on address lines
  - 2. put data on data inputs
  - 3. set CS=1, R/W’ = 0

Memory Timing (1)

- **Memory is un-clocked:**
  - Operation of memory unit are controlled by CPU
  - Memory does not employ CPU clock
  - R/W operations are timed by changes in values on its control inputs
  - Devices interacting with memory are CPU clocked

Memory Timing (2)

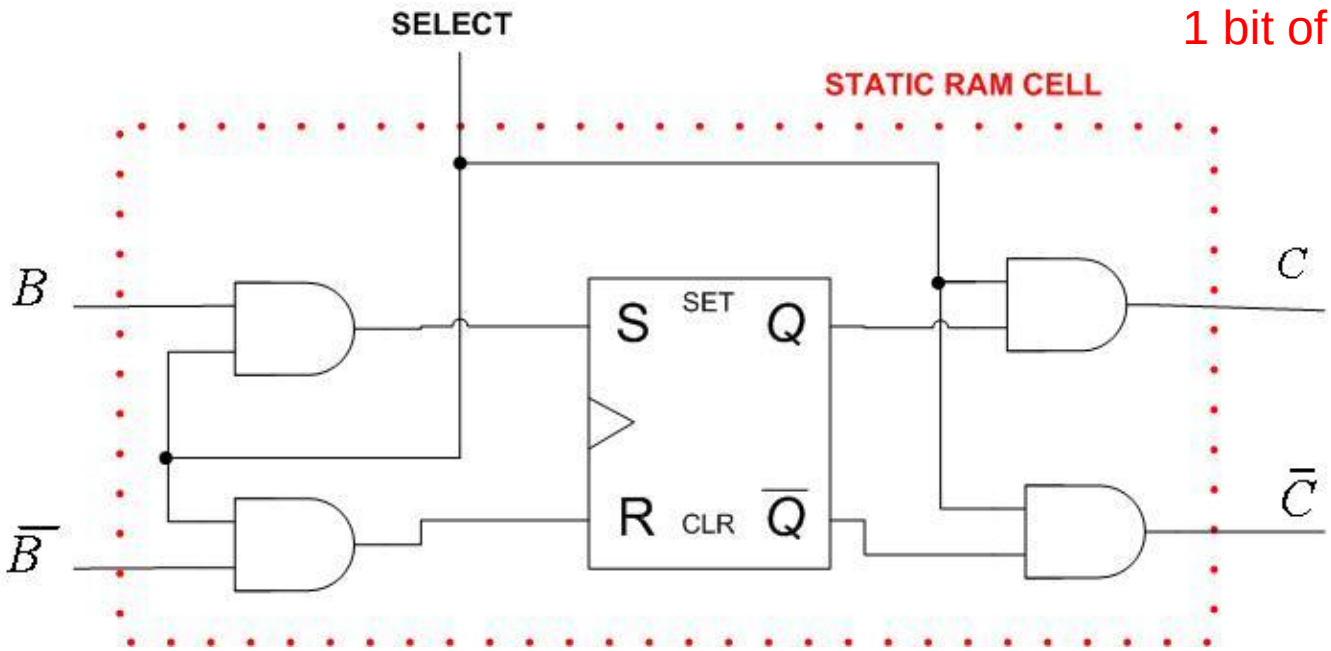
- **Read access time**
  - Max time from the application of the address to the appearance of the data on the data output
- **Write cycle time**
  - Max time from the application of the address to the completion of all internal memory operations to write a word

- **Example:** CPU clock ~ 333MHz ~1/(333*10^6) = 3ns clock period; Read access time=65ns; Write cycle time=75ns
  - Number of CPU clock cycles per memory request?

    Answer: max(75ns,65ns)/clock period = 75/3=25 CPU clock cycles

Static RAM Cell

- Storage Model = SR latch



1 bit of information!

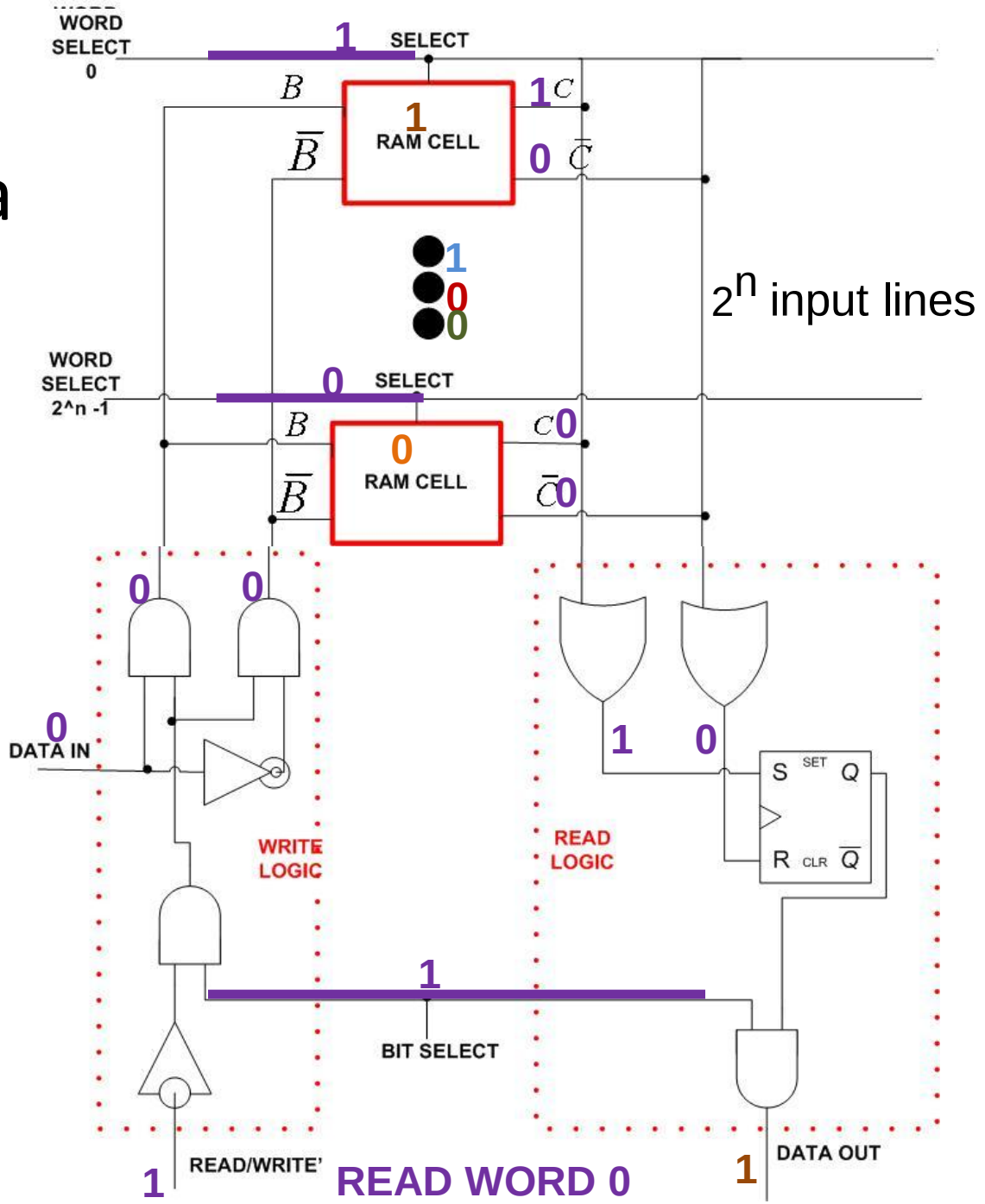
Select	B	B'	C	C'
0	X	X	0	0
1	1	0	1	0
1	0	1	0	1
1	0	0	No change	No change
1	1	1	Undefined	Undefined

From RAM Cell to a RAM Bit Slice

Logic Model of RAM Bit Slice

Needed:

RAM Cells and Read and Write Logic

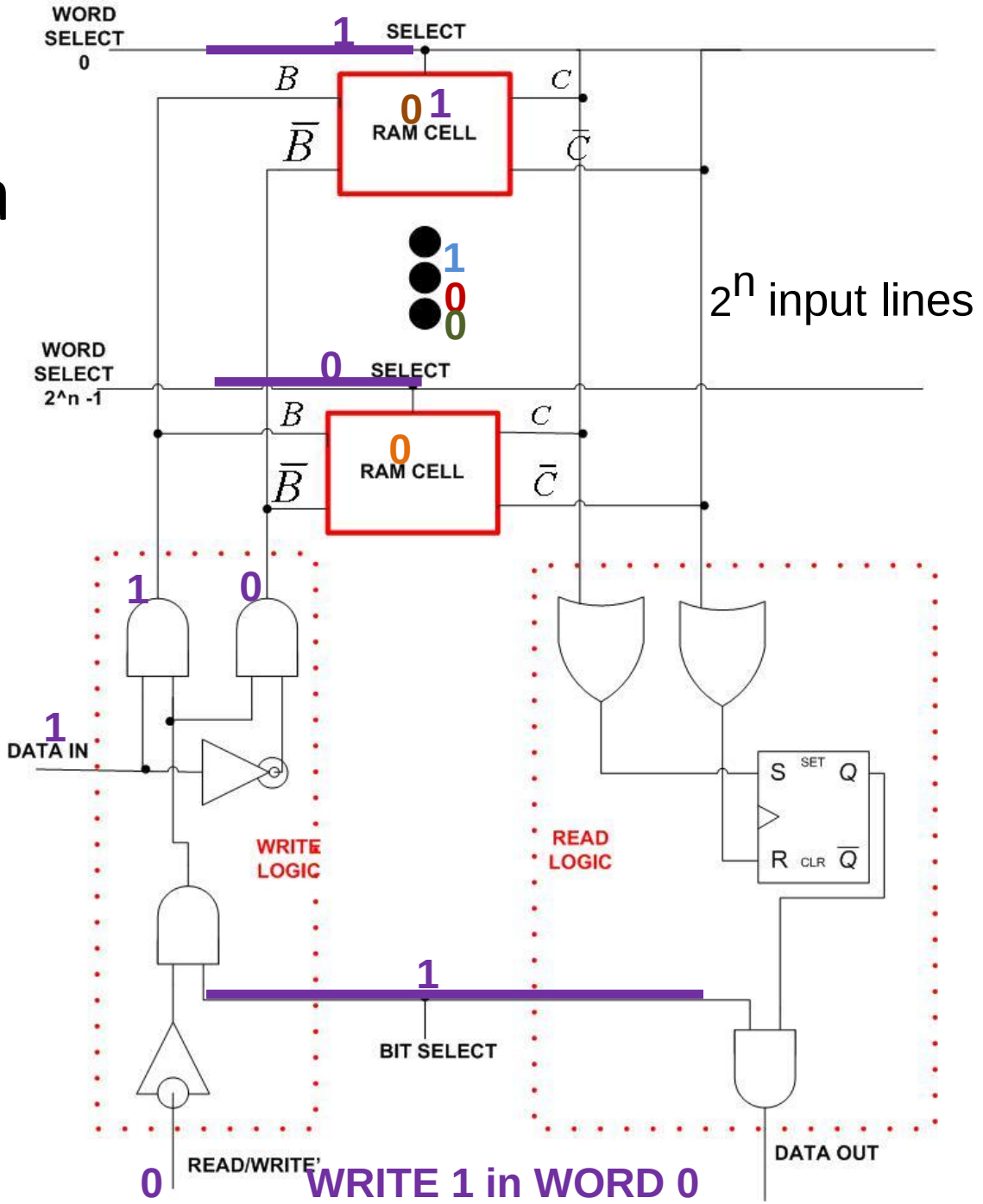


From RAM Cell to a RAM Bit Slice

Logic Model of RAM Bit Slice

RAM Cells and Read and Write Logic

Note : only one WORD SELECT is 1



Read and Write Logic

Word Select i	Read/ Write'	Bit Select	Data In	B	B'	C	C'	Data Out
0	X	X	X	0	0	No change	No change	0
1	0	1	0	0	1	0	1	0
1	0	1	1	1	0	1	0	1
1	0	0	0	0	0	No change	N o change	0
1	0	0	1	0	0	No Change	No Change	0
1	1	1	X	0	0	No Change	No Change	C
1	1	0	X	0	0	No Change	No Change	0

WRITE

READ

Read and Write Operations

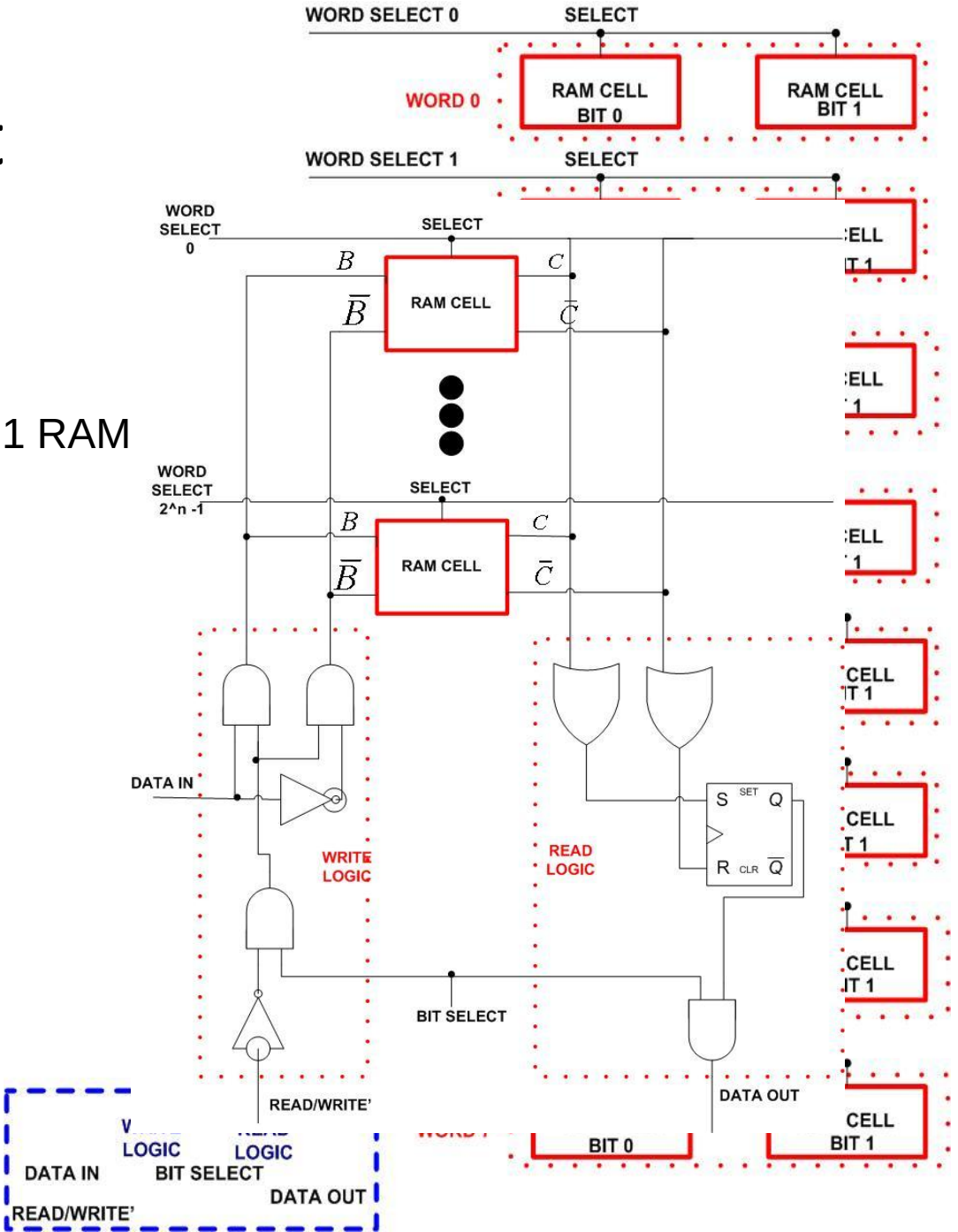
- **Write operation:**
  - Only one word is written at a time
  - Example: n x 1 RAM ~ only one RAM cell (1 bit) is written
- **Read operation:**
  - If Word Select i is 1 then Read takes place
    - Read occurs regardless of Read/Write' value
  - Bit Select has to be 1 for the data to appear on Data Out

Expand Word Lengt

From n x 1 RAM

Example:
Build 8 x 2 RAM

Word Length > 1



Memory Addressing With Cost Considerations

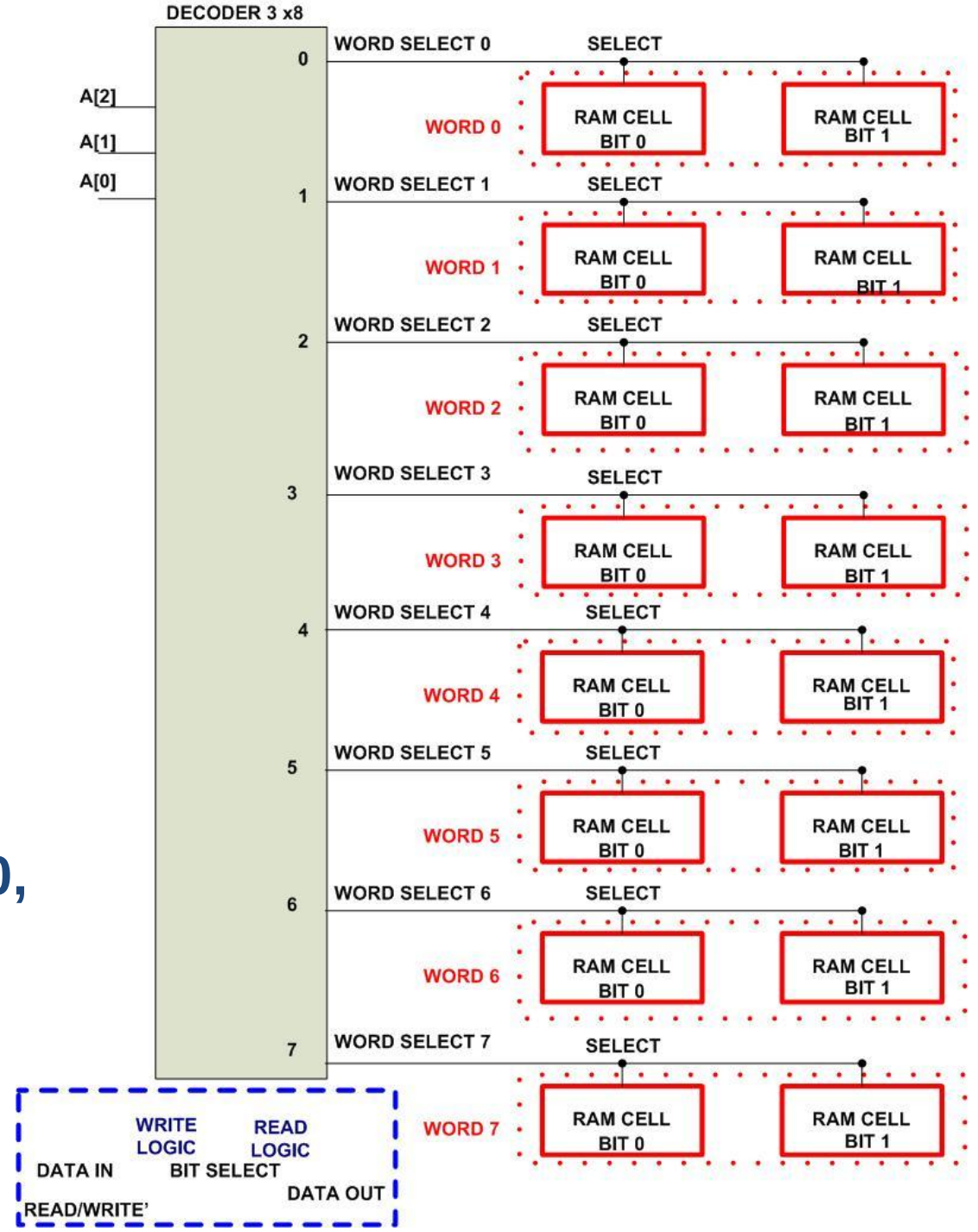
- How to deliver the Address (Word Select bits) with min cost?
  - 1D addressing
  - Coincident (2D) addressing

1D Memory Addressing

Needed: Decoders

Input A: 000, 001, 010, …

Output: Word 0, 1, 2, …



Coincident Addressing

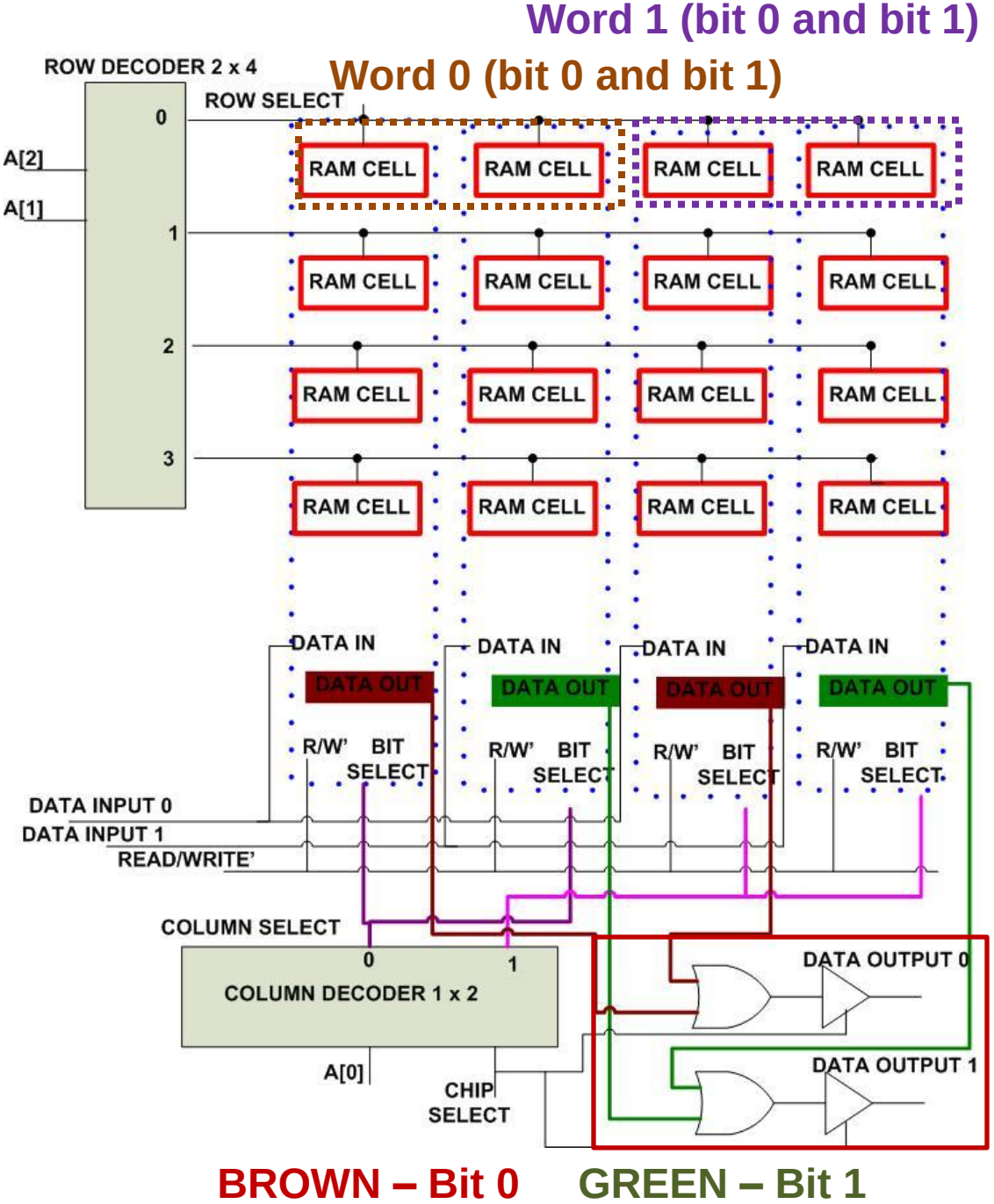
- Design Idea:
  - Number of decoder gates (k inputs requires 2^k AND gates with k inputs) can be reduced by employing two decoders with a coincident selection scheme
- Use row decoder & column decoder
- Decoder outputs control multiple bit-slices
- Fewer gates are required for decoding
- Can extend to more then 2 dimensions

Coincident Addressing

Example:
Build 8 x 2 RAM using 4 x 4 RAM Cell Array

Cost Analysis:
1D addressing: 8 AND gates
2D addressing: 6 AND gates

64K x 2 RAM:
2^16 versus 2^9 AND gates



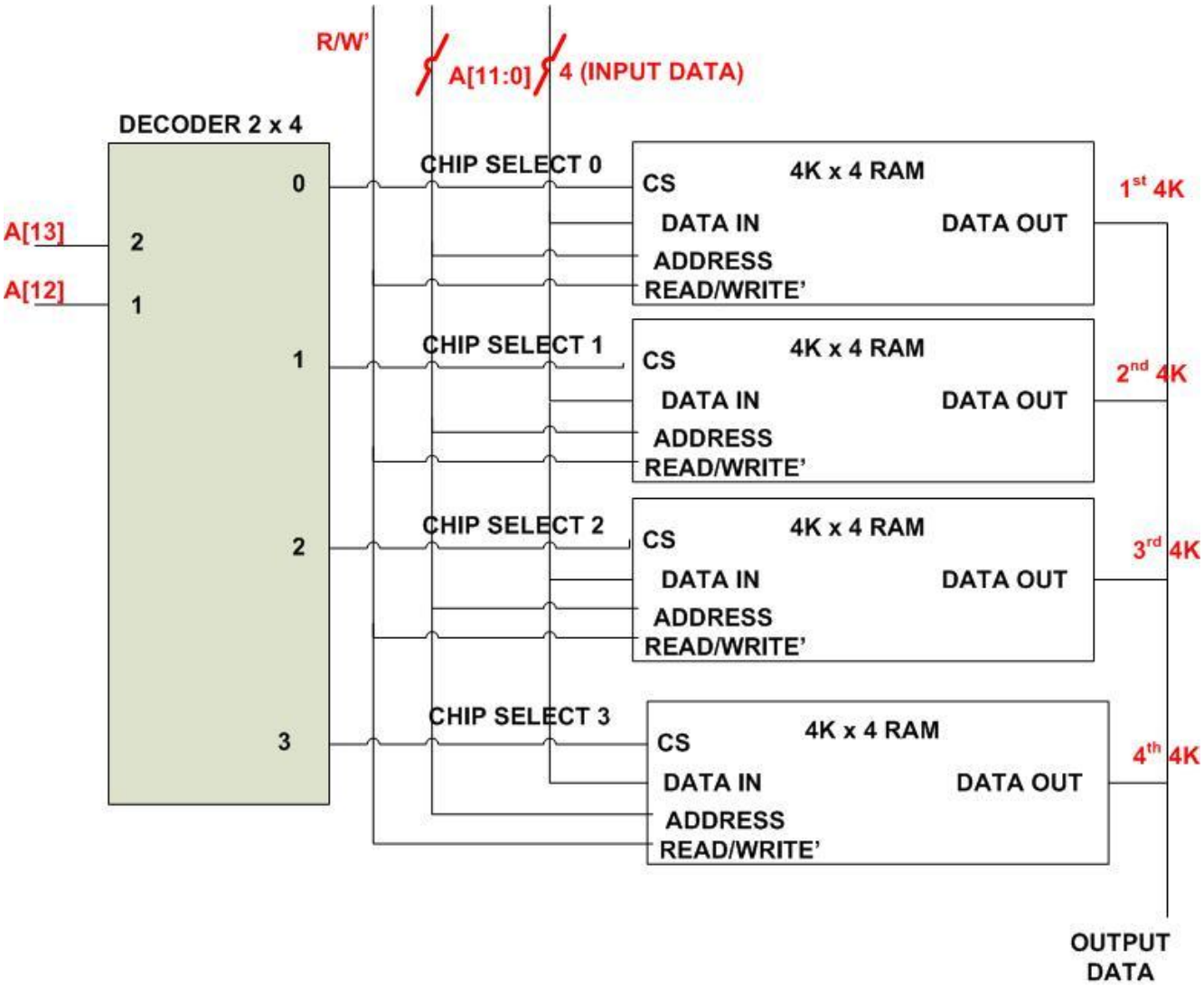
Expanding RAM Memory Bit Slice

- What if available RAM memory chips have a pre-defined number of words and word length (n x m RAM)?
  - Driven by availability of RAM modules
  - Given modules that have n ~number of words, m ~ length of one word
  - **Expand n and m!**

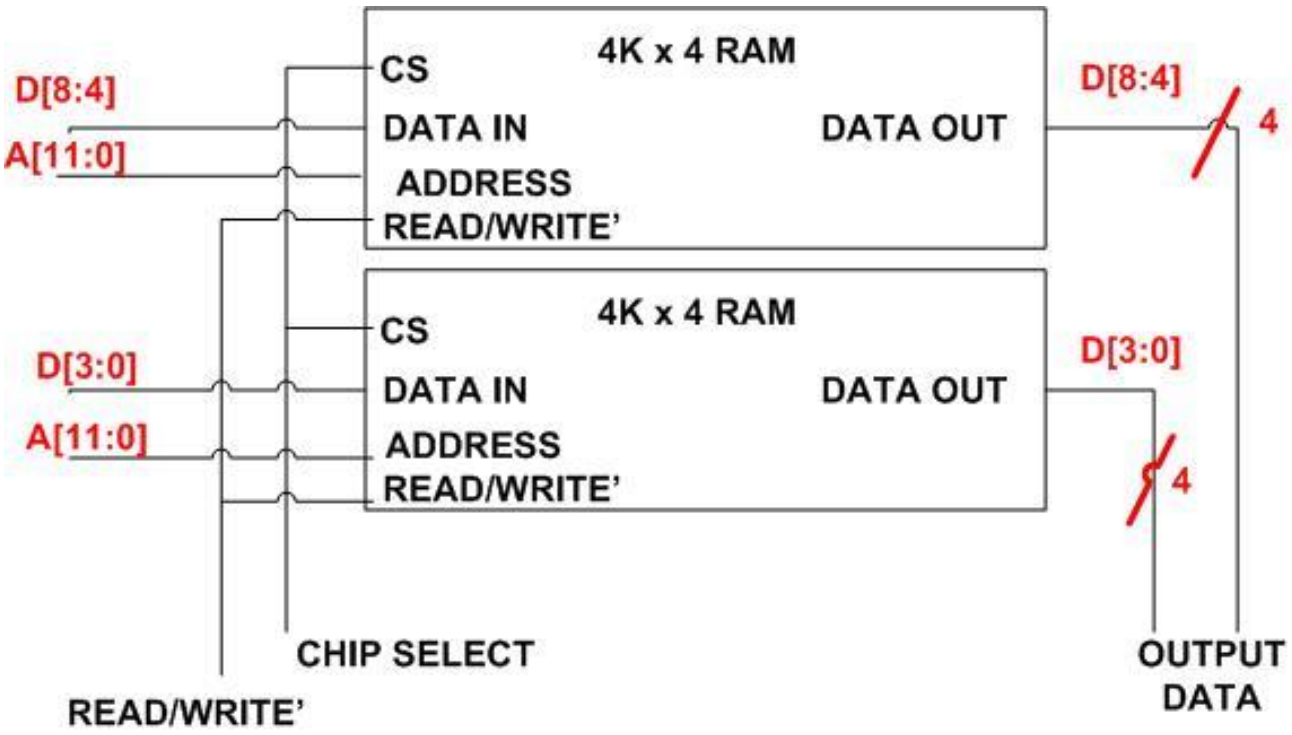
Expand Memory: Number of Words

Example:
Given 4K x 4 RAM chips build 16K x 4 RAM

Needed: 14 bit address and Decoder 2 x 4 for chip select



Expand Memory: Word Length



Example:
Given 4K x 4 RAM chips build 4K x 8 RAM

Needed: Data Split (Data In) and Data Aggregation (Data Out)

Problem 1: Compute Memory Capacity

- Given
  - Number of address bits k = 10
  - Number of data bits n = 16
- Task: Compute the total memory capacity in bytes

Solution: 2^10 * (16/8) Bytes = 2KB

Problem 2: Compute CPU Cycles Per Memory Request

- Given:
  - CPU clock ~ 333MHz ~1/(333*10^6) = 3ns clock period;
  - Read access time=65ns;
  - Write cycle time=75ns
- Task: Compute the number of CPU clock cycles per memory request?

Solution: max(75ns,65ns)/clock period = 75/3=25 CPU clock cycles