Lecture Notes for ECE 422 / EE 522

Fall 2012

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Acknowledgments

These course notes were originally developed by me for EE476 in Fall 1996 at Washington State University (WSU). The material in these notes has been derived from several sources. These include Dr. Venu Gopinathan's course notes from Columbia University, Dr. David Rich's analog IC design course notes, Prof. Terri Fiez's EE476 course notes, and Prof. Paul Gray's EE240 lecture notes. Their contributions to these notes are gratefully acknowledged. Also a significant amount of the material is based on the Gray and Meyer textbook. Prof. George La Rue at WSU made a monumental effort in cleaning up and formatting the original hand written notes in MS-WORD. I thank him for this effort and for providing me with the formatted notes. This version of the course notes is directly from him and includes his additions and my recent modifications.

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IC Technologies

CMOS

Si Bipolar

BiCMOS

GaAs (E/D MESFET & HFET)

InP Heterojunction Bipolar

SiGe Bipolar and BiCMOS

Applications

Telecommunications
- Optical
- Wireless
- DSL

Computing Applications
- A/Ds and D/As
- Audio including voice
- Displays
- Disk drives and CDROMs

Sensors and Actuators

Automotive
- Engine control
- Displays
- Anticollision systems
- Airbags

Biomedical
- Pacemakers
- Hearing aids

Analog Circuit Hierarchy

Device Technology
- CMOS, bipolar, GaAs MESFET, HBT

Basic Circuits
- Amplifiers
- Current mirrors
- Buffers

Functional blocks
- Operational Amplifiers
- A/D converters, D/A converters
- Voltage controlled oscillators
- Mixers
- Comparators
- Phase lock loops
- Voltage references
- Filters

Subsystems
- Modulators and Demodulators
- Optical and wireless transceivers
- DSL and LAN modems

Systems
- Cellular phones
- Disk and CD ROM drives
- Modems
- Measurement instruments
- Automobile air bag

Advantages of single-chip implementation

1) Reduced system size – cell phones, hearing aids.
2) Increased speed – no parasitic capacitances from pins and interconnect
3) Reduced power dissipation – fewer off chip drivers required
4) Increased reliability – fewer packages, fewer interconnects and fewer bond wires (connections are most unreliable)
5) Reduced cost – smaller and simpler printed circuit boards, fewer packages (It costs about $10,000 per kg to launch a satellite)

Disadvantages

Integrating digital and analog components on same chip may increase design time and number of iterations due to noise coupling

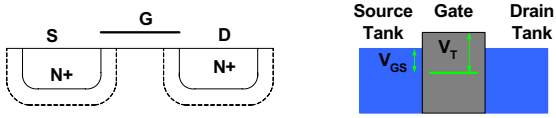
Other technologies may offer improved performance

For instance, InP low noise amplifiers have lower noise figure than other technologies and may set the performance level for the whole system.

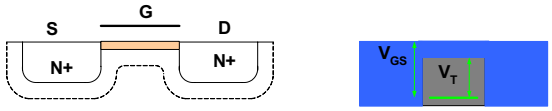
MOSFET Operation Simplified (Fluid Dynamics Analog)

V_T = turn-on Voltage (threshold voltage)

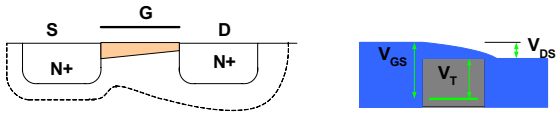
1) Cut off: $V_{GS} < V_T$, $V_{DS} = 0$



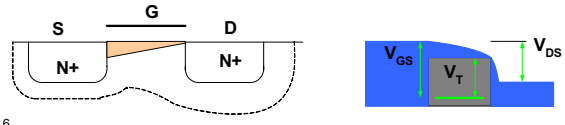
2) Strong Inversion: $V_{GS} > V_T$, $V_{DS} = 0$



3) Non-saturation: $V_{GS} > V_T$, $0 < V_{DS} < V_G - V_T$

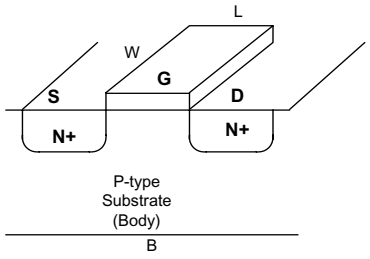


4) Saturation: $V_{GS} > V_T$, $0 < V_{DS} > V_G - V_T$
Flow becomes independent of V_{DS}

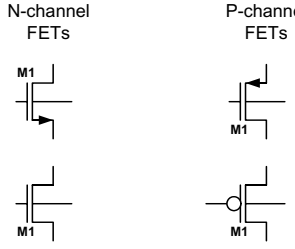


The MOSFET

Enhancement mode n-channel transistor (NMOSFET)



MOSFET Symbols



If bulk is connected to proper power supply:

Basic MOSFET Equations

N-channel MOSFET Equations (simple model)

$I_{DS} = 0$ $\quad V_{GS} \le V_T$ **Cut Off**

$I_{DS} = K'\frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1+\lambda V_{DS})$ $\quad V_{GS} > V_T,\ V_{DS} \le V_{GS} - V_T$ **Triode**

$I_{DS} = \frac{1}{2}K'\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$ $\quad V_{GS} > V_T,\ V_{DS} > V_{GS} - V_T$ **Saturation**

$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$ $\quad \Phi = 2\Phi_F$

$K' = \mu C_{ox}$ $\quad C_{ox} = 3.45\,fF/\mu^2$ for t = 10 nm

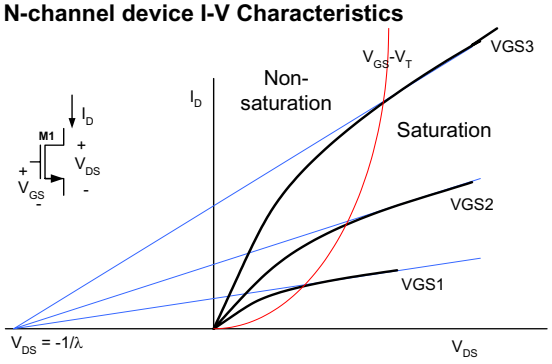
K', V_{T0}, γ, Φ, λ are process parameters
W and L are device geometry parameters

The simplest model in SPICE (Level 1 or default model) uses the above equations.

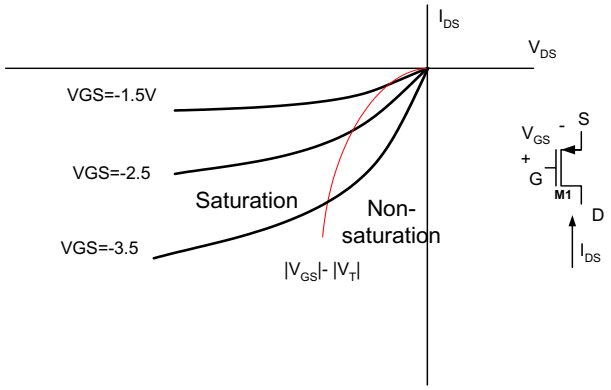
Parameter	SPICE Parameter	Units
K'	KP	A/V^2
V_{T0}	VTO	V
γ	GAMMA	$V^{0.5}$
λ	LAMBDA	V^{-1}
Φ	PHI	V

Typical values	
λ	0.05 – 0.005 V^{-1}
VTO	0.5 – 1.0 V
K'	200uA/V^2 (t_{ox} = 0.01u)
γ	.2 – 1.0 $V^{0.5}$

N-channel device I-V Characteristics



P-channel device I-V Characteristics



P-channel MOSFET Equations (simple model)

1) Multiply all voltages by –1
2) Compute current as for n-channel
3) Multiply current by –1

OR

$I_{SD} = 0$ $\quad V_{SG} \le |V_T|$ **Cut Off**

$I_{SD} = K_P' \frac{W}{L}\left[(V_{SG} - |V_T|)V_{SD} - \frac{V_{SD}^2}{2}\right](1 + \lambda V_{SD})$ $\quad V_{SG} > |V_T|,\ V_{SD} \le V_{SG} - |V_T|$ **Triode**

$I_{SD} = \frac{1}{2} K_P' \frac{W}{L}(V_{SG} - |V_T|)^2(1 + \lambda V_{SD})$ $\quad V_{SG} > |V_T|,\ V_{SD} > V_{SG} - |V_T|$ **Saturation**

$V_T = V_{T0} - \gamma\left(\sqrt{\Phi + V_{BS}} - \sqrt{\Phi}\right)$ $\quad K_P' = \mu_p C_{ox}$

Example

V_S = 4V, V_G = 2V, V_D = 1V
V_T = 0.8, λ = 0, Kp' = 100 μA/V^2
W = 10μ, L = 2μ

$|V_{DS}| > |V_{GS}| - |V_T|$ ⇒ in saturation

$$I_{SD} = \frac{1}{2} K_P' \frac{W}{L}(V_{SG} - |V_T|)^2(1 + \lambda V_{SD})$$

$$I_{SD} = \frac{100\mu}{2}\frac{10\mu}{2\mu}(2 - |-0.8|)^2(1 + 0) = 250u(1.44) = 360\mu A$$

I_{DS} = -360 μA

Body effect parameter (γ)

N-channel device

$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

Example

V_{T0} = 0.5 V, γ = 0.3 V$^{0.5}$, V_{SB} = 3 V, Φ = 0.6 V

$$V_T = 0.5 + 0.3\left(\sqrt{3 + 0.6} - \sqrt{0.6}\right)$$
$$V_T = 0.5 + 0.34 = 0.84V$$

P-channel device

$$V_T = V_{T0} - \gamma\left(\sqrt{\Phi + V_{BS}} - \sqrt{\Phi}\right)$$

Example

V_{T0} = -0.7 V, γ = 0.6 V$^{0.5}$, V_{BS} = 2 V, Φ = 0.7 V

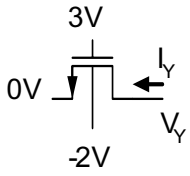
$$|V_T| = 0.7 + 0.6\left(\sqrt{2 + 0.7} - \sqrt{0.7}\right)$$
$$V_T = -(0.7 + 0.48) = -1.18V$$

The source and drain terminals are interchangeable

In our equations $V_{DS} \ge 0$. Interchange terminals if $V_{DS} < 0$.

Example

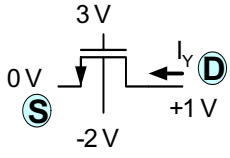
V_{T0} = 1 V, λ = 0, K' = 60 μA/V^2
γ = 0.5 V$^{0.5}$, Φ = 0.8 V
W = 1μ, L = 1μ



1) Calculate I_Y for V_Y = 1 V

Since V_Y = 1 V > 0 V, the drain is on the right

V_{GS} = 3 V, V_{DS} = 1 V, V_{SB} = 2 V



$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

$$V_T = 1.0 + 0.5\left(\sqrt{2 + 0.8} - \sqrt{0.8}\right)$$
$$V_T = 1.0 + 0.39 = 1.39V$$

$V_{GS} - V_T$ = 3 – 1.39 = 1.61 V

$V_{DS} < V_{GS} - V_T$ ⇒ non-saturation region

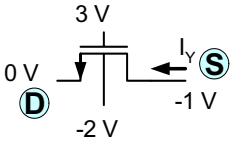
$$I_{DS} = K'\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$$

$$I_{DS} = 60\mu\frac{1}{1}\left[(1.61)1 - \frac{1^2}{2}\right](1 + 0 \times 1) = 66.6\mu A = I_Y$$

2) Calculate I_Y for V_Y = -1 V

Since V_Y = -1 V < 0 V, the drain is now on the left

V_{GS} = 4 V, V_{DS} = 1 V, V_{SB} = 1 V



$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

$$V_T = 1.0 + 0.5\left(\sqrt{1+0.8} - \sqrt{0.8}\right)$$

$$V_T = 1.0 + 0.2 = 1.2V$$

V_{GS} - V_T = 4 – 1.2 = 2.8 V > V_{DS} $\Rightarrow$ non-saturation region

$$I_{DS} = 60\mu\frac{1}{1}\left[(2.8)1 - \frac{1^2}{2}\right](1+0\times1) = 138\mu A = -I_Y$$

I_Y = - 138μA

Calculation of V_{GS} for a given drain current

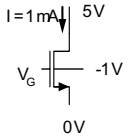
Transistor in saturation

$$I_{DS} \cong \frac{1}{2}K'\frac{W}{L}(V_{GS} - V_T)^2$$ assuming λ small

$$V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}} \quad \text{or} \quad V_{GS} \cong V_T + \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}}$$

Example

V_{T0} = 0.8 V, λ = 0, K' = 77 μA/V^2
γ = 0.35 V$^{0.5}$, Φ = 0.8 V
W = 10μ, L = 2μ



a) V_D = 5V

$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

$$V_T = 0.8 + 0.35\left(\sqrt{1+0.8} - \sqrt{0.8}\right) = 0.96V$$

Assume transistor in saturation

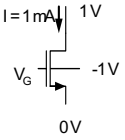
$$V_{GS} \cong V_T + \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}}$$

$$V_{GS} \cong 0.96 + \sqrt{\frac{2x10^{-3}}{77\times10^{-6}\frac{10}{2}}} = 0.96 + 2.28V = 3.24V$$

Check assumption: V_{GS} - V_T = 2.28 V < V_{DS} = 5V $\Rightarrow$ saturation region ✓

b) With V_D = 1V, the saturation assumption is invalid

For non-saturation



$$I_{DS} \cong K'\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$V_{GS} \cong V_T + \frac{I_{DS}}{K'\frac{W}{L}V_{DS}} + \frac{V_{DS}}{2}$$

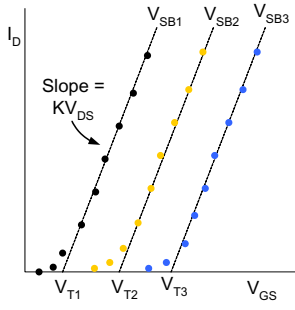
$$V_{GS} \cong 0.96 + \frac{10^{-3}}{77\times10^{-6}\frac{10}{2}\times1} + \frac{1}{2} = 4.06V$$

Check assumption: V_{GS} - V_T = 4.06 – 0.96 = 3.1 V > V_{DS} = 1V $\Rightarrow$ non-saturation region ✓

Parameter Extraction

Determination of K and V_T (K = K'W/L)

At very small V_{DS}, $I_{DS} \cong K(V_{GS} - V_T)V_{DS}$
Slope = KV_{DS}, extrapolated intercept is V_T



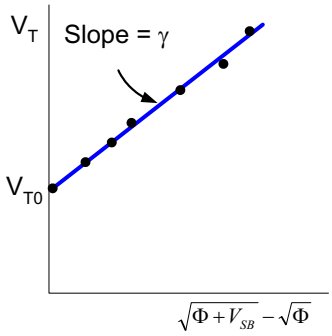
If W/L is known then K' = K/(W/L)
If slope is not the same for all curves, use an average value

Determination of γ and V_{T0}

From previous measurement, V_T is known as a function of V_{SB}

$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

Plot V_T versus $\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}$ assuming Φ = 0.6 V



Slope = γ, intercept = V_{T0}.

Calculation of λ

$$I_{DS} = \frac{1}{2}K'\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

For a fixed V_{GS} and V_{SB}: $I_{DS} = I_0(1 + \lambda V_{DS})$

where $I_0 = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2$

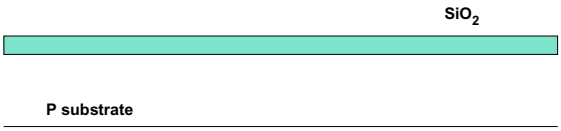
$$\frac{I_{D1}}{I_{D2}} = \frac{(1+\lambda V_{DS1})}{(1+\lambda V_{DS2})}$$

Solve for λ: $$\lambda = \frac{I_{D2} - I_{D1}}{V_{DS2} I_{D1} - V_{DS1} I_{D2}}$$

CMOS Integrated Circuit Technology

Starting Material

Start with a single-crystal Silicon wafer – up to 12" diameter (300 mm)



Grow oxide layer

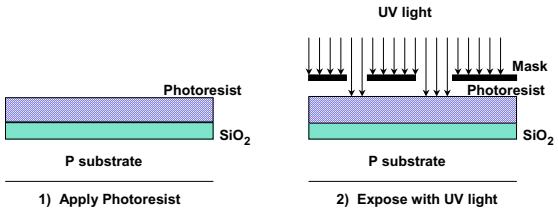
$Si + O_2 \rightarrow SiO_2$

Temperature raised between 850°C to 1100°C

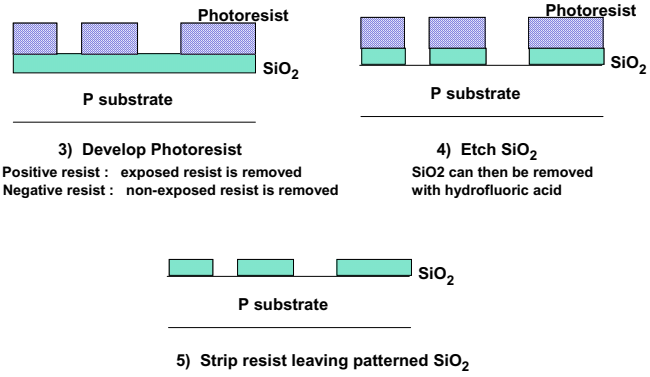
Consumes Si at rate of 0.44 times SiO_2 thickness

A unique property of Si is that the SiO_2 oxide layer thickness can be controlled very uniformly

Photolithography



Creating N and P-Type Regions



Diffusion

Deposit a layer of material on surface

Boron for P-type and Arsenic or Phosphorus for N-type

Raise temperature to ~ 1000° C to allow impurities to diffuse into substrate and replace Si atoms

Highest impurity concentration at surface

Ion Implantation

Atoms are inserted at high energy into substrate

Must be annealed at ~800° C to activate and reduce damage to substrate

Most common method because

- Very uniform across wafer
- Peak of impurity profile can be below surface

Deposition and Etching

Deposition

Various materials need to be deposited on the wafers to fabricate circuits

Chemical vapor deposition (CVD) is a common method to apply polysilicon, silicon nitride (Si_3N_4) and other dielectrics

Metals are typically evaporated onto the wafers

Etching

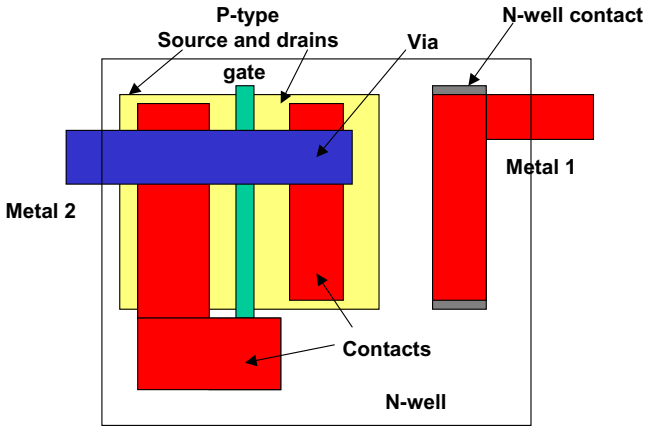
Used to remove materials with high precision

Wet etching

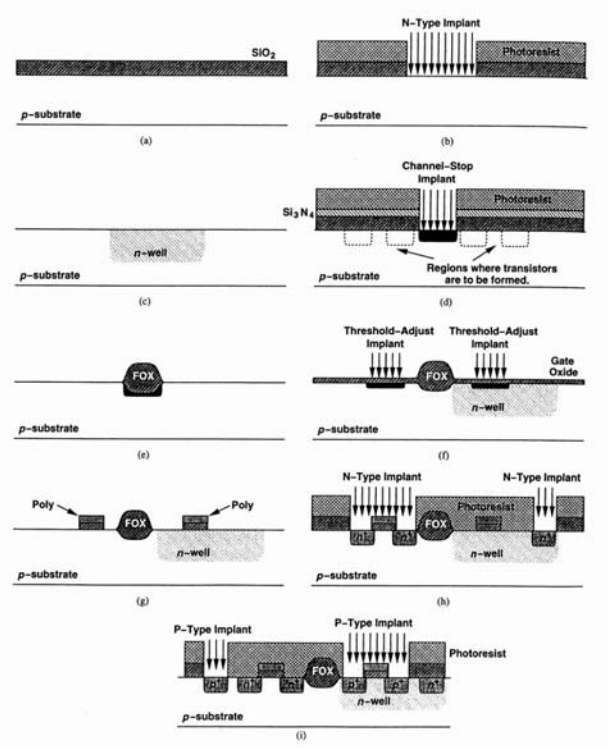
plasma etching

Reactive ion etching

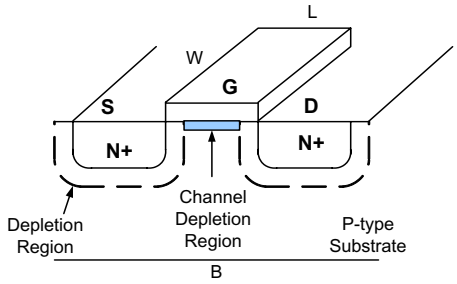
Layout Example of PMOS Transistor



Process Flow



Calculation of Threshold Voltage



Assume $V_{DS} = 0$.
As voltage is applied to the gate, a depletion region forms in p-type substrate.

$\nabla^2\phi = -\frac{\rho}{\varepsilon} = \frac{qN_A}{\varepsilon}$, where N_A is density of acceptors in p-type substrate. Integrating twice in vertical (x) direction yields

$\phi = \frac{qN_A}{\varepsilon}\frac{x_D^2}{2}$, where x_D is the depletion depth.

Therefore $x_D = \sqrt{\frac{2\varepsilon\phi}{qN_A}}$

The charge exposed per unit area $Q_{dep} = qN_A x_D = \sqrt{2qN_A\varepsilon\phi}$

When ϕ reaches 2 ϕ_F inversion occurs where ϕ_F is the Fermi level. An increase in ϕ results in no further increase in x_D but electrons

can flow from the source/drain. This forms a channel between source and drain.

The voltage on the gate required to produce inversion is called the threshold voltage, V_T.

$$V_T = 2\phi_F + \frac{Q_{dep}}{C_{ox}} + \phi_{ms} - \frac{Q_{SS}}{C_{ox}}$$

ϕ_{ms} is the work function difference between gate metal and Si.

Q_{SS} is the surface charge at Si – SiO_2 interface.

C_{ox} is the capacitance per unit area of the gate oxide.

$$V_T = \underbrace{2\phi_F + \phi_{ms} - \frac{Q_{SS}}{C_{ox}} + \frac{Q_{dep0}}{C_{ox}}}_{V_{T0}} + \underbrace{\frac{Q_{dep} - Q_{dep0}}{C_{ox}}}_{\text{Correction term}}$$

$$\frac{Q_{dep} - Q_{dep0}}{C_{ox}} = \frac{\sqrt{2qN_A\varepsilon(2\phi_F + V_{SB})} - \sqrt{2qN_A\varepsilon(2\phi_F)}}{C_{ox}}$$

$$\frac{Q_{dep} - Q_{dep0}}{C_{ox}} = \frac{\sqrt{2qN_A\varepsilon}}{C_{ox}}\left(\sqrt{(2\phi_F + V_{SB})} - \sqrt{2\phi_F}\right)$$

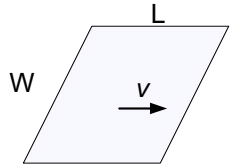
$\gamma = \frac{\sqrt{2qN_A\varepsilon}}{C_{ox}}$ and is typically about 0.5 $V^{0.5}$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.45\,fF/\mu^2$ for t_{ox} = 10 nm = oxide thickness

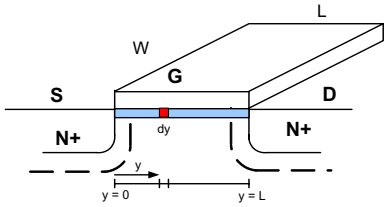
$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

$\varphi_F = \frac{KT}{q}\ln(\frac{N_A}{n_i})$ where n_i is the intrinsic impurity concentration of silicon.

Derivation of Non-saturation Equation



If Q_A is the charge per unit area, then the current $I = \frac{Q}{t} = Q_A W\frac{(vt)}{t} = Q_A W v$, where the *v* is the velocity.
Now consider the channel when $V_{GS} > V_T$ and $V_{DS} = 0$.



The charge induced in the channel is

$$Q_I = C_{ox} WL(V_{GS} - V_T)$$

If $V_{DS} > 0$ then the surface potential is a function of position

V(y=0) = 0 and V(y=L) = V_{DS}

The charge per unit area is

$$Q_I(y) = C_{ox}(V_{GS} - V_T - V(y))$$

$$I_{DS} = -Q_I W v = -Q_I W \mu E = -Q_I W(-\mu \frac{dV}{dy})$$

$$I_{DS} = \mu C_{ox} W (V_{GS} - V_T - V(y)) \frac{dV}{dy}$$

$$\int_0^L I_{DS} dy = \mu C_{ox} W \int_0^{V_{DS}} (V_{GS} - V_T - V(y)) dV$$

$$I_{DS} L = \mu C_{ox} W \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] = K' \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

where $K' = \mu C_{ox}$ and $K = K' \frac{W}{L} = \mu C_{ox} \frac{W}{L}$.

This equation is only valid for $V_{DS} \leq V_{GS} - V_T$

For $V_{DS} = V_{GS} - V_T$, $I_{DS} = \frac{K'}{2} \frac{W}{L} (V_{GS} - V_T)^2$

When $V_{DS} = V_{GS} - V_T$, the value of V_{DS} is called V_{DSsat}

$Q_I(L) = C_{ox} WL(V_{GS} - V_T - V_{DS}) = 0$, implying there is no mobile charge, which can not be true!

Channel Length Modulation

Above V_{DSsat} channel pinches off at drain end

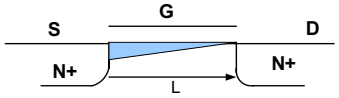
$$I_{DS} = \frac{K'}{2} \frac{W}{L_{eff}} (V_{GS} - V_T)^2$$

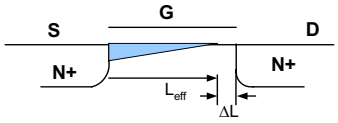
$L_{eff} = L - \Delta L$

$$\frac{1}{L_{eff}} = \frac{1}{L(1 - \frac{\Delta L}{L})} \approx \frac{1}{L}\left(1 + \frac{\Delta L}{L}\right)$$

To first order $\frac{\Delta L}{L} \propto V_{DS}$ or $\frac{\Delta L}{L} = \lambda V_{DS}$

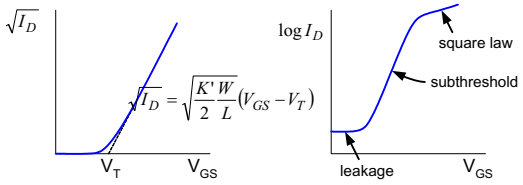
$$I_{DS} = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \text{for } V_{DS} > V_{GS} - V_T$$





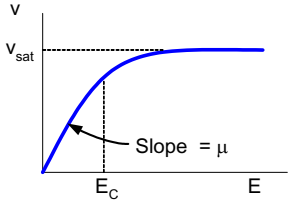
Second order effects in MOSFETs

Subthreshold conduction



$$I_D = K_x \frac{W}{L} e^{V_{GS}/nV_{th}} \left(1 - e^{-V_{DS}/V_{th}}\right)$$

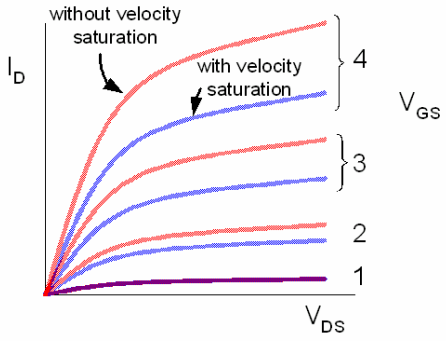
Velocity saturation



$$v = \frac{\mu E}{1 + E/E_C}$$

For a 1μ device with V_{DS} > 2 V, the electron velocity is saturated

$I_D \propto (V_{GS} - V_t)$ but not a square law



Hot electron effects

High field in drain region give enough energy for carriers to enter oxide.

changes V_{TO} over time

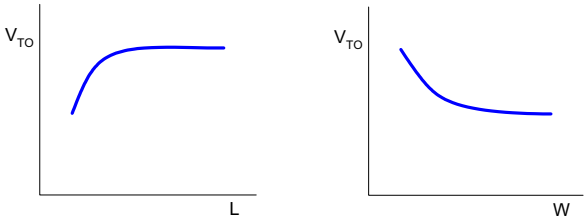
leads to significant substrate currents - r_{db} term

Small geometry effects on V_{TO} and γ

Gate Length

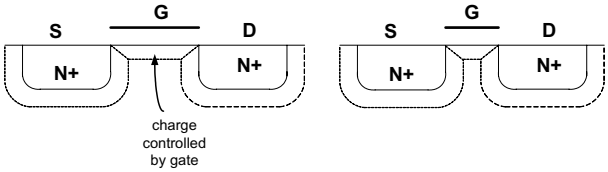
V_{TO} decreases as L decreases because more of depletion region controlled by source and drain

γ decreases because substrate has less effect



Gate Width
V_{TO} increases as W decreases because field under gate weakened by fringing effects
γ increases because more charge controlled by body

Drain induced barier lowering (DIBL)
The drain acts as a second gate and modulates the depletion charge $\Rightarrow$ shift in V_{TO}



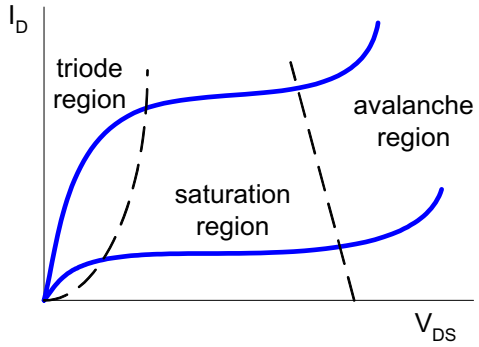
$$V_{TO}' = V_{TO} - \Delta V_T(L) - \Delta V_T(V_{DS}) + \Delta V_T(W)$$

Punch through

The drain source depletion regions reach one another resulting in current below surface

Avalanche breakdown

Electron-hole pairs create additional e-h pairs at high V_{ds}



SPICE

Example SPICE circuit to measure I-V curves of N-channel MOSFET
WinSpice 3 is a free interactive SPICE program

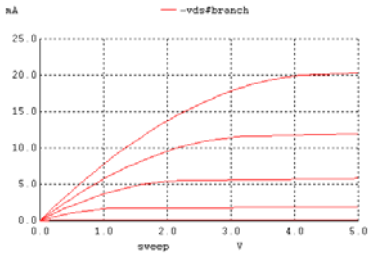
Input file
Circuit Title
*First line is the title line comment line! SPICE will ignore it
* an asterisk at beginning of line is a comment line

* voltage sources
vds 3 0 5V
vss 2 0 0
vgs 1 0 2

m1 3 1 2 2 cmosn l=1u w=10u ad=20p as=20p pd=24u ps=24u

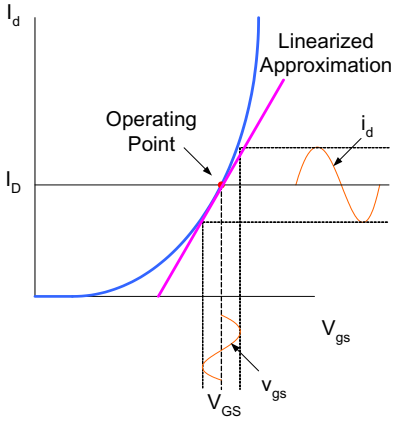
.MODEL CMOSN NMOS (LEVEL = 1 VTO=0.7 KP=200u
+GAMMA=0.5 LAMBDA=0.02 PHI=0.7)

*scans vds in 0.1 volt increments from 0 to 5 V for 5 different
*values of vgs: 1, 2, 3, 4, and 5 V
.dc vds 0 5 0.1 vgs 1 5 1
.plot -i(vds)
.end



Small-signal DC Model (low frequency)

Analog circuits often operate with signal levels that are small compared to bias currents and voltages.
Small-signal (linear) models are useful to predict circuit operation



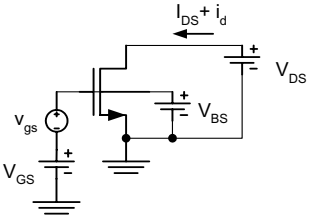
Small signal operation

Nomenclature

Lower case is used for small-signal values.
Upper case with upper case subscripts is used for DC biases.
Upper case with lower case subscripts is used for total signal.

g_m: small-signal transconductance

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{i_d}{v_{gs}}$$



In saturation: assuming $\lambda V_{DS} << 1$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = K'\frac{W}{L}(V_{GS} - V_T)$$

$$V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}}$$

$$g_m = K'\frac{W}{L}\sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}} = \sqrt{2K'\frac{W}{L}I_{DS}}$$

In non-saturation: $g_m = \frac{\partial I_d}{\partial V_{gs}} = K'\frac{W}{L}V_{DS}$

Where is region where small-signal model is accurate?

Assume $V_{BS} = 0$ and the transistor is in saturation

$$I_{DS} + i_d = \frac{1}{2}K'\frac{W}{L}\left(V_{GS} - V_T + v_{gs}\right)^2$$

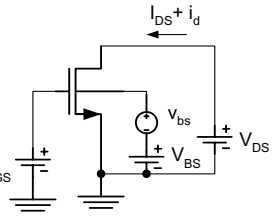
Consider the function $(x+\delta)^2 = x^2 + 2x\delta + \delta^2$. In order for linear approximation to be accurate $\frac{\delta^2}{2x\delta} << 1$ or $\frac{\delta}{2x} << 1$.

Therefore $\frac{v_{gs}}{2(V_{GS} - V_T)} << 1$ in order for i_d to be accurate

Note that by increasing $V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}}$ the region of small-signal (linear) operation can be increased.

g_{mb}: small-signal substrate transconductance

$$g_{mb} = \frac{\partial I_d}{\partial V_{bs}} = \frac{i_d}{v_{bs}}$$



Saturation: assuming $\lambda V_{DS} << 1$

$$g_{mb} = \frac{\partial I_d}{\partial V_{bs}} = -K'\frac{W}{L}(V_{GS} - V_T)\frac{\partial V_T}{\partial V_{bs}}$$

$$g_{mb} = K'\frac{W}{L}(V_{GS} - V_T)\frac{\partial V_T}{\partial V_{sb}} = g_m\frac{\partial V_T}{\partial V_{sb}}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}\right)$$

$$\frac{\partial V_T}{\partial V_{sb}} = \frac{\gamma}{2\sqrt{V_{SB} + \Phi}} \equiv \eta$$

$$\therefore g_{mb} = \eta g_m$$

$$\eta = \frac{g_{mb}}{g_m} \approx 0.1 \rightarrow 0.3$$

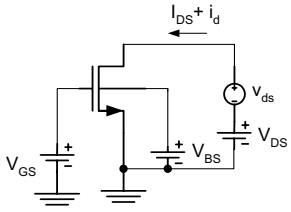
Non-saturation: assuming $\lambda V_{DS} << 1$

$$g_{mb} = \frac{\partial I_d}{\partial V_{bs}} = -K'\frac{W}{L}V_{DS}\frac{\partial V_T}{\partial V_{bs}} = K'\frac{W}{L}V_{DS}\frac{\partial V_T}{\partial V_{sb}} = \eta g_m$$

In both cases $g_{mb} = \eta g_m$

g_{ds}: small-signal drain-source conductance

$$g_{ds} = \frac{\partial I_d}{\partial V_{ds}} = \frac{i_d}{v_{ds}}$$



In saturation:

$$g_{ds} = \frac{\partial I_d}{\partial V_{ds}} = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2\lambda$$

$$g_{ds} = \frac{\lambda I_D}{(1 + \lambda V_{ds})} \approx \lambda I_D \quad \text{if } \lambda V_{DS} << 1$$

$$\lambda = \frac{1}{I_d}\frac{\partial I_d}{\partial V_{ds}}$$

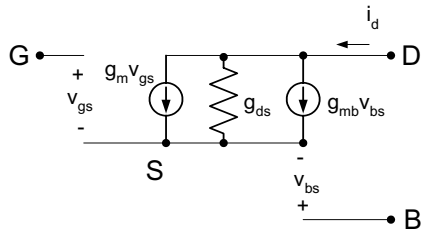
In non-saturation: assuming $\lambda V_{DS} << 1$

$$g_{ds} = \frac{\partial I_d}{\partial V_{ds}} = K'\frac{W}{L}(V_{GS} - V_T - V_{DS})$$

Small signal output resistance is r_0 $r_0 = \frac{1}{g_{ds}} = \left(\frac{\partial I_d}{\partial V_{ds}}\right)^{-1} = \frac{1}{\lambda I_d}$

DC small-signal equivalent circuit

$$i_d = g_m v_{gs} + g_{ds} v_{ds} + g_{mb} v_{bs}$$



Example: p-channel FET

$V_{T0} = -0.8$ V, $\lambda = 0.01$, $K_P' = 100\ \mu A/V^2$, $\gamma = 0.5\ V^{0.5}$, $\Phi = 0.8$ V
W = 10μ, L = 1μ
Calculate the small-signal parameters for $V_{GS} = -3$ V, $V_{DS} = -3$ V, $V_{BS} = 2$ V

$$V_T = V_{T0} - \gamma\left(\sqrt{\Phi + V_{BS}} - \sqrt{\Phi}\right)$$

$$V_T = -0.8 - 0.5\left(\sqrt{0.8 + 2} - \sqrt{0.8}\right) = -0.8 - 0.39 = -1.19V$$

$V_{SG} - |V_T| = 3 - |-1.19| = 1.81$ V

$V_{SD} = 3V > V_{SG} - |V_T| \quad \Rightarrow$ saturation region

$\lambda V_{SD} = 0.01(3) = 0.03 << 1$

$$I_{SD} \approx \frac{K_P'}{2}\frac{W}{L}\left(V_{SG} - |V_T|\right)^2 = \frac{100\mu}{2}\frac{10}{1}(1.81)^2 = 1.64mA$$

$$g_m = \sqrt{2K'\frac{W}{L}I_{SD}} = \sqrt{2(100\mu)\frac{10}{1}(1.64m)} = 1.81m\frac{A}{V} = 1.81mS$$

$$\eta = \frac{\gamma}{2\sqrt{V_{BS}+\Phi}} = \frac{0.5}{2\sqrt{2+0.8}} = 0.149$$

$$g_{mb} = \eta g_m = 0.149(1.81mS) = 0.27mS$$

$$g_{ds} = \lambda I_D = 0.01(1.64m) = 16.4\mu S$$

$$r_0 = \frac{1}{g_{ds}} = \frac{1}{16.4\mu} = 61K\Omega$$

Example: n-channel FET

V_{T0} = 0.8 V, λ = 0.01, K' = 100 μA/V^2, γ = 0.5 V$^{0.5}$, Φ = 0.8 V
W = 10μ, L = 1μ
Calculate the small-signal parameters for V_{GS} = 3 V, V_{DS} = 3 V, V_{SB} = -2 V

Since all parameters and voltages are the same (with appropriate negative signs) the small-signal parameters are the same:

g_m=1.81mS

g_{mb}=0.27mS

g_{ds}=16.4μS

r_0=61KΩ

MOS Single-Stage Amplifiers

Common-Source Amplifier

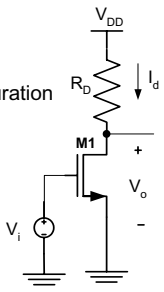
Common-source amplifier with resistive load

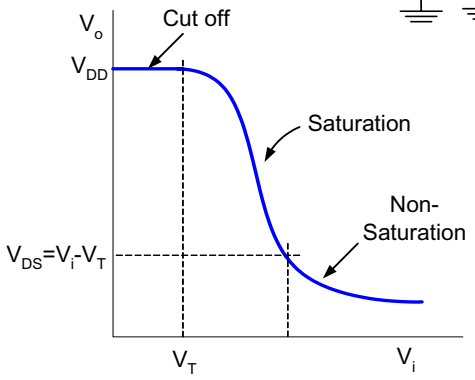
When V_i = 0, M1 cut off ⇒ I_D = 0, $V_o = V_{dd}$

When $V_i = V_{GS} > V_T$, $V_{DS} \approx V_{DD}$, FET enters saturation

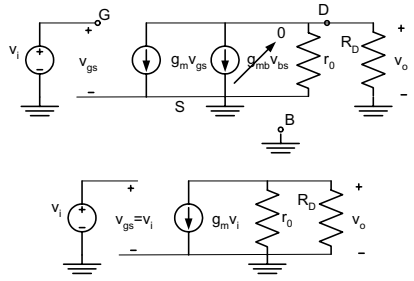
$$V_o = V_{DD} - I_D R_D = V_{DD} - \frac{K'}{2}\frac{W}{L}(V_i - V_T)^2 R_D$$

V_o decreases as V_i increases until M1 enters non-saturation ($V_o < V_i - V_T$)





Small Signal Analysis



$$v_o = -g_m v_i (r_o \parallel R_D) = -g_m v_i \frac{r_o R_D}{r_o + R_D}$$

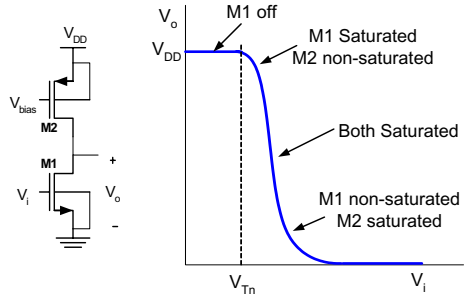
$$A_v = \frac{v_o}{v_i} = -g_m \frac{r_o R_D}{r_o + R_D} = -g_m \frac{r_o}{1 + \frac{r_o}{R_D}}$$

$$\lim_{R_D \to \infty} A_v = -g_m r_o$$

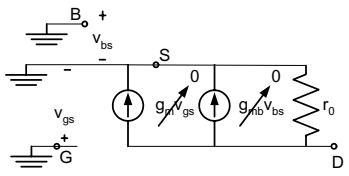
i.e. the maximum possible voltage gain is $-g_m r_o$

for $R_D << r_0$, $A_v = -g_m R_D$

Common-source amplifier with active load



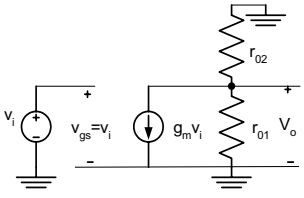
$v_{bs1} = v_{bs2} = 0$
$v_{gs2} = 0$, $v_{gs1} = v_i$



Therefore $g = \frac{1}{r_o}$

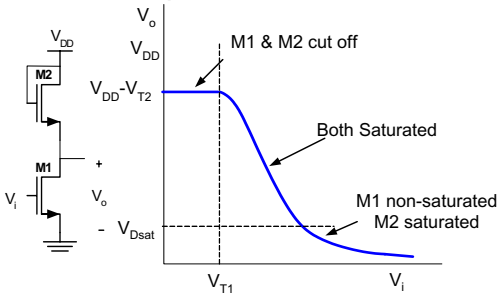
Small Signal Analysis

$$v_o = -g_m v_i (r_{o1} \parallel r_{o2})$$



$$A_v = \frac{v_o}{v_i} = -g_m\left(r_{o1} \parallel r_{o2}\right) = \frac{-g_m}{g_{o1} + g_{o2}}$$

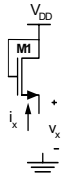
Common-source amplifier with N-channel load

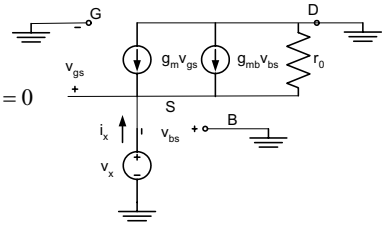


$$-I_x = I_{DS} = \frac{K'}{2}\frac{W}{L}\left(V_{DD} - V_x - V_T\right)^2$$

at $V_x = 0$, $\quad -I_x = I_{DS} = \frac{K'}{2}\frac{W}{L}\left(V_{DD} - V_T\right)^2$

at $V_x = V_{DD} - V_T$, $I_x = 0$



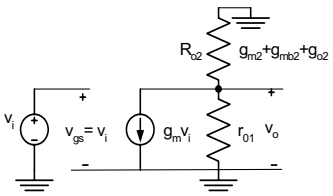


$v_{gs} = -v_x$, $v_{bs} = -v_x$

$$i_x + g_m v_{gs} + g_{mb} v_{bs} - g_o v_x = 0$$

$$\therefore i_x = \left(g_m + g_{mb} + g_o\right)v_x$$

$$g = \frac{i_x}{v_x} = g_m + g_{mb} + g_o$$



Small Signal Analysis

$$v_o = -g_{m1}v_i\left(r_{o1} \parallel R_{o2}\right)$$

$$A_v = \frac{v_o}{v_i} = \frac{-g_{m1}}{g_{o1} + g_{m2} + g_{mb2} + g_{o2}}$$

since $g_m >> g_o, g_{mb}$ $\qquad A_v \approx \frac{-g_{m1}}{g_{m2}}$

Remarks

Voltage gain is low ~ 10 or 20

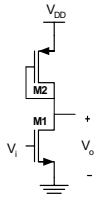
$$A_v \approx \frac{-g_{m1}}{g_{m2}} = \frac{\sqrt{2I_D K'\left(W/L\right)_1}}{\sqrt{2I_D K'\left(W/L\right)_2}} = \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

i.e. independent of the dc operating point when both devices in saturation

With P-channel diode connected load, similar result but no body effect

$$A_v = \frac{v_o}{v_i} = \frac{-g_{m1}}{g_{o1} + g_{m2} + g_{o2}}$$

$$A_v \approx \frac{\sqrt{\mu_n\left(W/L\right)_1}}{\sqrt{\mu_p\left(W/L\right)_2}}$$

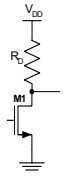


Common Source Amplifier Summary

Resistor load

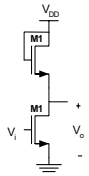
Gain a function of bias
Large variations in passive loads

$$A_v = -g_m R_D$$



N-channel diode connected load

Improved linearity
Controlled gain
Gain small ≤ 10
Low output swing

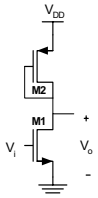


$$A_v \approx \frac{\sqrt{\left(W/L\right)_1}}{\sqrt{\left(W/L\right)_2}}$$

P-channel diode connected load

No body effect

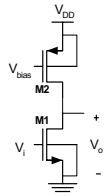
$$A_v \approx \frac{\sqrt{\mu_n\left(W/L\right)_1}}{\sqrt{\mu_p\left(W/L\right)_2}}$$



P-channel active load

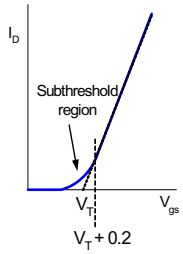
Higher gain
Output bias not well defined – Needs feedback
Large swing

$$A_v = -g_m\left(r_{o1} \parallel r_{o2}\right)$$



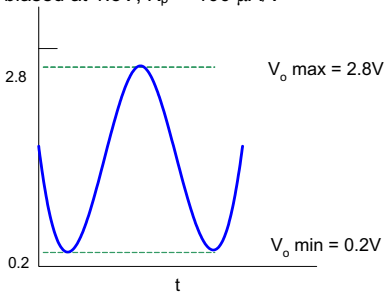
How low can V_o go?

For saturation $V_{DS} > V_{GS} - V_T > 0.2$



Example

For V_{DD} = 3V, I_D =100mA,
biased at 1.5V, K_p' = 100 μA/V²



V_o amplitude ~ 1.3V without distortion

At edge of triode/saturation

$$I_{DS} = \frac{K'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 = \frac{K'}{2}\frac{W}{L}V_{DS}^{\ 2}$$

$$V_{DS} = \sqrt{\frac{2I_{DS}}{K'\frac{W}{L}}} = 0.2 \Rightarrow \left(\frac{W}{L}\right)_2 = \frac{2I_{DS}}{K'V_{DS}^{\ 2}} = \frac{2\times100\times10^{-6}}{100\times10^{-6}(0.2)^2} = 50$$

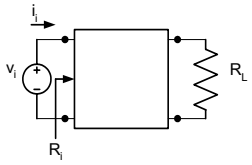
Can choose $\left(\frac{W}{L}\right)_2 = \frac{50\mu}{1\mu}$

Amplifiers

Parameters of interest and how they are measured

R_i

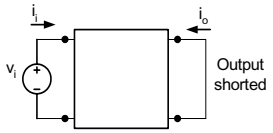
$$R_i = \frac{v_i}{i_i}$$



G_m and A_i

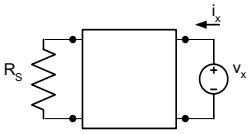
$$G_m = \frac{i_o}{v_i}$$

$$A_i = \frac{i_o}{i_i} = \frac{i_o}{v_i}\frac{v_i}{i_i} = G_m R_i$$



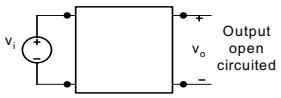
R_o

$$R_o = \frac{v_o}{i_o}$$

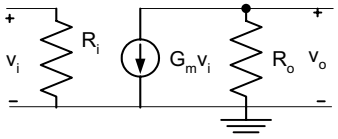


A_v

$$A_v = \frac{v_o}{v_i} = -G_m R_o$$

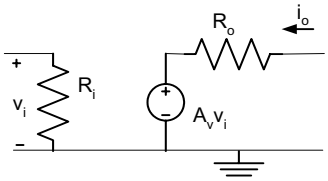


Amplifier Representation

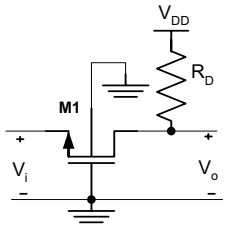


Alternative representation

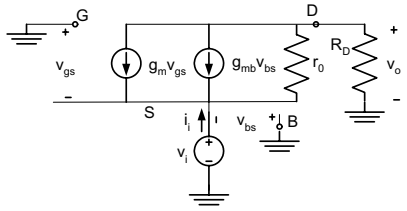
Using Thevenin's equivalent where $A_v = -G_m R_o$



Common Gate Amplifier



Small signal analysis



$$v_{gs} = v_{bs} = -v_i$$

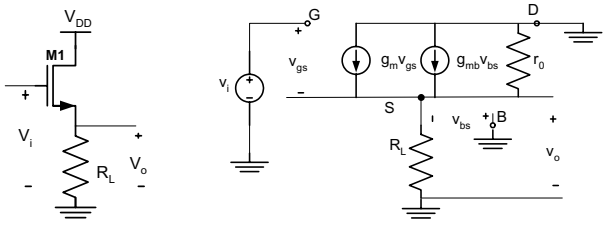
$$v_o = -\left(g_m v_{gs} + g_{mb} v_{bs}\right) R_D = +\left(g_m + g_{mb}\right) v_i R_D$$

$$\therefore A_v = \frac{v_o}{v_i} = +\left(g_m + g_{mb}\right) R_D$$

$$i_i = \left(g_m + g_{mb}\right) v_i \qquad R_i = \frac{v_i}{i_i} = \frac{1}{g_m + g_{mb}}$$

$$G_m = g_m + g_{mb} \qquad R_o = R_D$$

Common Drain Amplifier (Source Follower)



$$v_i = v_{gs} + v_o; \qquad v_{bs} = -v_o$$

$$g_m v_{gs} + g_{mb} v_{bs} - \frac{v_o}{R_L} - \frac{v_o}{r_o} = 0$$

$$g_m (v_i - v_o) - g_{mb} v_o - v_o \left(\frac{1}{R_L} + \frac{1}{r_o}\right) = 0$$

$$\left(g_m + g_{mb} + g_o + g_L\right) v_o = g_m v_i$$

$$\therefore A_v = \frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb} + g_o + g_L}$$

If g_o is negligible compared to g_m $\quad A_v \approx \dfrac{g_m}{g_m + g_{mb} + g_L}$

If $R_L \rightarrow \infty$, $g_L \rightarrow 0 \Rightarrow$ $\quad A_v \approx \dfrac{g_m}{g_m + g_{mb}} = \dfrac{1}{1 + \frac{g_{mb}}{g_m}} = \dfrac{1}{1+\eta}$

Since η ~0.2 the source follower gain doesn't approach unity as $R_L \rightarrow \infty$. A MOSFET in a well with the body tied to the source would result in unity gain for large R_L.

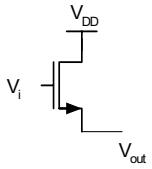
Output Resistance

$$R_o = \frac{1}{g_m + g_{mb}} \quad \text{for large } R_L$$

Source followers used as
buffers because of low R_o
Level shifters – the value of V_{gs} can be set to an arbitrary value by choosing proper W/L ratio

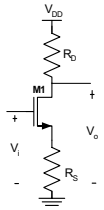
Remark

The region of operation is always saturation
$V_{GS} = V_i - V_{out}$; $V_{DS} = V_{DD} - V_{out}$
If V_i is small, then V_{GS} is small and V_{DS} is large
$V_{i\,max} = V_{DD} \rightarrow V_{GS\,max} = V_{DD} - V_{out} \rightarrow$ saturation



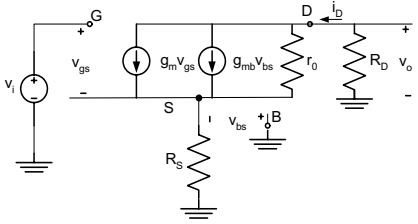
Common source amplifier with source degeneration

Source degeneration reduces G_m but increases R_o



Small signal analysis

$v_i = v_{gs} + v_s; \quad v_{bs} = -v_s$



$$A_v = \frac{v_o}{v_i} = -G_m R_o \parallel R_D$$

Calculation of G_m

$$i_D = g_m v_{gs} + g_{mb} v_{bs} - \frac{v_S}{r_o}$$

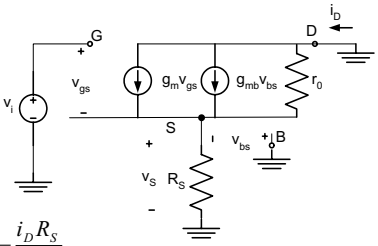
$$i_D = g_m (v_i - v_s) - g_{mb} v_S - \frac{v_S}{r_o}$$

$$but \quad v_S = i_D R_S$$

$$i_D = g_m (v_i - i_D R_S) - g_{mb} i_D R_S - \frac{i_D R_S}{r_o}$$

$$i_D \left(1 + g_m R_S + g_{mb} R_S + \frac{R_S}{r_o} \right) = g_m v_i$$

$$G_m = \frac{i_D}{v_i} = \frac{g_m}{1 + (g_m + g_{mb} + g_o) R_S}$$



Remark Original G_m was g_m, this is now reduced

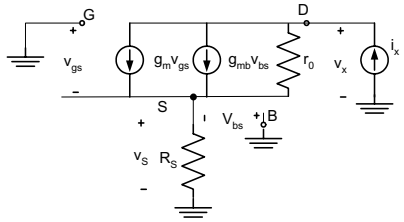
For large R_s

$$G_m \approx \frac{g_m}{(g_m + g_{mb}) R_S} = \frac{1}{\left(1 + \frac{g_{mb}}{g_m}\right) R_S} = \frac{1}{(1+\eta) R_S}$$

i.e. depends on the active device parameter η

Calculation of R_o

$$v_{gs} = v_{bs} = -v_S = -i_x R_S$$



$$v_x = v_s + (i_x - g_m v_{gs} - g_{mb} v_{bs}) r_o$$

$$v_x = i_x R_s + (i_x + (g_m + g_{mb}) i_x R_s) r_o$$

$$v_x = i_x (R_s + r_o + (g_m + g_{mb}) R_s r_o)$$

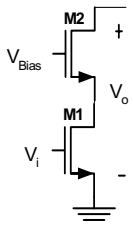
$$R_o = \frac{v_x}{i_x} = R_s + r_o + (g_m + g_{mb}) R_s r_o$$

i.e. R_o increases as R_s increases

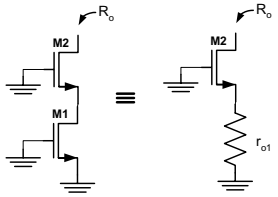
$$R_o \approx r_o (1 + g_m R_s)$$

Cascode Configuration

Connection of common source and common gate amplifiers
- High R_o
- High voltage gain
- Good high-frequency response



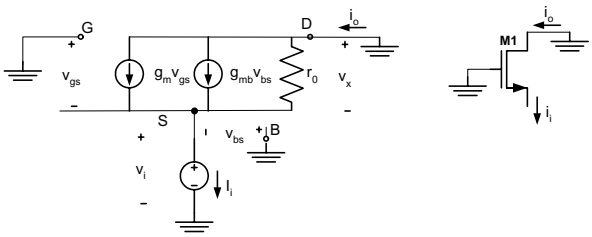
Calculate R_o



i.e. source degeneration with $R_S = r_{o1}$

$$R_o = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}$$

Calculate G_m



$i_o = i_i$ (current gain is unity)

$$G_m = \frac{i_0}{i_1} \frac{i_1}{v_1} = 1 \times g_{m1} = g_{m1}$$

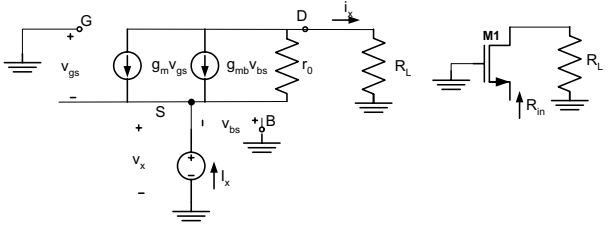
Unloaded voltage gain

$$A_v = G_m R_o = -g_{m1} \left[r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right]$$

$$A_v \approx -g_{m1} g_{m2} r_{o1} r_{o2}$$

This is the gain of two stages, one inverting and the other non-inverting

Input impedance at intermediate node



$$v_{gs} = v_{bs} = -v_x$$

$$i_x + g_m v_{gs} + g_{mb} v_{bs} - \frac{(v_x - i_x R_L)}{r_o} = 0$$

$$i_x - g_m v_x - g_{mb} v_x - \frac{v_x}{r_o} + \frac{i_x R_L}{r_o} = 0$$

$$i_x\left(1 + \frac{R_L}{r_o}\right) = \left(g_m + g_{mb} + \frac{1}{r_o}\right) v_x$$

$$\therefore R_i = \frac{v_x}{i_x} = \frac{1 + \frac{R_L}{r_o}}{g_m + g_{mb} + \frac{1}{r_o}}$$

Remarks

$g_m >> g_{mb}, 1/r_o \quad \Rightarrow \quad R_i = \frac{1}{g_m}\left(1 + \frac{R_L}{r_o}\right)$

if $R_L << r_o \quad \Rightarrow \quad R_i = \frac{1}{g_m} \quad \Rightarrow$ the voltage gain from input to intermediate node ~ 1

if $R_L >> r_o$ when R_L is due to a cascode active load

$R_L \approx r_o(1 + g_m r_o)$ then $R_i = \frac{1}{g_m}\left(1 + \frac{r_o(1 + g_m r_o)}{r_o}\right) \approx r_o$

The impedance of the intermediate node and therefore the voltage gain can be large if the load resistance is very large

Cascode gain stage

$R_{up} \approx g_m r_o^2$

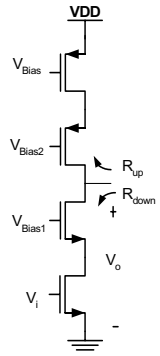
$R_{down} \approx g_m r_o^2$

$G_m = g_m$

$\therefore A_v = G_m\left(R_{up} \parallel R_{down}\right)$

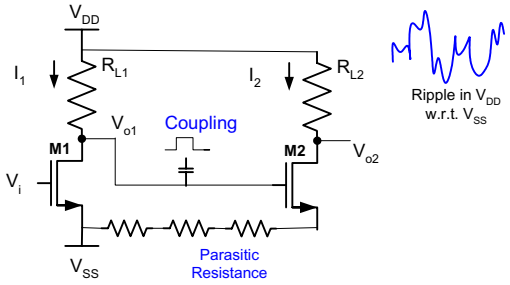
$A_v = -g_m\left(\frac{1}{2} g_m r_o^2\right) = -\frac{1}{2} g_m{}^2 r_o^2 = -\frac{1}{2}(g_m r_o)^2$

This is the gain of two stages.



Differential Signals

A single-ended circuit is subject to various noise sources



For M2: $V_{gs2} = (V_{DD} - I_1 R_{L1}) - V_{SS}$

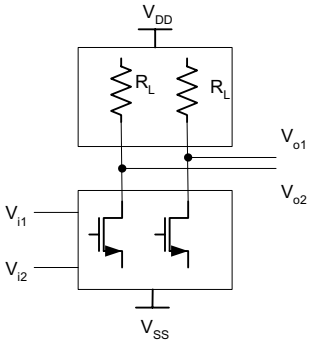
Any variation in V_{DD} with respect to V_{SS} will be amplified by M2 and cause spurious signals on the output (noise)

If the V_{SS} that M1 sees is different from M2 due to parasitic resistance, then a similar problem results

Capacitive coupling between other signals and the output of the first stage adds noise to the desired signal

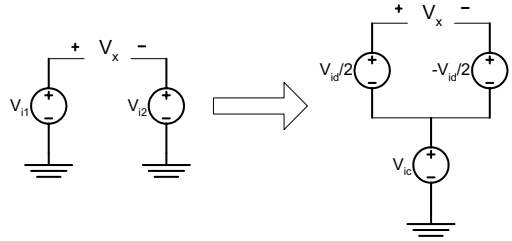
The problem is that the amplifiers amplify the voltage between the input terminal and V_{SS} and the output voltages are between the output terminal and V_{DD}.

A solution is to make amplifiers that amplify the voltage difference between 2 input terminals and deliver the output as a voltage difference between 2 output terminals.



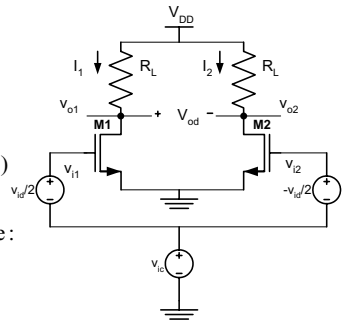
Noise that couple to both V_{i1} and V_{i2} leaves the difference V_{i1} - V_{i2} noise free.

Differential voltage $V_{id} = V_{i1} - V_{i2}$
Common-mode voltage $V_{ic} = ½ (V_{i1} + V_{i2})$



The key idea is to amplify the differential part of the signal and reject the common mode part of the signal.

One circuit approach



$v_{o1} = -g_m R_L v_{i1}$

$v_{o2} = -g_m R_L v_{i2}$

Output differential voltage:

$\therefore v_{o1} - v_{o2} = -g_m R_L (v_{i1} - v_{i2})$

$v_{od} = -g_m R_L v_{id}$

Output common mode voltage:

$v_{o1} + v_{o2} = -g_m R_L (v_{i1} + v_{i2})$

$v_{oc} = -g_m R_L (2v_{ic})$

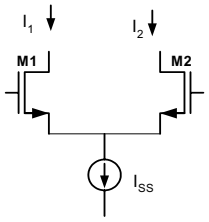
The input common-mode voltage is amplified along with the input differential signal. This circuit is that it does not reject the output common-mode voltage. Changing v_{ic} changes the currents I_1 and I_2.

Large signal common-mode output voltage

$$V_{oc} = \frac{1}{2}(V_{o1} + V_{o2}) = \frac{(V_{DD} - I_1 R_L) + (V_{DD} - I_2 R_L)}{2}$$

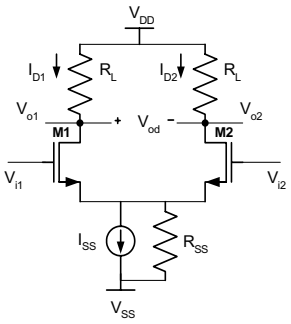
$$V_{oc} = V_{DD} - \frac{R_L}{2}(I_1 + I_2)$$

To keep V_{ocm} independent of V_{ic} need to keep $I_1 + I_2$ constant. This can be accomplished by using a current source and a source coupled pair.



$I_1 + I_2 = I_{SS}$ independent of V_{ic}

MOS source coupled pair



<u>DC transfer characteristics</u>

Want to find $\Delta I_D = I_{D1} - I_{D2}$ in terms of V_{id}

Each MOSFET is assumed to be in saturation

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{K'W/L}}$$

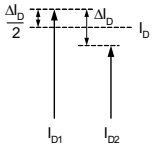
Assuming matched transistors

$$V_{T1} = V_{T2}; \qquad K'_1 = K'_2; \qquad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

$$V_{i1} - V_{i2} = V_{gs1} - V_{gs2} = V_{id} = \left(V_T + \sqrt{\frac{2I_{D1}}{K'W/L}}\right) - \left(V_T + \sqrt{\frac{2I_{D2}}{K'W/L}}\right)$$

$$V_{id} = \sqrt{\frac{2I_{D1}}{K'W/L}} - \sqrt{\frac{2I_{D2}}{K'W/L}} \qquad (1)$$

Define $I_{D1} = I_D + \frac{\Delta I_D}{2}$ and $I_{D2} = I_D - \frac{\Delta I_D}{2}$



At the source node $I_{D1} + I_{D2} = I_{SS} = 2I_D$

From equation (1) $V_{id}\sqrt{\frac{K'}{2}\frac{W}{L}} = \sqrt{I_{D1}} - \sqrt{I_{D2}}$

$$\therefore \frac{K'}{2}\frac{W}{L}V_{id}^2 = I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}} = I_{SS} - 2\sqrt{I_D^2 - \frac{\Delta I_D^2}{4}}$$

$$\frac{K'}{2}\frac{W}{L}V_{id}^2 = I_{SS} - \sqrt{4I_D^2 - \Delta I_D^2} = I_{SS} - \sqrt{I_{SS}^2 - \Delta I_D^2}$$

$$\sqrt{I_{SS}^2 - \Delta I_D^2} = I_{SS} - \frac{K'}{2}\frac{W}{L}V_{id}^2$$

$$I_{SS}^2 - \Delta I_D^2 = I_{SS}^2 + \left(\frac{K'}{2}\frac{W}{L}\right)^2 V_{id}^4 - 2I_{SS}\frac{K'}{2}\frac{W}{L}V_{id}^2$$

$$\Delta I_D^2 = 2I_{SS}\frac{K'}{2}\frac{W}{L}V_{id}^2 - \left(\frac{K'}{2}\frac{W}{L}\right)^2 V_{id}^4$$

$$\Delta I_D^2 = \left(\frac{K'}{2}\frac{W}{L}\right)^2 V_{id}^2 \left(\frac{2I_{SS}}{\frac{K'}{2}\frac{W}{L}} - V_{id}^2\right)$$

$$\therefore \Delta I_D = \frac{K'}{2}\frac{W}{L}V_{id}\sqrt{\frac{2I_{SS}}{\frac{K'}{2}\frac{W}{L}} - V_{id}^2}$$

With $V_{max} \equiv \sqrt{\frac{I_{SS}}{\frac{K'}{2}\frac{W}{L}}} \Rightarrow \frac{K'}{2}\frac{W}{L} = \frac{I_{SS}}{V_{max}^2}$

$$\Delta I_D = \frac{I_{SS}}{V_{max}^2}V_{id}\sqrt{2V_{max}^2 - V_{id}^2} = \sqrt{2}I_{SS}\left(\frac{V_{id}}{V_{max}}\right)\sqrt{1 - \frac{1}{2}\left(\frac{V_{id}}{V_{max}}\right)^2}$$

<u>Remark</u>

For $V_{id} = V_{max}$, $\Delta I_D = I_{SS}$

$I_{D1} = I_{SS}$

$I_{D2} = 0$

Therefore the above expressions are valid for $|V_{id}| \le V_{max}$

Let us plot I_{D1} as a function of V_{id}

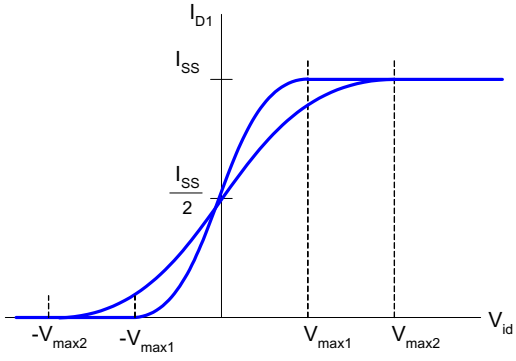
$$I_{D1} = I_D + \frac{\Delta I_D}{2} = \frac{I_{SS}}{2} + \frac{\Delta I_D}{2}$$

$$I_{D1} = \frac{I_{SS}}{2} + \frac{\sqrt{2}}{2}I_{SS}\frac{V_{id}}{V_{max}}\sqrt{1 - \frac{1}{2}\left(\frac{V_{id}}{V_{max}}\right)^2}$$

When $V_{id} = 0$, $I_{D1} = \frac{I_{SS}}{2}$

When $V_{id} = -V_{max}$, $I_{D1} = 0$

When $V_{id} = V_{max}$, $I_{D1} = I_{SS}$



V_{max} depends on device geometry and I_{SS}

$$V_{max} = \sqrt{\frac{I_{SS}}{\frac{K'}{2}\frac{W}{L}}}$$

As $\frac{W}{L}$ increases, V_{max} decreases

Calculation of G_m

$$G_m = \left.\frac{\partial I_{D1}}{\partial V_{id}}\right|_{V_{id}=0}$$

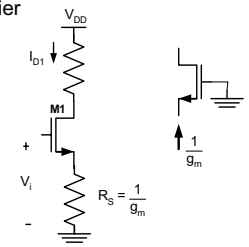
$$G_m = \left[\frac{\sqrt{2}}{2}\frac{I_{SS}}{V_{\max}}\sqrt{1-\frac{1}{2}\left(\frac{V_{id}}{V_{\max}}\right)^2} - \sqrt{2}I_{SS}\frac{V_{id}}{V_{\max}}\left(1-\frac{1}{2}\left(\frac{V_{id}}{V_{\max}}\right)^2\right)^{-\frac{1}{2}}\right]_{V_{id}=0}$$

$$G_m = \frac{\sqrt{2}}{2}\frac{I_{SS}}{V_{\max}} = \frac{1}{2}\frac{\sqrt{2}I_{SS}}{\sqrt{\frac{I_{SS}}{2}\frac{W}{L}}} = \frac{1}{2}\sqrt{2K'\frac{W}{L}\frac{I_{SS}}{2}} = \frac{1}{2}g_{m1}$$

Remark

The source-coupled (SC) pair can be thought of as a source degenerated common source amplifier

$$\frac{i_{d1}}{v_i} = G_m = \frac{g_m}{1+g_m R_S} = \frac{g_m}{1+1} = \frac{g_m}{2}$$



Small signal analysis

Define two small signal quantities

$v_{id} = v_{i1} - v_{i2} = \text{differential mode signal}$

$v_{ic} = \frac{v_{i1}+v_{i2}}{2} = \text{common mode signal}$

$\therefore \quad v_{i1} = \frac{v_{id}}{2} + v_{ic}$

$v_{i2} = -\frac{v_{id}}{2} + v_{ic}$

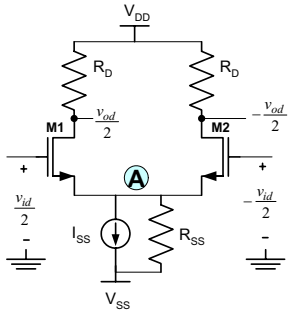
When the amplifier amplifies the voltage difference and rejects the common mode then it is a desirable situation

Any common variations in the input signal are cancelled out when using the difference voltage (i.e. supply voltage variations, coupling, etc.)

Differential-mode gain A_{dm} (v_{ic} = 0)

$$v_{i1} = \frac{v_{id}}{2} + v_{ic}$$

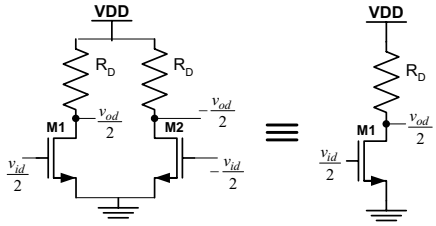
$$v_{i2} = -\frac{v_{id}}{2} + v_{ic}$$



The circuit is perfectly balanced and symmetrical

Node A does not experience any change in voltage. Signals at the gates of M1 and M2 are equal and opposite ⇒ node A is at an ac ground

Can use a simplified half circuit for analysis



Half CIrcuit

The differential mode half circuit is a common source amplifier

$$\frac{v_{od}}{2} = -g_m\left(R_D \,\|\, r_o\right)\frac{v_{id}}{2}$$

$$\therefore A_{dm} = \frac{v_{od}}{v_{id}} = -g_m\left(R_D \,\|\, r_o\right)$$

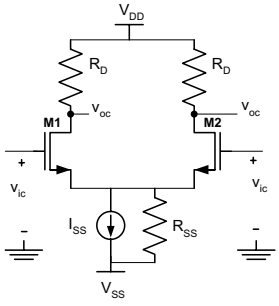
$$A_{dm} \approx -g_m R_D \quad \text{for} \quad r_o >> R_D$$

Common mode gain A_{cm} (v_{id} = 0)

$v_{i1} = v_{ic}$

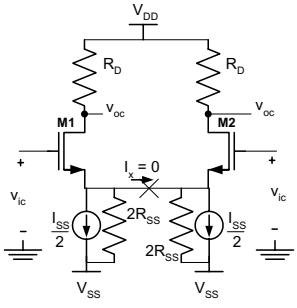
$v_{i2} = v_{ic}$

The drain currents must be identical



R_{ss} and I_{ss} can be split in 2 as shown

No current will flow in the lead connecting the two sources

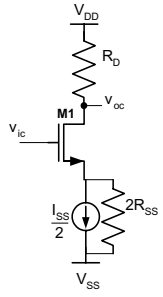


The common mode half circuit is a source degenerated SC pair

$$G_m = \frac{g_m}{1+g_m(2R_{SS})} \text{ and}$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -G_m\left(R_D \,\|\, r_o\right)$$

$$A_{cm} \approx \frac{-g_m R_D}{1+2g_m R_{SS}} \quad \text{for} \quad r_o >> R_D$$



Common Mode Rejection Ratio (CMRR)

$$CMMR \equiv \left|\frac{A_{dm}}{A_{cm}}\right|$$

Desired signal – differential signal
Undesired signal – common mode signal

Desire large CMRR

CMRR for MOS SC pair

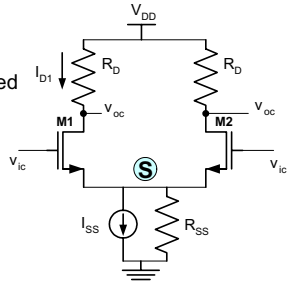
$$CMMR \equiv \frac{g_m R_D}{\frac{g_m R_D}{1+2g_m R_{SS}}} = 1+2g_m R_{SS}$$

CMRR improved if R_{ss} is large i.e. need a good quality current source

Input Common-mode range

Range of input common mode voltage that will keep transistors in saturation

For M1 (M2) in saturation



$$V_{DS} = V_{DD} - I_{D1}R_D - V_S$$
$$V_{GS} = V_{ic} - V_S$$
$$saturation: \quad V_{DS} \geq V_{Dsat} = V_{GS} - V_T$$
$$\therefore V_{DD} - I_{D1}R_D - V_S \geq V_{ic} - V_S - V_T$$
$$\Rightarrow V_{ic} \leq V_{DD} - I_{D1}R_D + V_T$$
$$\therefore V_{ic(\max)} \leq V_{DD} - I_{D1}R_D + V_T$$

Need to make sure current source operates properly. Say a voltage V_I is required across the current source, then

$$V_{ic} - V_{GS1} \geq V_I$$
V_{GS1} is determined by amount of current through M1
$$V_{ic} \geq V_I + V_{GS1}$$
$$V_{ic(\min)} = V_{GS1} + V_I$$
$$V_{ic(\min)} = V_{Dsat1} + V_T + V_I$$
$$V_{Dsat1} = V_{\max} \text{ at } I_{SS}$$
$$V_{Dsat1} = \frac{V_{\max}}{\sqrt{2}} \text{ at } \frac{I_{SS}}{2}$$

More on CMRR

$$CMRR \equiv \frac{g_m R_D}{\frac{g_m R_D}{1+2g_m R_{SS}}} = 1 + 2g_m R_{SS} \approx 2g_m R_{SS}$$
$$CMRR \approx 2\left(\frac{2I_{D1}}{V_{GS1} - V_T}\right)R_{SS}$$

$$I_{D1} = \frac{I_{SS}}{2} \Rightarrow CMRR \approx 2\frac{I_{SS}R_{SS}}{V_{GS1} - V_T}$$

For high CMRR:

Make ($V_{GS1} - V_T$) small but not in subthreshold region
Make $I_{ss}R_{ss}$ large i.e. good current source

CMRR expressed in dBs is $20\log\left|\frac{A_{dm}}{A_{cm}}\right|$

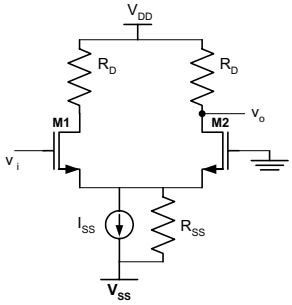
Example

$V_{T0} = 0.8$, $K' = 77\ \mu A/V^2$, $V_{SB} = 0$ V, $W = 10\mu$, $L = 2\mu$, $I_{SS} = 100\ \mu A$, $R_{SS} = 1M\Omega$, $R_D = 100K\Omega$

$$V_{GS} - V_T = \sqrt{\frac{2I_D}{K'\frac{W}{L}}} = \sqrt{\frac{I_{SS}}{K'\frac{W}{L}}} = \sqrt{\frac{100\mu}{77\mu\frac{10\mu}{2\mu}}} = 0.51V$$
$$CMRR = 20\log\left(\frac{2\times 100\mu\times 1M}{0.51}\right) = 52dB$$
$$g_m = \frac{2I_{D1}}{V_{GS1} - V_T} = \frac{I_{SS}}{V_{GS} - V_T} = \frac{100\mu A}{0.51V} = 196\mu A/V$$
$$A_{dm} = -g_m R_D = 196\mu \times 100K = -19.6$$
$$A_{cm} = \frac{-g_m R_D}{1+2g_m R_{SS}} = \frac{-19.6}{1+2(196\mu)(1M)} = -0.05$$

Single-ended Input to MOS SC pair

Now consider the case where the input signal v_i is applied to M1 and M2 is grounded and the output is taken at the drain of M2



$$v_o = -\frac{v_{od}}{2} + v_{oc}$$
$$v_o = -A_{dm}\frac{v_{id}}{2} + A_{cm}v_{ic}$$

Note that if the output is taken between one node and ground, the gain is ½ compared to taking the output differentially The common-mode gain is not halved.

$$v_{id} = v_i - 0 = v_i$$
$$v_{ic} = \frac{v_i + 0}{2} = \frac{v_i}{2}$$

Remark

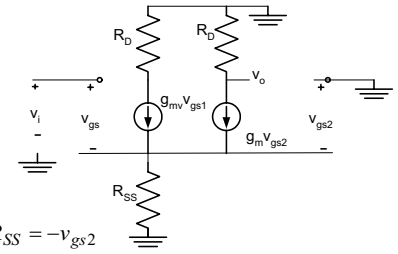
Note that it doesn't matter to A_{dm} if the input is applied all to one input or to both, only the magnitude of the difference matters.

It does matter to A_{cm} whether the input is applied differentially or to a single side since there is a common-mode component for a single-sided input.

$$v_o = -\frac{A_{dm}}{2}(v_i) + A_{cm}\left(\frac{v_i}{2}\right)$$
$$v_o = \left(\frac{19.6}{2} - \frac{0.05}{2}\right)v_i = 9.78v_i$$
$$\therefore Gain = \frac{v_o}{v_i} = 9.78$$

Small-signal circuit analysis (single-ended input)

Find $A_v = \frac{v_o}{v_i}$



$$v_o = -g_m R_D v_{gs2}$$
$$v_i = v_{gs1} - v_{gs2}$$
Also $(g_m v_{gs1} + g_m v_{gs2})R_{SS} = -v_{gs2}$
$$\therefore v_{gs1} = -\frac{(1+g_m R_{SS})}{g_m R_{SS}}v_{gs2}$$
Then $v_i = v_{gs1} - v_{gs2} = -\left[1 + \frac{(1+g_m R_{SS})}{g_m R_{SS}}\right]v_{gs2}$
or $v_{gs2} = -\frac{g_m R_{SS}}{1+2g_m R_{SS}}v_i$
$$\therefore A_v = \frac{v_o}{v_i} = g_m R_D\left(\frac{g_m R_{SS}}{1+2g_m R_{SS}}\right)$$

Remark

$$A_v = -\frac{A_{dm}}{2} + \frac{A_{cm}}{2}$$
$$A_v = \frac{1}{2}\left(g_m R_D - \frac{g_m R_D}{1+2g_m R_{SS}}\right)$$

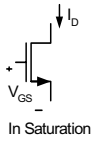
$$A_v = \frac{1}{2}\left(\frac{g_m R_D + 2g_m R_D g_m R_{SS} - g_m R_D}{1+2g_m R_{SS}}\right)$$

$$A_v = g_m R_D\left(\frac{g_m R_{SS}}{1+2g_m R_{SS}}\right) \quad \text{as expected!}$$

MOSFET Current Sources

Current sources are used as
- Biasing elements
- Load devices (instead of resistors) in amplifier stages
  - **High incremental resistance of current sources** ⇒
  - High voltage gain at low supply voltages
  - Requires less layout area than resistors

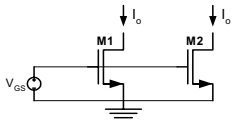
Key idea
If r_o is neglected, the current I_D of a FET is only a function of V_{GS} in saturation.



To generate a certain current I_o
Determine V_{GS} required to support I_o

$$V_{GS} = V_T + \sqrt{\frac{2I_o}{K'\frac{W}{L}}}$$ and apply across G-S of MOSFET in saturation.

Can also obtain multiple copies of I_o if M1 and M2 are identical.

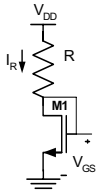


Generation of V_{GS}
M1 is always in saturation

$$V_{DD} = I_R R + V_{GS}$$

$$V_{DD} = I_R R + V_T + \sqrt{\frac{2I_R}{K'\frac{W}{L}}}$$

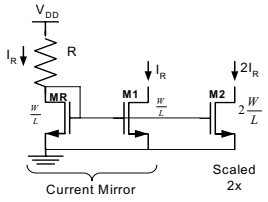
Solve for I_R



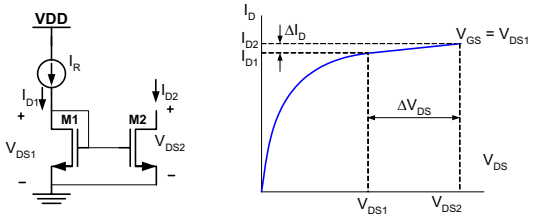
Simple MOS current source

In saturation, neglecting r_o

$$I_o = I_R \frac{\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)_R}$$



Effect of r_o



If V_{DS} of M1 and M2 are different then $I_{D2} \neq I_{D1}$

$$I_{D1} = \frac{1}{2}K'\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}K'\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS2})$$

$$\therefore \frac{I_{D2}}{I_{D1}} = \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \neq 1 \text{ as desired}$$

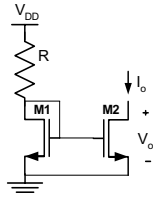
The error $\Delta I_D = \frac{\partial I_D}{\partial V_{DS}}\Delta V_{DS} = \lambda I_D \Delta V_{DS}$

Remarks
- Decreasing λ decreases the error ΔI_D - use long channel lengths
- If V_{DS1} and V_{DS2} are the same, mismatch in channel lengths lead to mismatches in λ and error in I_D

- For current source matching must use identical channel lengths
- Ratio of currents is set by channel width, W

Minimum possible voltage for proper operation

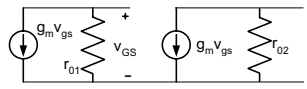
V_{omin} = minimum value of VDS of M2 that ensures saturation



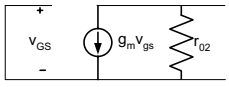
$$v_{o\,\min} = V_{Dsat} = V_{GS} - V_T = \sqrt{\frac{2I_o}{K'\frac{W}{L}}}$$

Small signal analysis

$v_{BS1} = v_{BS2} = 0$



Since V_{gs} is held fixed by I_R, $v_{gs} = 0$

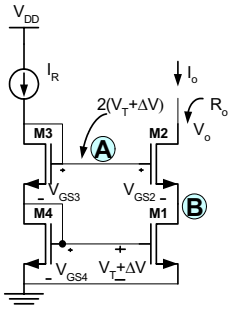


From the above simplified circuit $R_o = r_{o2}$

Desired properties of current sources
- Large output resistance R_o

- Large range of V_o for which R_o is high i.e. small V_{omin}
- Matching of currents

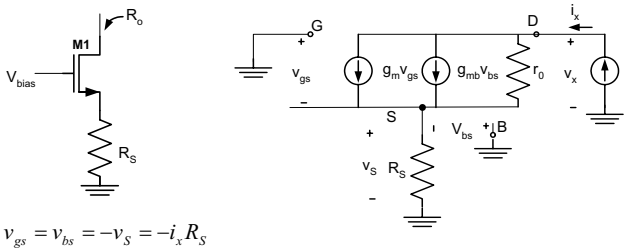
For the simple current source $R_o = r_{o2}$. How does one improve R_o?
One solution is to use a cascode connection, which gives a very high R_o.



MOS cascode current source

Calculation of R_o of cascode current source

First determine R_o of following circuit:



$$v_{gs} = v_{bs} = -v_S = -i_x R_S$$

$$v_x = v_s + (i_x - g_m v_{gs} - g_{mb} v_{bs}) r_o$$
$$v_x = i_x R_s + (i_x + (g_m + g_{mb}) i_x R_s) r_o$$
$$v_x = i_x (R_s + r_o + (g_m + g_{mb}) R_s r_o)$$
$$R_o = \frac{v_x}{i_x} = R_s + r_o + (g_m + g_{mb}) R_s r_o$$

We know that R_o of M1 in cascode current source = r_{o1}

Therefore in above circuit $R_S = r_{o1}$ and $r_o = r_{o2}$ so

$$R_o = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}$$

Can realize very high R_o by addition of more stacked cascode devices

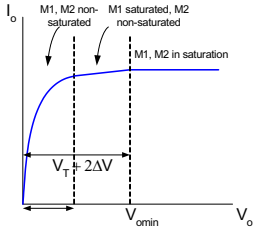
$$V_{GS4} = V_{GS3} = V_T + \sqrt{\frac{2I_R}{K'W/L}} = V_T + \Delta V$$

$$\Delta V = \sqrt{\frac{2I_R}{K'W/L}}$$

$$V_A = V_{GS3} + V_{GS4} = V_T + \Delta V + V_T + \Delta V$$
$$V_A = 2(V_T + \Delta V)$$

M2 is non-saturated when drain of M2 is lower than gate of M2 by V_T.

$$\boldsymbol{V_{DS2} = V_o - V_B}$$
$$\boldsymbol{V_{GS2} = 2(V_T + \Delta V) - V_B}$$
$$\boldsymbol{\therefore V_{GS2} - V_T = 2\Delta V + V_T - V_B}$$
$$\boldsymbol{V_{o\,min} = V_{GS2} - V_T + V_B = 2\Delta V + V_T}$$



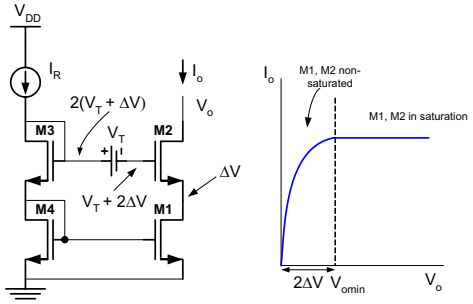
For a simple current source V_{omin} = ~1.1 – 1.4 V since ΔV ~ 250-300mV and V_T is typically between 0.6 and 0.8 V.

Problem
Although ΔV can be reduced by using large W, the V_T term represents a significant loss of voltage swing!

It would be nice if V_{omin} contained no V_T term

Lowest possible value for V_B is when M1 enters non-saturation
Bias M1 at the edge of saturation i.e. $V_B = \Delta V$
Need to bias V_A at $V_T + \Delta V$ above V_B for M2 to be in saturation
Thus V_A needs to be $V_T + 2\Delta V$ but the circuit generates $2(V_T + \Delta V)$ so we need a level-shifting arrangement of V_T

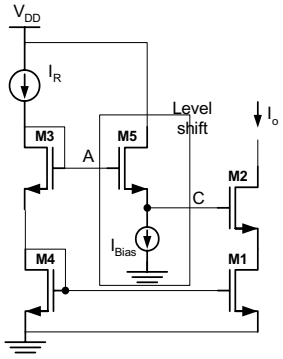
Conceptual picture



Practical implementation of V_T level shift

$$V_{GS5} = \Delta V + V_T$$
$$\Rightarrow V_C = V_A - (\Delta V + V_T)$$
$$With \quad V_A = 2(V_T + \Delta V)$$
$$\Rightarrow V_C = \Delta V + V_T$$

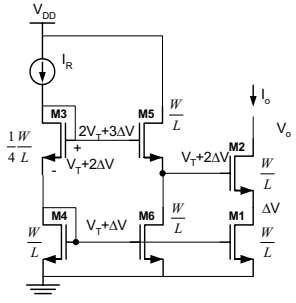
However, $V_C = V_T + 2\Delta V$ is what is required. Increase V_A by $\Delta V \Rightarrow$ V_{GS3} needs to increase by ΔV
$V_{GS3} = V_T + 2\Delta V \Rightarrow$ decrease W/L of M3 by 4x



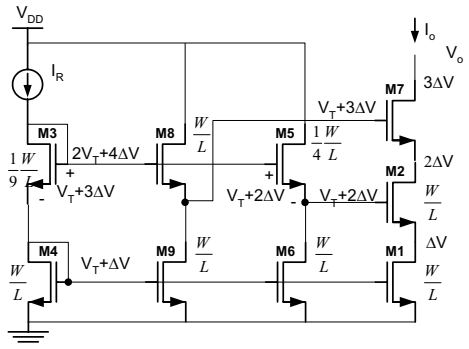
$$\Delta V = \sqrt{\frac{2I_D}{K'W/L}}; \quad 2\Delta V = 2\sqrt{\frac{2I_D}{K'W/L}} = \sqrt{\frac{2I_D}{K'\frac{W}{L}\frac{1}{4}}}$$

Also implement I_{Bias} with another mirror

This circuit is called a high-swing cascode
$V_{omin} = 2\Delta V$ ~ 500-600mV



Example (high-swing triple cascode)



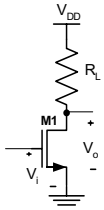
Current sources as active loads

Why active loads and not passive loads?

For the simple CS stage

$$A_v = \frac{v_o}{v_i} = -g_m R_L$$

$$A_v = -\frac{2I_D}{V_{GS}-V_T} R_L = -\frac{2}{V_{GS}-V_T}\{I_D R_L\}$$



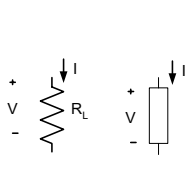
To obtain large gains $I_D R_L$ should be large. For M1 to be in saturation: $V_{omin} = V_{Dsat}$

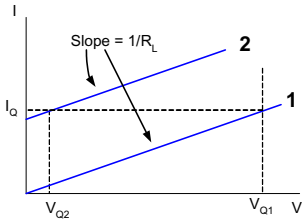
$V_{DD} = V_{omin} + I_D R_L$

Large implies V_{DD} should be large which is not always practical.

How do we overcome this problem?
Use a load element which has the following properties

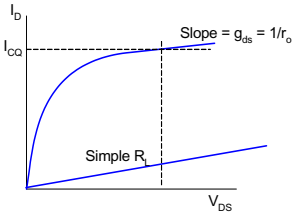
- A large variation in the voltage drop across it results in a small variation in the current through it. i.e. a large incremental resistance
- Support a large dc current without dropping a large dc voltage across itself





Both loads 1 and 2 show the same variation in I as V is varied (the slope is $1/R_L$ for both)

However, for a given bias current I_Q, load 2 produces a much smaller dc drop V_{Q2} than load 1 for which the drop is V_{Q1}



Recall the ID-VDS characteristic of a MOSFET. The equivalent small-signal resistance, as a load, is

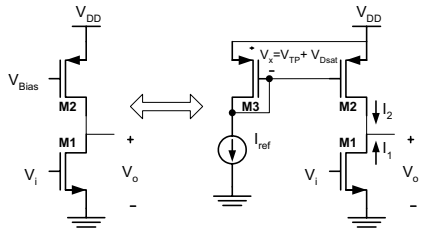
$$\frac{\partial V_{DS}}{\partial I_D} = r_o$$

$$r_o \approx \frac{1}{\lambda I_D} \Rightarrow r_o I_D = \frac{1}{\lambda} = 50V \quad \text{for } \lambda = 0.02\ \text{V}^{-1}$$

If a simple resistor of value r_o were used, then a 50 V drop would be required to support the same current.

Summary
Use of r_o of a MOSFET allows high voltage gain without requiring large power supply voltages.

Common source amplifier with active load



Assume M1, M2 and M3 are in saturation

$$V_x = V_{TP} + V_{Dsat} = V_{TP} + \sqrt{\frac{2I_{ref}}{K'(W/L)_3}}$$

$$I_{ref} = \frac{K_P'}{2}\left(\frac{W}{L}\right)_3 (V_x - V_{TP})^2 (1+\lambda_P V_x)$$

$$I_2 = \frac{K_P'}{2}\left(\frac{W}{L}\right)_2 (V_x - V_{TP})^2 (1+\lambda_P (V_{DD} - V_o))$$

$$with \quad \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 \quad we \quad have$$

$$I_2 = \frac{(1+\lambda_P(V_{DD}-V_o))}{(1+\lambda_P V_x)} I_{ref}$$

$$I_2 = I_1 = \frac{K_N'}{2}\left(\frac{W}{L}\right)_1 (V_i - V_{TN})^2 (1+\lambda_N V_o)$$

$$\therefore \frac{(1+\lambda_P(V_{DD}-V_o))}{(1+\lambda_P V_x)(1+\lambda_N V_o)} I_{ref} = \frac{K_N'}{2}\left(\frac{W}{L}\right)_1 (V_i - V_{TN})^2$$

$$Assume \quad \lambda_P(V_{DD}-V_o) << 1, \quad \lambda_P V_x << 1, \quad \lambda_N V_o << 1$$

$$\frac{1}{1+\delta} \approx 1-\delta \qquad \text{for } \delta << 1$$

$$(1+\delta)(1+\alpha) \approx 1+\delta+\alpha \qquad \text{for } \delta, \alpha << 1$$

$$\therefore \frac{K_N'}{2}\left(\frac{W}{L}\right)_1 (V_i - V_{TN})^2 \approx I_{ref}\left[(1+\lambda_P(V_{DD}-V_o))(1-\lambda_P V_x)(1-\lambda_N V_o)\right]$$

$$\approx I_{ref}\left[1+\lambda_P(V_{DD}-V_o)-\lambda_P V_x - \lambda_N V_o\right]$$

$$\approx I_{ref}\left[1+\lambda_P(V_{DD}-V_x)-(\lambda_P+\lambda_N)V_o\right]$$

solving for V_o we have

$$V_o = \frac{\lambda_P}{\lambda_P+\lambda_N}(V_{DD}-V_x) + \frac{1}{\lambda_P+\lambda_N}\left[1 - \frac{1}{I_{ref}}\frac{K_N'}{2}\left(\frac{W}{L}\right)_1 (V_i - V_{TN})^2\right]$$

Remark
V_o extremely sensitive to V_i and I_{ref}.

Example
If $V_{DD} = 5V$, $\lambda_p = \lambda_n = 0.02$, $V_x = 1.2V$

$$V_o = \frac{0.02}{0.04}(5-1.2) + \frac{1}{0.04}\left[1 - \frac{1}{I_{ref}}\frac{K_N'}{2}\left(\frac{W}{L}\right)_1 (V_i - V_{TN})^2\right]$$

$$V_o = \frac{1}{2}(3.8) + 25\left[1 - \frac{1}{I_{ref}}(\text{current from M1})\right]$$

The factor of 25 makes it difficult to bias properly in this configuration of current source biasing

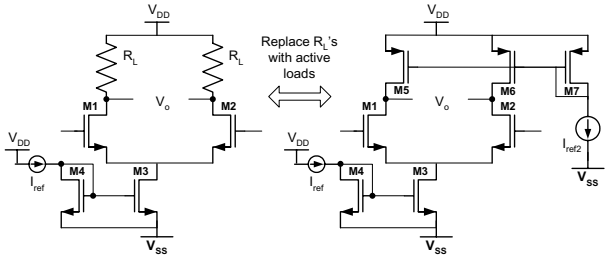
Remark

Small-signal analysis

$$A_v = -g_m(r_{o1} \| r_{o2})$$

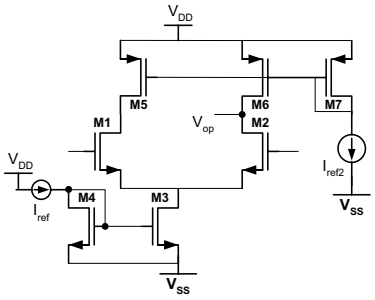
$$R_o = r_{o1} \| r_{o2}$$

Source-coupled pair with active load



Need to adjust I_{ref2} such that output common-mode (CM) voltage is at the desired value – difficult to do.

Suppose only a single-ended output is of interest, V_{op}.



Bias value of V_{op} extremely sensitive to I_{ref1} and I_{ref2}.

Need to modify the circuit to stabilize the bias voltages

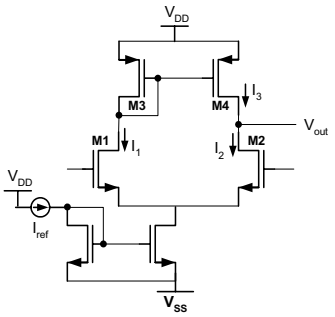
Remark

M2 and M3 form a cascode so the output is very sensitive to the voltage at the gate of M3/M4 i.e. I_{ref1}.

Use a current mirror for the active load ⇒ bias voltages get stabilized

If I_{ref} increases, then I_1 and I_2 increase because of M3/M4 current mirror, I_3 increases by an equal amount ⇒ I_2 and I_3 are equal

In the previous circuit they could be different.



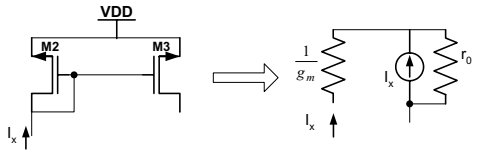
Consider a signal v_{id} applied to the input

If v_{id} increases, then I_1 increases and I_2 decreases
I_3 also increases because of the M3/M4 mirror
⇒ Current (I_2-I_3) is pumped into the output resistance at v_{out}, which if unloaded is $r_{o2}||r_{o4}$

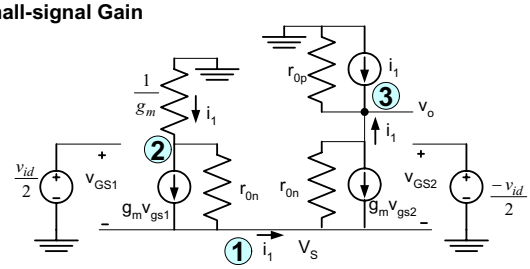
Small-signal analysis

Calculation of gain and R_o

Recall



Small-signal Gain



$$v_{gs1} = \frac{v_{id}}{2} - v_s \qquad v_{gs2} = -\frac{v_{id}}{2} - v_s$$

At node 3

$$i_1 + i_1 - \frac{v_o}{r_{op}} = 0$$

$$\therefore i_1 = \frac{v_o}{2r_{op}} \Rightarrow v_2 = -\frac{1}{2g_m r_{op}} v_o$$

At node 2

$$i_1 - g_m v_{gs1} - (v_2 - v_s)/r_{on} = 0$$

$$\frac{v_o}{2r_{op}} - g_m\left(\frac{v_{id}}{2} - v_s\right) - \left(-\frac{1}{2g_m r_{op}} v_o - v_s\right)\frac{1}{r_{on}} = 0 \text{ or}$$

$$v_o\left(\frac{1}{2r_{op}} + \frac{1}{2g_m r_{op} r_{on}}\right) + g_m\left(1 + \frac{1}{g_m r_{on}}\right)v_s = g_m \frac{v_{id}}{2}$$

$$\frac{1}{r_o} << g_m \Rightarrow \frac{1}{r_o g_m} << 1$$

$$\therefore \frac{v_o}{2r_{op}} + g_m v_s = g_m \frac{v_{id}}{2} \qquad (1)$$

At node 1

$$i_1 + g_m v_{gs2} + (v_o - v_s)/r_{on} = 0$$

$$\therefore v_o\left(\frac{1}{2r_{op}} + \frac{1}{r_{on}}\right) - g_m\left(1 + \frac{1}{g_m r_{on}}\right)v_s = g_m \frac{v_{id}}{2} \text{ or}$$

$$v_o\left(\frac{1}{2r_{op}} + \frac{1}{r_{on}}\right) - g_m v_s = g_m \frac{v_{id}}{2} \qquad (2)$$

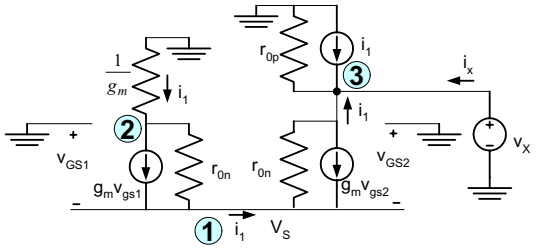
Adding equations (1) and (2)

$$\frac{v_o}{2r_{op}} + v_o\left(\frac{1}{2r_{op}} + \frac{1}{r_{on}}\right) = g_m v_{id}$$

$$v_o\left(\frac{1}{r_{op}} + \frac{1}{r_{on}}\right) = g_m v_{id}$$

$$\therefore A_v = \frac{v_o}{v_{id}} = g_m\left(\frac{1}{\frac{1}{r_{op}} + \frac{1}{r_{on}}}\right) = g_m\left(r_{op} \| r_{on}\right)$$

Output Resistance



Now $v_{gs1} = v_{gs2} = -v_s$

At node 3 $i_1 + i_1 + i_x - v_x/r_{op} = 0$

$2i_1 + i_x - v_x/r_{op} = 0 \qquad (1)$

At node 2

$v_2 = -\frac{1}{g_m} i_1$

$i_1 - g_m v_{gs1} + (v_2 - v_s)/r_{on} = 0$

$i_1 - g_m(-v_s) + (-\frac{1}{g_m} i_1 - v_s)/r_{on} = 0$

$i_1\left(1 + \frac{1}{g_m r_{on}}\right) + g_m\left(1 + \frac{1}{g_m r_{on}}\right) v_s = 0$

$\therefore i_1 = -g_m v_s$

At node 1

$i_1 + g_m v_{gs2} - (v_s - v_x)/r_{on} = 0$

$i_1 - g_m\left(1 + \frac{1}{g_m r_{on}}\right) v_s + \frac{v_x}{r_{on}} = 0$ since $v_{gs2} = -v_s$

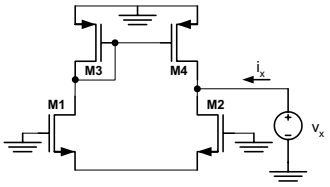
$i_1 - g_m v_s + \frac{v_x}{r_{on}} = 0 \Rightarrow i_1 + i_1 + \frac{v_x}{r_{on}} = 0 \Rightarrow 2i_1 = -\frac{v_x}{r_{on}}$

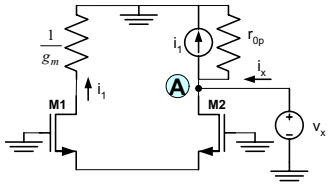
Substitute in equation 1

$-\frac{v_x}{r_{on}} + i_x - \frac{v_x}{r_{op}} = 0 \Rightarrow \left(\frac{1}{r_{on}} + \frac{1}{r_{op}}\right) v_x = i_x$

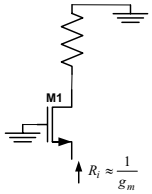
$\therefore R_o = r_{on} \| r_{op}$

Simplified analysis for R_o



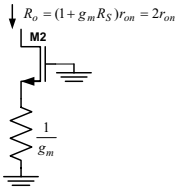


Current through $r_{op} = v_x/r_{op}$



Consider M1

$R_i \approx \frac{1}{g_m}$ since $R_L = \frac{1}{g_m}$ is small



Consider M2

So current through M2 is $\frac{v_x}{2r_{on}}$ which flows into M1 and $1/g_m$ and therefore $i_1 = \frac{v_x}{2r_{on}}$.

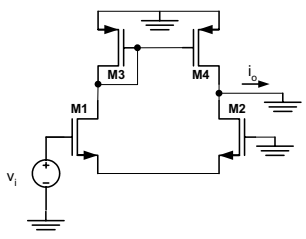
At node A then:

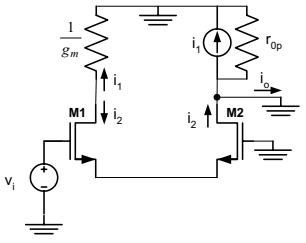
$i_x - \frac{v_x}{2r_{on}} - \frac{v_x}{2r_{on}} - \frac{v_x}{r_{op}} = 0$

$\left(\frac{1}{r_{on}} + \frac{1}{r_{op}}\right) v_x = i_x$

$\Rightarrow R_o = r_{on} \| r_{op}$

Simplified analysis for G_m





$i_1 = -i_2$

The gain of a SF is $\frac{g_m R_S}{1 + g_m R_S}$

With $R_S = \frac{1}{g_m}$

$\Rightarrow v_s = \frac{1}{1+1} v_i = \frac{1}{2} v_i$

$v_{gs1} = v_i - \frac{1}{2} v_i = \frac{1}{2} v_i$ and

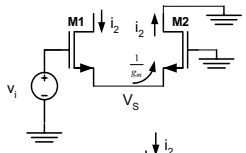
$i_2 = g_m v_{gs1} = \frac{g_m}{2} v_i$

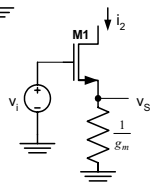
at the output we have

$i_o = i_2 - i_1 = i_2 - (-i_2) = 2i_2$

$i_o = 2\frac{g_m}{2} v_i = g_m v_i$

$\Rightarrow G_m = \frac{i_o}{v_i} = g_m$



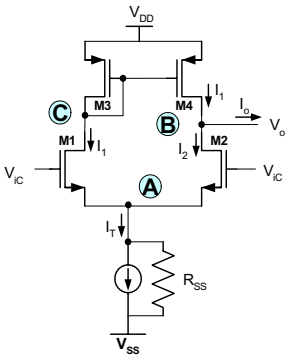


Remark

The small-signal gain $A_v = G_m R_o$ for a non-inverting amplifier

$\Rightarrow A_v = g_m(r_{on} \| r_{op})$

Common-mode Rejection

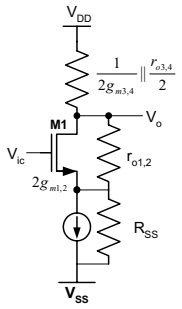


Assume all transistors are matched:
M1 with M2, M3 with M4

Increase $V_{ic} \Rightarrow V_A$ increases
This causes I_T to increase because of current through R_{SS}
Therefore I_1 and I_2 both increase but remain equal
Thus $I_o = 0 \Rightarrow V_o$ does not change

Can short B and C since $V_o = V_C$.

The equivalent circuit becomes



$$A_{CM} \approx \frac{-1}{2g_{m3,4}} \| \frac{r_{o3,4}}{2} \left(\frac{2g_{m1,2}}{1+2g_{m1,2}R_{SS}} \right) \text{neglecting } r_{o1,2}$$

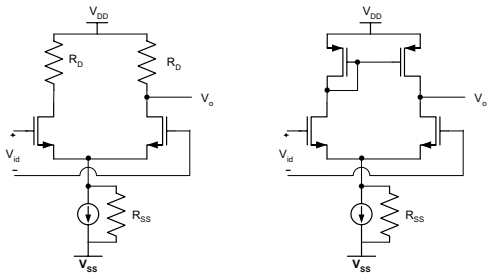
$$A_{CM} \approx \frac{-1}{g_{m3,4}} \frac{g_{m1,2}}{\left(1+2g_{m1,2}R_{SS}\right)} \text{ since } r_{o3,4} >> \frac{1}{g_{m3,4}}$$

$$A_{CM} \approx \frac{-1}{2R_{SS}g_{m3,4}}$$

$$\therefore CMRR \approx \frac{g_{mn}}{g_{op}+g_{on}} 2R_{SS}g_{mp}$$

The circuit is very insensitive to input common mode changes ⇒ CMRR is very high

Summary of differential to single-ended circuits



Parameter	Circuit A	Circuit B
G_m	$\frac{g_m}{2}$	g_m
R_o	$R_L \| r_{on}$	$r_{op} \| r_{on}$
A_v	$\frac{g_m}{2}(R_L \| r_{on})$	$g_m(r_{op} \| r_{on})$
CMRR	$1+2g_mR_{SS}$	$\frac{2R_{SS}g_{mp}g_{mn}}{g_{on}+g_{op}}$

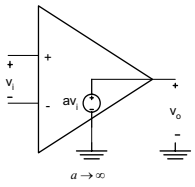
Remarks

- Effective G_m in circuit B is twice that of circuit A because of the current mirror active load
- The CMRR of circuit B is much superior to that of circuit A
- Circuit B delivers much higher voltage gain than circuit A
- Circuit B has a much higher R_o than circuit A

Operational Amplifiers

Ideal Opamp

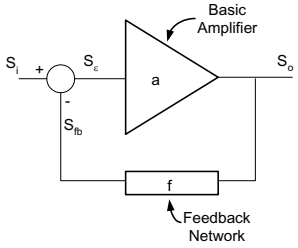
Differential input
Single-ended output
Infinite gain
Infinite input resistance
Zero output resistance



Applications of Op amps

Inverting, non-inverting amplifiers
Voltage follower
Differential amplifier
Nonlinear analog operations
Log, exponential, limiting, rectification, square rooting
Integrator, Differentiator
Switched-capacitor integrator

Basic Feedback Concepts



Gain of the system in absence of feedback in called open-loop gain: a of the amplifier

With the feedback the gain is closed-loop gain
f is usually < 1

The block diagram is that of negative feedback

$$S_o = aS_\varepsilon = a(S_i - S_{fb}); \quad S_{fb} = fS_o$$

$$S_o = a(S_i - fS_o)$$

$$\Rightarrow \frac{S_o}{S_i} = \frac{a}{1+af} \quad \leftarrow \text{ closed - loop gain}$$

T = af is called the loop gain

$$\lim_{af \to \infty} \frac{a}{1+af} = \frac{1}{f}$$

Remark

The closed-loop gain is independent of any variations in a. f is typically composed of passive elements.

Inverting amplifier

At node 1 $\quad I_1 - I_2 = 0$

$$\frac{V_S - V_i}{R_1} - \frac{V_i - V_o}{R_2} = 0$$

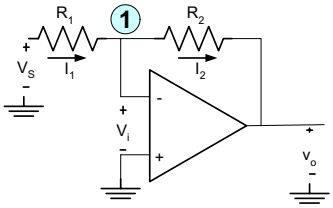
$$\frac{V_S}{R_1} + \frac{V_o}{R_2} - \left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_i = 0$$

Since $V_o = -aV_i \Rightarrow V_i = \frac{-1}{a} V_o$

$$\frac{V_S}{R_1} + \frac{V_o}{R_2} + \frac{1}{a}\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_o = 0$$

$$V_o \left[\frac{1}{R_2} + \frac{1}{aR_1} + \frac{1}{aR_2} \right] = -\frac{V_S}{R_1}$$

$$\frac{V_o}{V_S} = -\frac{R_2}{R_1} \frac{1}{1+\frac{1}{a}\left(1+\frac{R_2}{R_1}\right)}$$



If a is large enough so that

$$\frac{1}{a}\left(1+\frac{R_2}{R_1}\right) << 1 \quad \text{then}$$

$$\frac{V_o}{V_S} \approx -\frac{R_2}{R_1}$$

Remarks

- Closed-loop gain depends only on external passive components R_1 and R_2
- If a were to change from 5×10^4 to 10^5, this 100% increase in gain would have no observable effect on closed-loop performance. Performance independent of variations in a.

Summing-Point Constraints

Negative feedback circuit, stable operating point
Gain of opamp is large

$$V_i = \frac{V_o}{a} \to 0 \qquad \text{for large a}$$

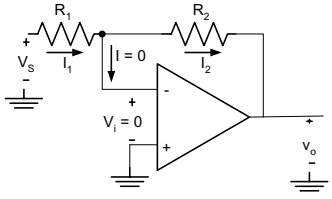
$V_i = 0$ is a summing-point constraint. Since $V_i = 0$, no voltage exists across the input resistance of opamp $\Rightarrow$ no current flows into the opamp input terminals.

Revisit inverting amplifier

$$I_1 = \frac{V_S}{R_1}; \quad I_1 = I_2$$

$$\therefore V_o = -R_2 I_2 = -R_2 I_1 = -\frac{R_2}{R_1} V_S$$

$$\Rightarrow \frac{V_o}{V_S} = -\frac{R_2}{R_1}$$

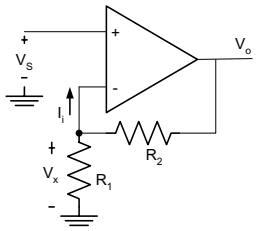


Non-inverting amplifier

$$V_x = V_o\left(\frac{R_1}{R_1+R_2}\right) \quad \text{since } I_i = 0$$

$$V_s = V_x = V_o\left(\frac{R_1}{R_1+R_2}\right) \quad \text{since } V_i = 0$$

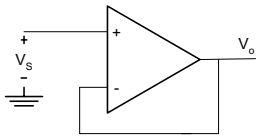
$$\therefore \frac{V_o}{V_S} = 1 + \frac{R_2}{R_1}$$



Remark

Common-mode input voltage = V_S.

Voltage Follower



$$\frac{V_o}{V_S} = 1 \quad \text{non - inverting amp with } R_2 = 0,\ R_1 = \infty$$

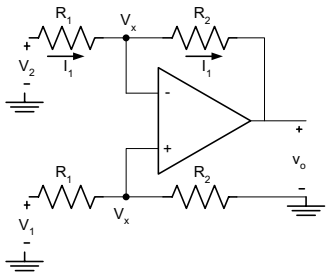
Differential Amplifier

$$V_x = V_1\left(\frac{R_2}{R_1+R_2}\right) \quad \text{since } I_i = 0$$

$$V_o = V_x - I_1 R_2$$

$$I_1 = \frac{V_2 - V_x}{R_1}$$

$$V_o = V_x - \frac{R_2}{R_1}(V_2 - V_x)$$



$$V_o = V_x\left(1+\frac{R_2}{R_1}\right) - \frac{R_2}{R_1}V_2 = \frac{R_2+R_1}{R_1}V_x - \frac{R_2}{R_1}V_2$$

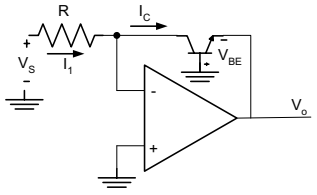
$$V_o = \frac{R_2+R_1}{R_1}\left(\frac{R_2}{R_1+R_2}\right)V_1 - \frac{R_2}{R_1}V_2 = \frac{R_2}{R_1}(V_1 - V_2)$$

Logarithmic Amplifier

$$I_1 = \frac{V_S}{R} = I_C = I_S e^{V_{be}/V_T}$$

$$V_{be} = V_T \ln\frac{I_C}{I_S} = V_T \ln\frac{V_S}{I_S R}$$

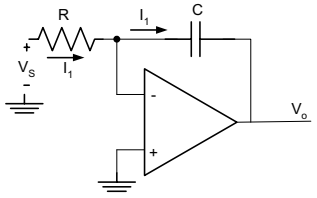
$$\Rightarrow V_o = -V_{be} = -V_T \ln\frac{V_S}{I_S R}$$



Integrator/Differentiator

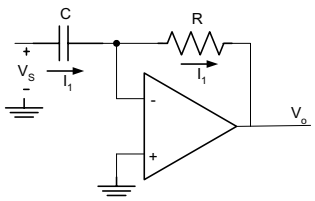
$$I_1 = \frac{V_S}{R} = -C\frac{dV_o}{dt}$$

$$\therefore V_o = -\frac{1}{RC}\int_0^t V_s(t)dt + V_o(0)$$



$$I_1 = C\frac{dV_S}{dt}$$

$$V_o = -I_1 R = -RC\frac{dV_S}{dt}$$

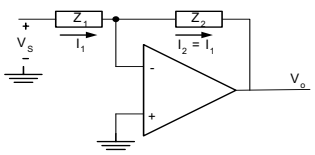


General Impedances (s-domain)

$$I_1 = \frac{V_S}{Z_1} \Rightarrow = V_o = -I_2 Z_2$$

$$V_o = -\frac{Z_2}{Z_1}V_S$$

$$\frac{V_o}{V_S} = -\frac{Z_2}{Z_1}$$



Deviations from ideality in real opamps

1) Finite gain
Gain is high and can use summing-point constraints in a feedback configuration

2) Input bias current
Not of significance in MOS opamps

3) Input offset current
Not in MOS opamps

4) Input offset voltage
Due to process variations. Places a lower limit on the magnitude of the dc voltage which can be accurately amplified

5) Common-mode rejection ratio

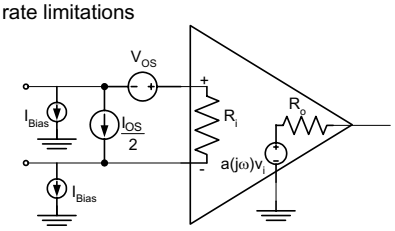
$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right|$$

6) Input Resistance
$R_{in} = \infty$ for MOSFET inputs
Even otherwise has little effect on circuit performance in closed-loop configurations

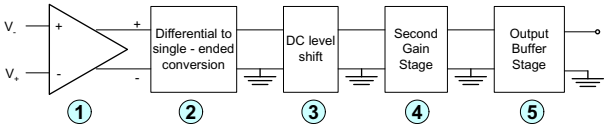
7) Output Resistance
Typically 40-100Ω. Affects stability under large capacitive loading

8) ac and transient behavior

Unity gain bandwidth ~1 to 100 MHz
Compensation to ensure circuit does not oscillate
Slew rate limitations



CMOS Opamps



1 – amplify voltage differences between the input terminals, independent of their common-mode voltage
2 – convert differential signal into single-ended
3 – dc level shift to properly bias the second gain stage
4 – second gain stage for additional gain
5 – output stage required for driving heavy resistive loads and large off-chip capacitances

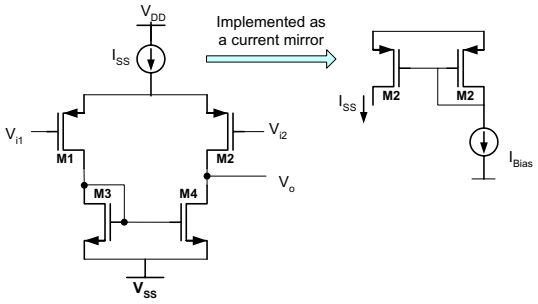
MOS opamps are typically used for on-chip applications where they drive small capacitive loads
⇒ Output stage is not necessary

Input Differential Amplifier

n-channel or p-channel
In n-well technologies (where p-channel transistors are in a well) p-channel stages are used to reduce power-supply coupling. Source and bulk are tied together.

Differential to single-ended conversion

A current mirror active load provides this function. This functional block can be implemented in the first stage itself



Note: $V_{DS4} = V_{GS3}$
This can be shown by taking I_{D3} and I_{D4} and setting them both equal to $I_{SS}/2$

$$I_{D3} = \frac{1}{2}K'\frac{W}{L}(V_{GS3} - V_T)^2(1 + \lambda V_{GS3}) = \frac{I_{SS}}{2}$$

$$I_{D4} = \frac{1}{2}K'\frac{W}{L}(V_{GS3} - V_T)^2(1 + \lambda V_{DS4}) = \frac{I_{SS}}{2}$$

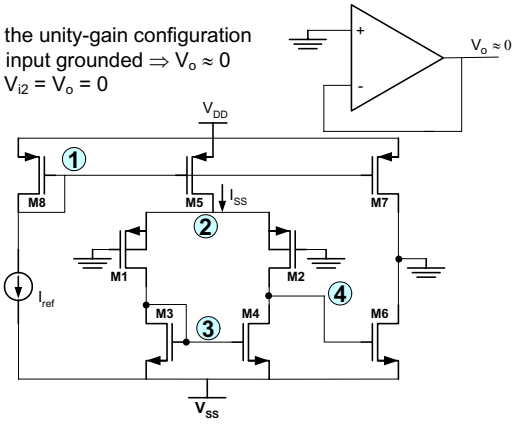
$$\therefore V_{GS3} = V_{DS4}$$

DC Analysis of the CMOS Two-Stage Opamp

Assumption

The opamp is within a feedback loop that forces the output to some specified voltage, usually zero. Because of the large gain, if this assumption is not made, output would be at V_{DD} or V_{SS}. Example: 0.1mV V_{OS} and a gain of $10^5 \Rightarrow V_o = 10$ V!

We take the unity-gain configuration with one input grounded ⇒ $V_o \approx 0$
i.e. $V_{i1} = V_{i2} = V_o = 0$



$$I_{D8} = I_{ref}$$

$$\therefore I_{SS} = I_{ref}\left(\frac{W}{L}\right)_5 \Big/ \left(\frac{W}{L}\right)_8 ; \qquad I_{D7} = I_{ref}\left(\frac{W}{L}\right)_7 \Big/ \left(\frac{W}{L}\right)_8$$

$$I_{D1} = I_{D2} = \frac{I_{ss}}{2} = I_{D3} = I_{D4}$$

$$Since \quad V_4 = V_{SS} + V_{DS4} = V_{SS} + V_{GS3}$$

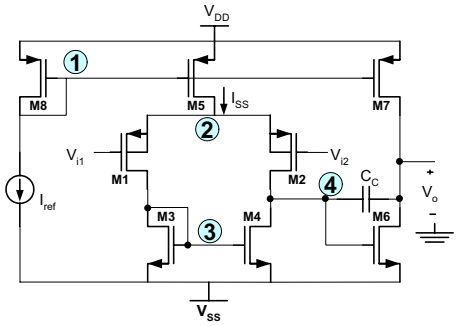
$$V_4 = V_{SS} + V_{Tn} + \sqrt{\frac{I_{SS}}{K'\left(\frac{W}{L}\right)_3}}$$

(ignoring channel-length modulation)

The first-stage output is one V_{GS} above V_{SS}. The next stage must shift the dc level toward the positive supply voltage

Level shifting can be done by a p-channel source follower or by using an n-channel MOSFET as a common-source amplifier. An n-channel CS amplifier provides level shifting and added gain in a single stage. A p-channel current mirror is used to maximize second-stage gain.

Complete Topology



C_C – compensation capacitor to ensure feedback amplifier is stable

Also $I_{D7} = I_{D6}$ since I_o=0

Calculation of Node Voltages

$$\text{Node 1}: V_1 = V_{DD} - |V_{GS8}|$$

$$|V_{GS8}| = |V_{TP}| + \sqrt{\frac{2I_{ref}}{K'_P \left(W/L\right)_8}}$$

$$\therefore V_1 = V_{DD} - |V_{TP}| - \sqrt{\frac{2I_{ref}}{K'_P \left(W/L\right)_8}}$$

$$\text{Node 2}: V_2 = |V_{GS1,2}| \quad \text{M1 \& M2 identical}$$

$$V_2 = |V_{TP}| + \sqrt{\frac{2\,I_{D5}/2}{K'_P \left(W/L\right)_{1,2}}}$$

$$\text{Node 3}: V_3 = V_{SS} + V_{GS3,4}$$

$$V_3 = V_{SS} + V_{Tn} + \sqrt{\frac{2\,I_{D5}/2}{K'_N \left(W/L\right)_{3,4}}}$$

$$\text{Node 4}: V_4 = V_{SS} + V_{Tn} + \sqrt{\frac{2I_{D7}}{K'_N \left(W/L\right)_6}}$$

To avoid creating a systematic offset voltage we must impose the constraint

$$V_{D1} = V_{D2} \Rightarrow V_3 = V_4$$

$$\therefore \frac{I_{D5}/2}{\left(W/L\right)_{3,4}} = \frac{I_{D7}}{\left(W/L\right)_6}$$

But current in M5 and M7 are also related as

$$\frac{I_{D7}}{I_{D5}} = \frac{\left(W/L\right)_7}{\left(W/L\right)_5} = \frac{\left(W/L\right)_6}{2\left(W/L\right)_{3,4}}$$

More on Systematic Offset Voltage

Recall

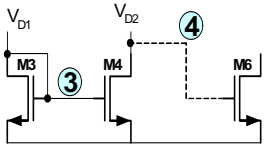
The input offset voltage V_{OS} is the differential input voltage for an output voltage of 0V. It has two components

1) A systematic offset due to improper transistor sizing and/or bias conditions
2) A random offset which is due to random parameter variations in the IC fabrication process

For the 2 stage CMOS opamp if the inputs are grounded and we also require $V_o = 0$ then $I_{D7} = I_{D6}$ and $V_{D1} = V_{D2}$ or $V_3 = V_4$

Which gave us the condition

$$\frac{\left(W/L\right)_3}{\left(W/L\right)_6} = \frac{\left(W/L\right)_4}{\left(W/L\right)_6} = \underbrace{\frac{1}{2}\frac{\left(W/L\right)_5}{\left(W/L\right)_7}}$$



Remark

To minimize the effects of random process-induced channel-length variations on the matching of the devices, and thus the random offset, the channel lengths of M3, M4 and M6 must be identical. The current ratios must be provided by a proper choice of channel widths. As usual there are tradeoffs involved.

Common-mode input range

For $V_{id} = 0$, it is the difference between the highest dc common-mode input voltage $V_{ic\text{-}max}$ and the lowest dc common-mode input voltage $V_{ic\text{-}min}$ such that all devices remain in their constant current regions (saturation region).

$V_{ic\text{-}max}$

As V_{ic} is increased, $|V_{DS5}|$ decreases and M5 will enter non-saturation.

$$|V_{DS5}| = V_{DD} - \left(V_{ic} + |V_{GS1}|\right)$$

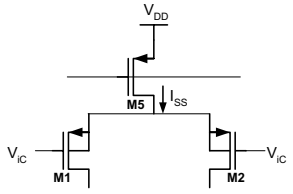
For M5 at the edge of saturation

$$|V_{DS5}| = |V_{GS5}| - |V_{TP}|$$

But $|V_{GS5}| = |V_{GS8}| = |V_{TP}| + \sqrt{\frac{2I_{ref}}{K'_P \left(W/L\right)_8}}$

$$V_{DD} - \left(V_{ic-\max} + |V_{GS1}|\right) = |V_{GS5}| - |V_{TP}|$$

$$\Rightarrow V_{ic-\max} = V_{DD} + |V_{TP}| - |V_{GS5}| - |V_{GS1}|$$



Remarks

- For $V_{ic\text{-}max}$ to be close to V_{DD}, reduce $|V_{GS5}|$ and $|V_{GS1}|$ i.e. increase W/L
- In the limit $|V_{GS5}| \approx |V_{TP}| + \Delta \approx |V_{GS1}|$
  $\therefore V_{ic-\max} \to V_{DD} - |V_{TP}| - 2\Delta$

$V_{ic\text{-}min}$

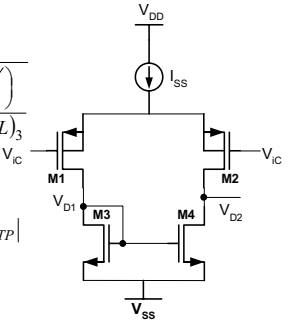
Ensure M1, M2 are in saturation

$$V_{D1} = V_{SS} + V_{GS3} = V_{SS} + V_{TN} + \sqrt{\frac{2\left(I_{SS}/2\right)}{K'_N \left(W/L\right)_3}}$$

$$|V_{DS1}| = V_{S1} - V_{D1}$$

$$V_{S1} = V_{ic} + |V_{GS1}|$$

$$\therefore |V_{DS1}| = V_{ic-\min} + |V_{GS1}| - V_{D1} = |V_{GS1}| - |V_{TP}|$$



$$\therefore V_{ic-\min} = V_{D1} - |V_{TP}| = V_{SS} + |V_{GS3}| - |V_{TP}|$$

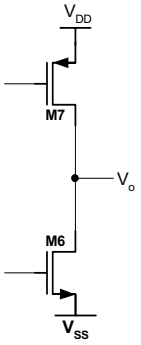
$$V_{ic-\min} = V_{SS} + V_{TN} + \sqrt{\frac{I_{SS}}{K'_N (W/L)_3}} - |V_{TP}|$$

Remark

- Increasing $\left(\frac{W}{L}\right)_{3,4}$ lowers $V_{ic\text{-}min}$ (i.e. improves)
- In the limit, $V_{ic\text{-}min} \approx V_{SS}$ if the n- and p-channel thresholds are equal

Output Voltage Range

M6 and M7 limit output range
M7 saturated for:



$$|V_{DS7}| = V_{DD} - V_o \geq |V_{GS7}| - |V_{TP}|$$

i.e. $V_{o-\max} = V_{DD} - |V_{GS7}| + |V_{TP}|$

$$V_{o-\max} = V_{DD} - \sqrt{\frac{2I_{D7}}{K'_P (W/L)_7}}$$

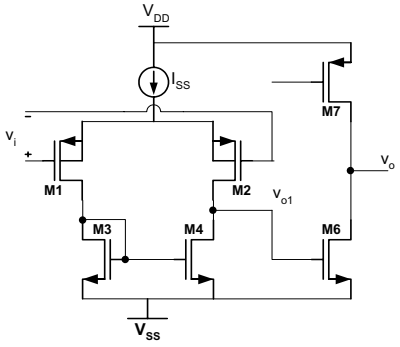
M6 saturated for:

$$V_{DS6} = V_o - V_{SS} \geq V_{GS6} - V_{TN}$$

$$V_{o-\min} = V_{SS} + \sqrt{\frac{2I_{D7}}{K'_N (W/L)_6}}$$

DC (low-frequency) Gain

Since the MOSFET has an infinite input resistance consider the 2 stages separately



$$\frac{v_{o1}}{v_i} = g_{m1}(r_{o2} \parallel r_{o4}) = \frac{g_{m1}}{g_{o2} + g_{o4}}$$

$$\frac{v_o}{v_{o1}} = -g_{m6}(r_{o6} \parallel r_{o7}) = \frac{-g_{m6}}{g_{o6} + g_{o7}}$$

$$\therefore \text{Overall gain } A_v = \frac{v_o}{v_i} = \frac{v_o}{v_{o1}} \times \frac{v_{o1}}{v_i} = \frac{-g_{m6} g_{m1}}{(g_{o6} + g_{o7})(g_{o2} + g_{o4})}$$

Remark
The overall gain is related to $(g_m r_o)^2$.

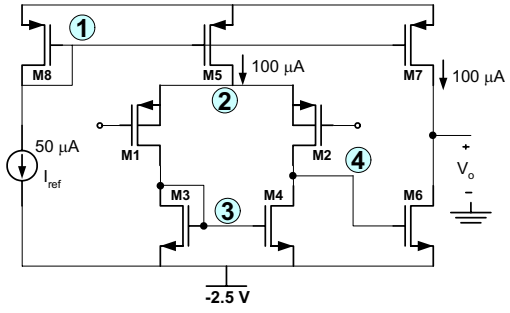
Design Example of 2-Stage Opamp

Specifications
V_{DD} = 2.5 V, V_{SS} = -2.5 V. Total power dissipation = 1.25 mW
Area constraints and high r_o requirement
$\Rightarrow W_{max}$ = 150µ, L_{min} = 3µ

$$\left(\frac{W}{L}\right)_{\max} = \frac{150\mu}{3\mu} = 50$$

Need large g_m for improved bandwidth, as we shall see later.

Small V_{GS} - V_T for high common-mode input and output ranges
$\Rightarrow$ Large W/L for the signal path



Power constraint $\Rightarrow$ bias current add to $\frac{1.25mW}{2.5V - (-2.5)V} = 250\mu A$

Bias first and second stages at 100 µA each $\Rightarrow I_{ref}$ = 50µA

$$V_{DS6} = V_o - V_{SS} \geq V_{GS6} - V_{TN}$$

$$g_m = \sqrt{2K' I_D W/L}$$

For large g_m and small V_{GS} - V_T

$$\left(W/L\right)_6 = \left(W/L\right)_7 = \frac{150}{3} = 50 = \left(W/L\right)_1 = \left(W/L\right)_2$$

Also $\left(W/L\right)_5 = \left(W/L\right)_7$ since $I_{Bias} = 100\mu A$

Choose $\left(W/L\right)_3$ and $\left(W/L\right)_4$ to avoid systematic offset voltage

$$\frac{\left(W/L\right)_3}{\left(W/L\right)_6} == \frac{1}{2}\frac{\left(W/L\right)_5}{\left(W/L\right)_7} = \frac{1}{2}$$

$$\therefore \left(W/L\right)_3 = \left(W/L\right)_4 = \frac{1}{2}\left(W/L\right)_6 = \frac{1}{2}\frac{150}{3} = 25$$

Note
We are keeping L's identical for matching

$$\left(W/L\right)_8 = \frac{1}{2}\left(W/L\right)_5 = 25$$

DC operating point
This will be computed with V_{i1}= V_{i2} = 0 and V_o = 0, assuming a feedback arrangement.

Transistor data
n-channel: V_T = 0.7 V, λ = 0.09/L µ/V, K' = 50 µA/V^2
p-channel: V_T = -0.7 V, λ = 0.09/L µ/V, K' = 25 µA/V^2

$$\text{Node1: } |V_{GS8}| = |V_{TP}| + \sqrt{\frac{2I_{D8}}{K'_P (W/L)_8}} = 1.1V$$

$$\therefore V_{D1} = V_{DD} - |V_{GS8}| = 2.5 - 1.1 = 1.4\text{V}$$

$$\text{Node2: } |V_{GS2}| = |V_{TP}| + \sqrt{\frac{2I_{D2}}{K'_P (W/L)_2}} = 0.7 + \sqrt{\frac{2 \times 50\mu}{25\mu \times 50}} = 0.98V$$

$$\therefore V_2 = 0.98\text{V}$$

$$\text{Node3}: V_{GS3} = 0.7 + \sqrt{\frac{2\times 50\mu}{50\mu\times 25}} = 0.98V$$

$$\therefore V_3 = -2.5 + 0.98 = \text{-}1.52\text{V}$$

$$\text{Node4}: V_{GS6} = 0.7 + \sqrt{\frac{2\times 100\mu}{50\mu\times 50}} = 0.98V$$

$$\therefore V_4 = -2.5 + 0.98 = \text{-}1.52\text{V}$$

Operating point check
All devices should be in saturation for the circuit to work properly. Use SPICE to check individual transistors by hand.

Calculation of input common-mode range

$$V_{ic-\max} = V_{DD} + |V_{TP}| - |V_{GS5}| - |V_{GS1}|$$

$$|V_{GS5}| = 0.7 + \sqrt{\frac{2\times 100\mu}{25\mu\times 50}} = 1.1V$$

$$\therefore V_{ic-\max} = 2.5 + 0.7 - 1.1 - 0.98 = 1.12\text{V}$$

$$V_{ic-\min} = V_{SS} + V_{GS3} - |V_{TP}| = -2.5 + 0.98 - 0.7 = \text{-}2.22\text{V}$$

Remark
V_{icm} is asymmetrical. To increase V_{icmax} need to reduce $|V_{GS5}|$ and $|V_{GS1}| \Rightarrow$ M1, M2 and M7 should be made wider or the length reduced. Both violate given constraints!

Output voltage range

$$V_{o-\max} = V_{DD} + |V_{TP}| - |V_{GS7}| = 2.5 - 0.4 = 2.1\text{V}$$

$$V_{o-\min} = V_{SS} + \sqrt{\frac{2I_{D7}}{K'_N (W/L)_6}} = -2.5 + 0.28 = -2.22V$$

Small signal quantities

$$g_{m1} = g_{m2} = \sqrt{2I_{D1,2}K'_P (W/L)_{1,2}} = \sqrt{2\times 50\mu\times 25\mu(50)} = 353.5\mu A/V$$

$$g_{m6} = \sqrt{2I_{D7}K'_N (W/L)_6} = \sqrt{2\times 100\mu\times 50\mu(50)} = 707\mu A/V$$

$$r_{02} = \frac{1}{\lambda_P I_{D1}} = \frac{1}{0.03\times 50\mu} = 666.7K\Omega$$

$$r_{04} = \frac{1}{\lambda_N I_{D2}} = r_{02} = 666.7K\Omega$$

$$r_{06} = \frac{1}{\lambda_P I_{D7}} = \frac{1}{0.03\times 100\mu} = 333.3K\Omega$$

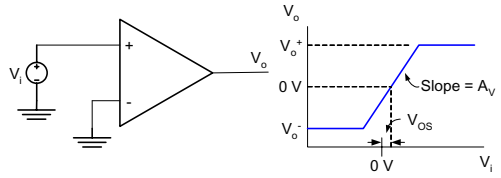
$$\therefore A_v = \frac{g_{m1}}{g_{o2}+g_{o4}}\frac{g_{m6}}{g_{o6}+g_{o7}} = 353.5\mu(666.7K \,\|\, 666.7K)707\mu(333K \,\|\, 333K)$$

$$A_v = 140{,}000$$

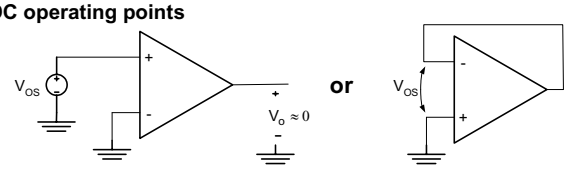
$$R_o = r_{o6} \,\|\, r_{o7} = 166.7K\Omega$$

SPICE simulations

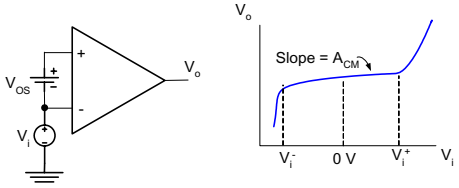
V_{OS} and open-loop gain



DC operating points



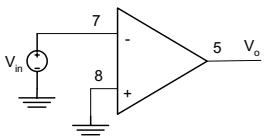
Input common-mode range and A_{cm}



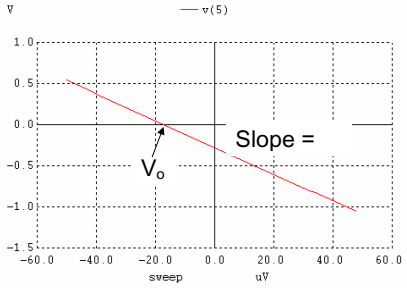
Could also use a .TF command for A_{cm}

SPICE file for measuring V_{os} and A_{dm}

```
* Two-stage op-amp

*inputs: inverting node 7, noninverting node 8

*Power supplies
VDD 10 0 2.5
Vss 20 0 -2.5

*Current mirror
M8 1 1 10 10 CMOSP L=3u W=75u
Iref 1 20 50.0uA

*Differential amp
*ISS
M5 2 1 10 10 CMOSP L=3u W=150u

*Drivers
M1 3 7 2 2 CMOSP L=3u W=150u
M2 4 8 2 2 CMOSP L=3u W=150u

*Active loads
M3 3 3 20 20 CMOSN L=3u W=75u
M4 4 3 20 20 CMOSN L=3u W=75u

*2nd stage
M7 5 1 10 10 CMOSP L=3u W=150u
M6 5 4 20 20 CMOSN L=3u W=150u

.MODEL CMOSN NMOS( LEVEL=1 KP=50u VTO=0.7 LAMBDA=0.03)
.MODEL CMOSP PMOS( LEVEL=1 KP=25u VTO=-0.7 LAMBDA=0.03)
```



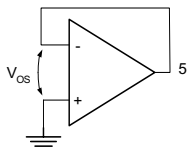

```
vin 7 0 0
vinp 8 0 0

.control
dc vin -50u 50u 2u
reset
run
plot v(5)
.endc

.end
```



V_{OS} = 17.5 uV
A_{dm} ~1.6V/100uV =

SPICE file for measuring V_{os}

```
* Two-stage op-amp

*inputs: inverting node 7, noninverting node 8

*Power supplies
VDD 10 0 2.5
Vss 20 0 -2.5

*Current mirror
M8 1 1 10 10 CMOSP L=3u W=75u
Iref 1 20 50.0uA

*Differential amp
*ISS
M5 2 1 10 10 CMOSP L=3u W=150u

*Drivers
*unity gain feedback: output(5) connected to inverting input
M1 3 5 2 2 CMOSP L=3u W=150u
M2 4 8 2 2 CMOSP L=3u W=150u

*Active loads
M3 3 3 20 20 CMOSN L=3u W=75u
M4 4 3 20 20 CMOSN L=3u W=75u

*2nd stage
M7 5 1 10 10 CMOSP L=3u W=150u
M6 5 4 20 20 CMOSN L=3u W=150u

.MODEL CMOSN NMOS( LEVEL=1 KP=50u VTO=0.7 LAMBDA=0.03)
.MODEL CMOSP PMOS( LEVEL=1 KP=25u VTO=-0.7 LAMBDA=0.03)
```



```
vin 8 0 0

.control
run
print all
.endc
.end
```

Output:

```
WinSpice 33 ->op
WinSpice 34 ->run
WinSpice 35 -> print all
v(1) = 1.406404e+00
v(2) = 9.745137e-01
v(3) = -1.51948e+00
v(4) = -1.52169e+00
v(5) = -1.72739e-05
v(8) = 0.000000e+00
v(10) = 2.500000e+00
v(20) = -2.50000e+00
vdd#branch = -2.55340e-04
vin#branch = 0.000000e+00
vss#branch = 2.553398e-04

WinSpice 36 -> show all

 Mos1: Level 1 MOSfet model with Meyer ca

device          m6       m4       m3
model        cmosn    cmosn    cmosn
      id  0.000104  5.06e-05  5.06e-05
      is -0.000104 -5.06e-05 -5.06e-05
      ig         0         0         0
      ib -9.67e-13 -3.78e-13 -3.79e-13
     vgs     0.978     0.981     0.981
     vds       2.5     0.978     0.981
     vbs         0         0         0
     von       0.7       0.7       0.7
   vdsat     0.278     0.281     0.281
      rs         0         0         0
      rd         0         0         0
      gm  0.000748  0.000361  0.000361
     gds   2.9e-06  1.48e-06  1.48e-06


 Mos1: Level 1 MOSfet model with Meyer ca
device          m5       m8
model        cmosp    cmosp
      id  0.000101    5e-05
      is -0.000101   -5e-05
      ig         0         0
      ib  -5.9e-13 -4.23e-13
     vgs      1.09      1.09
```

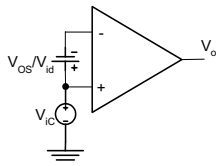
$|V_{ds}| > |V_{dsat}|$ for saturation


```
vds       1.53      1.09
vbs          0         0
von       -0.7      -0.7
vdsat   -0.394    -0.394
rs           0         0
rd           0         0
gm    0.000515  0.000254
gds    2.9e-06  1.45e-06
```

$|V_{ds}| > |V_{dsat}|$ for saturation

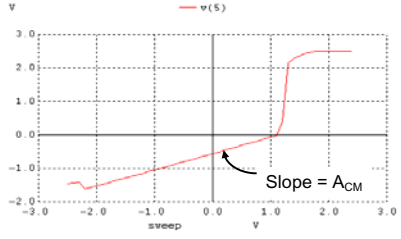
SPICE file for measuring input common-mode range and A_{cm}

```
* Two-stage op-amp
*inputs: inverting node 7, noninverting node 8

*Power supplies
VDD 10 0 2.5
Vss 20 0 -2.5

*Current mirror
M8 1 1 10 10 CMOSP L=3u W=75u
Iref 1 20 50.0uA

*Differential amp
*ISS
M5 2 1 10 10 CMOSP L=3u W=150u

*Drivers
M1 3 7 2 2 CMOSP L=3u W=150u
M2 4 8 2 2 CMOSP L=3u W=150u

*Active loads
M3 3 3 20 20 CMOSN L=3u W=75u
M4 4 3 20 20 CMOSN L=3u W=75u

*2nd stage
M7 5 1 10 10 CMOSP L=3u W=150u
M6 5 4 20 20 CMOSN L=3u W=150u


.MODEL CMOSN NMOS( LEVEL=1 KP=50u VTO=0.7 LAMBDA=0.03)
.MODEL CMOSP PMOS( LEVEL=1 KP=25u VTO=-0.7 LAMBDA=0.03)

vid 7 8 17.27u
vic 8 0 0

.control
tf v(5) vic
run
dc vic –2.5 2.5 .1
run
plot v(5)
dc vid -200u 200u 2u vic -2. 2. .5
run
plot v(5)
.endc
.end
```



Output:

```
WinSpice 1 -> tf v(5) vic
Transfer function analysis ...
WinSpice 2 -> print all
 transfer_function = 4.922230e-01   A_CM
output_impedance_at_v(5) = 1.694335e+05
vic#input_impedance = 1.000000e+20
WinSpice 3 -> tf v(5) vid
Transfer function analysis ...
WinSpice 4 -> print all
transfer_function = -1.61465e+04   A_DM
output_impedance_at_v(5) = 1.694335e+05   R_o
vid#input_impedance = 1.000000e+20
```



Acm ~1.6V/3.2V =

Frequency Response

Circuits operate at different frequencies

Example

- Audio amplifiers	20Hz-20KHz
- Telecommunication circuits	~ 200KHz
- Video Amplifiers	~ 50 MHz
- RF circuits	> 100MHz
- Cellular applications	1-2 GHz

So an understanding of how circuits operate over a frequency band is important.

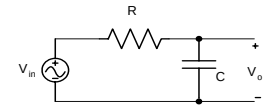
We will work with small input signals → small-signal analysis will be used extensively.

Input will be considered to be a sinusoid → phasor analysis and complex variables.

Goal

Find the amplitude and phase of an output signal given an input sinusoidal signal.

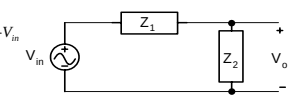
Low-pass Filter



$$\frac{V_o}{V_{in}} = \frac{1/j\omega C}{R + 1/j\omega C} = \frac{1}{1 + j\omega RC}$$

Use impedances: $Z_C = \frac{1}{j\omega C}$, $Z_R = R$

Voltage division $V_{out} = \frac{z_2}{z_1 + z_2} V_{in}$



Magnitude = $\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\sqrt{1+(\omega RC)^2}}$

Recall:

$$\frac{1}{a+jb} = \frac{1}{a+jb}\frac{a-jb}{a-jb} = \frac{a-jb}{b^2+b^2} \Rightarrow \angle\frac{1}{a+jb} = -\tan(b/a)$$

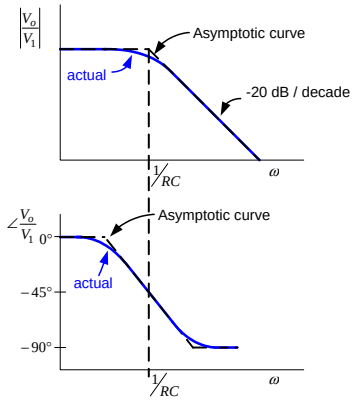
Phase = $\angle\frac{V_o}{V_{in}} = -\tan^{-1}(\omega RC)$

Observations

ωRc << 1 : $\left|\frac{Vo}{Vin}\right| \approx 1; \quad \angle\frac{Vo}{Vin} \approx -\tan^{-1} 0 = 0$

ωRc << 1 : $\left|\frac{Vo}{Vin}\right| \approx \frac{1}{\omega RC}; \quad \angle\frac{Vo}{Vin} \approx -\tan^{-1}\infty = -90^\circ$

Plot these quantities as a function of frequency (log).



Bode Plots

Transfer function $= T(j\omega) = |T(j\omega)| \angle T(j\omega)$

Magnitude: the plot of A = 20 log $|T(jw)|$ as a function of ω in log scale is the Bode plot for magnitude

Phase: the plot of $\theta = \angle T(j\omega)$ as a function of ω in log scale is the Bode plot for phase

Example

$T(j\omega) = 1 + \frac{j\omega}{z_1}$ ω = -z_1 is a zero

A(ω) = 20 log $\left|1+\frac{j\omega}{z_1}\right|$ = 20 log $\sqrt{1+\left(\frac{\omega}{z_1}\right)^2}$ = 10 log (1+ $\left(\frac{\omega}{z_1}\right)^2$)

ω << z_1 A(ω) = 10 log 1 = 0 dB

ω >> z_1 A(ω) = 10 log $\left(\frac{\omega}{z_1}\right)^2$ = 20 log $\frac{\omega}{z_1}$

ω = z_1 A(ω) = 10 log (1+1) = 10 log 2 = 3dB.

For frequency ω_2 = 2 ω_1 (ω_1, ω_2 >> z_1) change in A (ω) is

A (ω_2) – A (ω_1) = 20 log $\frac{2\omega_1}{z_1}$ - 20 log $\frac{\omega_1}{z_1}$ = 20 log 2 = 6 dB.

ω_2 = 2 ω_1 → frequency separation is an octave

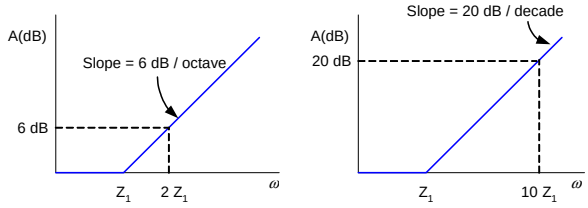
$\therefore$ slope = 6 dB/octave

Alternatively,

ω_2 = 10 ω_1 (ω_1, ω_2 >> z_1) then

A (ω_2) - A (ω_1) = 20 log $\frac{10\omega_1}{z_1}$ - 20 log $\frac{\omega_1}{z_1}$ = 20 log 10 = 20 dB

i.e. slope = 20 dB/decade because frequencies are separated by a decade



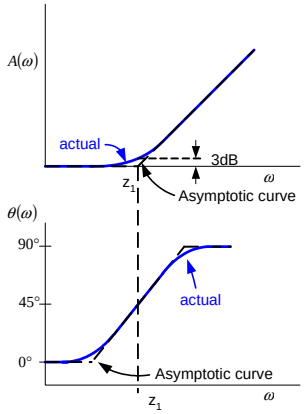
(ω in log scale)

The curves asymptotically approach a straight line

ω << z_1 θ (ω) ≅ $\tan^{-1}$ 0 = 0

ω = z_1 θ (ω) = $\tan^{-1}$ 1 = 45°

ω >> z_1 θ (ω) ≅ $\tan^{-1}\infty$ = 90°



The low pass filter was an example of

$T(j\omega) = \frac{1}{1+j\frac{\omega}{p_1}}$ i.e. a pole at p_1

$p_1 = \frac{1}{RC}$ Hz (RC has units of time)

Bode Plots of Arbitrary System Functions

$$T(j\omega) = \frac{Kj\omega\left(1+\frac{j\omega}{z_1}\right)\left(1+\frac{j\omega}{z_2}\right)\cdots\left(1+\frac{j\omega}{z_m}\right)}{\left(1+\frac{j\omega}{p_1}\right)\left(1+\frac{j\omega}{p_2}\right)\cdots\left(1+\frac{j\omega}{p_n}\right)}$$

$$A(\omega) = 20\log|T(j\omega)| = 20\log|K| + 20\log|j\omega| + 20\log\left|1+\frac{j\omega}{z_1}\right| + \ldots + 20\log\left|1+\frac{j\omega}{z_m}\right| - 20\log\left|1+\frac{j\omega}{p_1}\right| - \ldots - 20\log\left|1+\frac{j\omega}{p_n}\right|$$

$$\theta(\omega) = \underbrace{0^\circ \text{ or } 180^\circ}_{\text{sign of K}} + 90^\circ + \tan^{-1}\left(\frac{\omega}{z_1}\right) + \ldots + \tan^{-1}\left(\frac{\omega}{z_m}\right) - \tan^{-1}\left(\frac{\omega}{p_1}\right) - \ldots - \tan^{-1}\left(\frac{\omega}{p_n}\right)$$

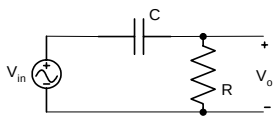
Remarks

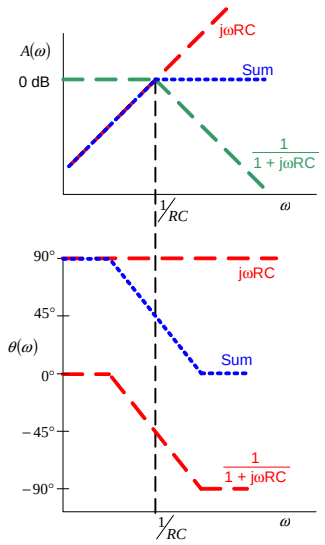
1) If K is negative then a phase angle of 180° is added.
2) Bode plot can be constructed by summing the magnitude and phase contributions of each pole & zero
3) Asymptotic plots are often sufficient

Example

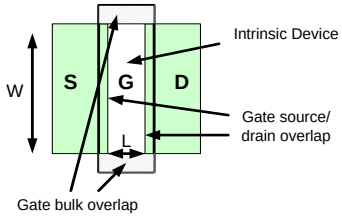
High-pass filter

$\frac{V_o}{V_{in}} = \frac{R}{R+\frac{1}{jwC}} = \frac{jwRC}{1+jwRC}$





MOSFET Capacitances



We will partition the FET into intrinsic and extrinsic parts. The intrinsic device is in the channel area only.

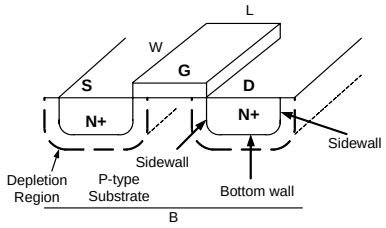
Extrinsic Capacitances

Overlap capacitances

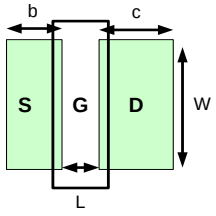
Due to overlap and fringing fields between gate and bulk, source or drain. Modeled in terms of constants C_{GS0}, C_{GD0} and C_{GB0}. A 0.5 µ process might have $C_{GS0} = C_{GD0} = 0.2$ fF/µ and $C_{GB0} = 0$.

$C_{GSov} = C_{GS0}$ x W $C_{GDov} = C_{GD0}$ x W $C_{GBov} = C_{GB0}$ x L

Junction capacitances



These are due to the S/B and D/B junction diodes. The junction diodes are always reversed biased for proper operation, but have an associated capacitance. Source and drain sizes are dependent on layout and therefore capacitances also depend on layout. A portion of the capacitance depends on area (bottom) and a portion on perimeter (sidewalls).



Area of source diffusion = AS = Wb (m^2)

Area of drain diffusion = AD = Wc (m^2)

Perimeter of source diffusion = PS = 2(W+b) (m)

Perimeter of drain diffusion = PD = 2(W+c) (m)

$$C_{bottom} = C_J = Area \frac{C_{j0}}{(1+\frac{V_J}{P_B})^{M_J}} \quad \text{where}$$

C_{j0} = CJ = zero bias junction capacitance per unit area (F/m^2)

P_B = PB = bulk built in potential (V)

M_J = MJ = bulk junction grading coefficient

V_J = applied reverse voltage (V)

$$C_{sidewall} = C_{SW} = Perimeter \frac{C_{jsw0}}{(1+\frac{V_J}{P_{BSW}})^{M_{JSW}}} \quad \text{where}$$

C_{jSW0} = CJSW = zero bias sidewall junction cap per unit area (F/m^2)

P_{BSW} = PBSW = bulk sidewall built in potential (V)

M_{JSW} = MJSW = bulk sidewall junction grading coefficient

$$C_J = C_{sidewall} + C_{bottom}$$

Example: N-channel MOSFET in 0.5µm CMOS process

CJ = 0.557 fF/µm^2, CJSW = 0.256 fF/µm, PB = PBSW = 0.99,

MJ = 0.6, MJSW = 0.1, W=50 µ, L = 1 µ, c = b = 2 µ

$C_{GS0} = C_{GD0} = 0.2$ fF/µ and $C_{GB0} = 0.1$ fF/µ

For $V_{DS} = 3$ V, $V_{SB} = 2$V $\Rightarrow$ $V_{DB} = 5$ V and $V_{SB} = 2$ V

$$C_{SB} = \frac{50\times2\times0.557\,fF}{(1+\frac{V_J}{P_B})^{M_J}} + \frac{2\times(50+2)\times0.256\,fF}{(1+\frac{V_J}{P_{BSW}})^{M_{JSW}}} = \frac{55.7\,fF}{(1+\frac{2}{0.99})^{0.6}} + \frac{26.6\,fF}{(1+\frac{2}{0.99})^{0.1}}$$

$$C_{SB} = 28.7 + 23.8 = 52.5\,fF$$

Since c = b, source and drain areas and perimeters are the same,

$$C_{DB} = \frac{55.7\,fF}{(1+\frac{V_J}{P_B})^{M_J}} + \frac{26.6\,fF}{(1+\frac{V_J}{P_{BSW}})^{M_{JSW}}} = \frac{55.7\,fF}{(1+\frac{5}{0.99})^{0.6}} + \frac{26.6\,fF}{(1+\frac{5}{0.99})^{0.1}} = 18.9 + 22.2 = 41.1\,fF$$

$C_{GSov} = C_{GDov} = 50\mu$ x 0.2 fF/µ = 10 fF

$C_{GBov} = 1\mu$ x 1 x 0.1 fF/µ = 0.1 fF

Intrinsic Capacitances

Cut off region

For $V_{GS} < V_T$, there is no conducting channel. Therefore intrinsic $C_{GS} = C_{GD} = 0$. Channel is at bulk potential and $C_{GB} = WLC_{ox}$.

Non-saturation region, small V_{DS}

Inversion layer in channel

Total capacitance between gate and channel = $WLC_{ox} = C_{GS} + C_{GD}$

The device is symmetrical so $C_{GS} = C_{GD} = ½\ WLC_{ox}$

Similarly, $C_{BS} = C_{BD}$ and equal ½ the total capacitance between inversion layer and bulk: $C_{BS} = C_{BD} = \eta(½\ WLC_{ox})$

$C_{GB} \approx 0$ since the inversion layer shields the gate from the body

Saturation region

Channel pinches off and V_{DS} has no effect on the channel charge

$\Rightarrow C_{GD} = 0$ and $C_{BD} = 0$

C_{GB} nonzero but can be ignored

$C_{GS} = \frac{2}{3} WLC_{ox}$ as will be shown next.

Derivation of C_{GS} in saturation

The charge per unit area in the channel was found to be

$$Q_I(y) = C_{ox}(V_{GS} - V_T - V(y))$$

The total charge in the channel is then

$$Q_{tot} = \int_0^L C_{ox} W (V_{GS} - V_T - V(y)) dy$$

We found before that $I_{DS} = \mu C_{ox} W (V_{GS} - V_T - V(y)) \frac{dV}{dy}$ or

$$dy = \frac{\mu C_{ox} W}{I_{DS}} (V_{GS} - V_T - V(y)) dV$$

Substituting, $Q_{tot} = \frac{\mu C_{ox}^2 W^2}{I_{DS}} \int_0^{V_{GS}-V_T} (V_{GS} - V_T - V(y))^2 dV$

$$Q_{tot} = \frac{\mu C_{ox}^2 W^2}{3 I_{DS}} \left\{ \left[(V_{GS} - V_T) - (V_{GS} - V_T) \right]^3 + (V_{GS} - V_T)^3 \right\}$$

$$Q_{tot} = \frac{\mu C_{ox}^2 W^2}{3 \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2} (V_{GS} - V_T)^3 = \frac{2 C_{ox} WL}{3} (V_{GS} - V_T)$$

$$C_{GS} = \frac{\partial Q_{tot}}{\partial V_{GS}} = \frac{2 C_{ox} WL}{3}$$

Summary of Intrinsic capacitances

Capacitance transitions smoothly from low V_{DS} in non-saturation to their values in non-saturation.

$$\boldsymbol{C_{GSi} = \frac{WLC_{ox}}{2} \left(1 + \frac{1}{3} \frac{V_{DS}}{V_{DSAT}} \right)}$$ non-saturation

$$\boldsymbol{C_{GSi} = \frac{2}{3} WLC_{ox}}$$ saturation

$$\boldsymbol{C_{GDi} = \frac{WLC_{ox}}{2} \left(1 - \left(\frac{V_{DS}}{V_{DSAT}} \right)^2 \right)}$$ non-saturation

$$\boldsymbol{C_{GDi} = 0}$$ saturation

$C_{GBi} \approx 0$ non-saturation and saturation

$$\boldsymbol{C_{BSi} = \eta \frac{WLC_{ox}}{2}}$$ non-saturation and saturation

$$\boldsymbol{C_{BDi} = \eta \frac{WLC_{ox}}{2} \left(1 - \frac{V_{DS}}{V_{DSAT}} \right)}$$ non-saturation

$$\boldsymbol{C_{BDi} = 0}$$ saturation

$C_{GBi} = WLC_{ox}$ cut-off region

$C_{GSi} = C_{GDi} = C_{BSi} = C_{DBi} = 0$ cut-off region

Example of intrinsic capacitance

$C_{ox} = 3.45$ fF/μ^2, ($T_{ox} = 10$nm) $V_{T0} = 0.7$ V, λ = 0, K' = 153 μA/V^2
γ = 0.7 V$^{0.5}$, Φ = 0.8 V, W = 10μ, L = 1μ
$V_{DS} = 3$ V, $V_{SB} = 2$V, $V_{GS} = 3$ V

$$V_T = 0.7 + 0.7\left(\sqrt{2 + 0.8} - \sqrt{0.8}\right) = 1.25V$$

$V_{GS} - V_T = 3 - 1.25 = 1.75$ V < V_{DS} = 3V $\Rightarrow$ saturation region
WLCox = 10 x 1 x 3.45fF = 34.5 fF

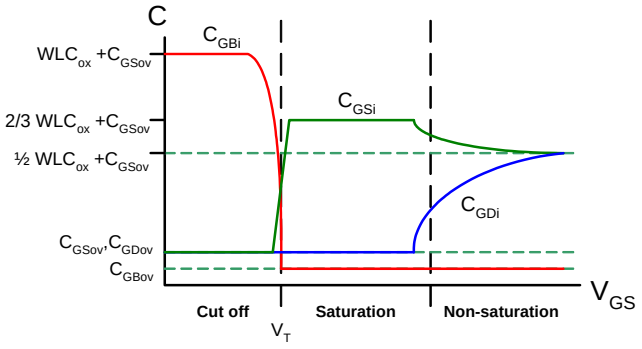
$$\boldsymbol{C_{GSi} = \frac{2}{3} WLC_{ox} = 23\,fF}$$

$$\boldsymbol{C_{BSi} = \eta \frac{WLC_{ox}}{2} = \frac{0.7}{2\sqrt{2.8}} \frac{34.5}{2}\,fF = 3.6\,fF}$$

$C_{GDi} = C_{GBi} = C_{BDi} = 0$

Total capacitance is the sum of intrinsic and extrinsic capacitances.

Overlap capacitances C_{Gsov}, C_{GDov}, C_{GBov}
Junction capacitances (area and perimeter) C_{SBJ}, C_{BDJ}
Intrinsic capacitances C_{GSi}, C_{GDi}, C_{GBi}, C_{BDi}, C_{BSi}



Gate capacitances

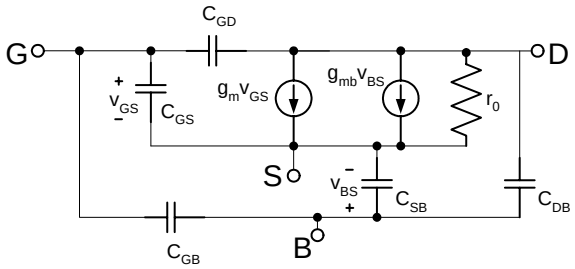
$C_{GS} = C_{GSi} +$ C_{GSov}
$C_{GD} = C_{GDi} +$ C_{GDov}
$C_{GB} = C_{GBi} +$ C_{GBov}

$C_{SB} = C_{SBi} +$ C_{SBJ}
$C_{DB} = C_{DBi} +$ C_{DBJ}

From Examples

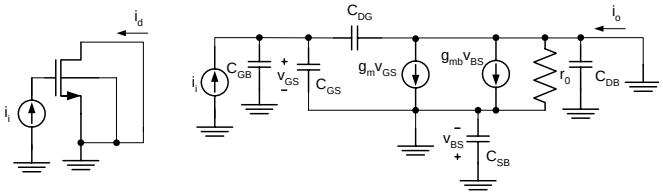
$C_{GS} = C_{GSi} + C_{GSov} = 23$ fF + 2 fF = 25 fF
$C_{GD} = C_{GDi} + C_{Gdov} = 0 + 2$ fF = 2 fF
$C_{GB} = C_{GBi} + C_{GBov} = 0 + 0.2$ fF = 0.2 fF
$C_{SB} = C_{SBi} + C_{SBJ} = 3.6$ fF + 52.5 fF = 56.1 fF
$C_{DB} = C_{DBi} + C_{DBJ} = 0 + 41.1$ fF = 41.1 fF

Complete MOSFET small-signal model



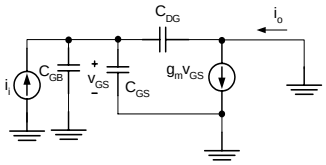
Unity Gain Frequency

This is the frequency at which the magnitude of the short-circuit current gain of the FET is unity.



$i_i = j\omega(C_{gb} + C_{gs} + C_{gd})v_{gs}$

$i_o \approx g_m v_{gs}$



neglecting current through C_{gd}

$$A_i = \frac{i_0}{i_i} = \frac{g_m}{j\omega(C_{gb} + C_{gs} + C_{gd})}$$

$A_i = 1$ at $\omega = \omega_T \Rightarrow \dfrac{g_m}{j\omega_T(C_{gb} + C_{gs} + C_{gd})} = 1$

$$\therefore \omega_T = \frac{g_m}{(C_{gb} + C_{gs} + C_{gd})} \approx \frac{g_m}{C_{gs}}$$

$$f_T = \frac{\omega_T}{2\pi} = \frac{g_m}{2\pi(C_{gb} + C_{gs} + C_{gd})} \approx \frac{g_m}{2\pi C_{gs}}$$

In saturation for n-channel MOSFET

$g_m = \dfrac{\partial I_d}{\partial V_{gs}} = K'\dfrac{W}{L}(V_{GS} - V_T)$ and $C_{GS} = \dfrac{2}{3}WLC_{ox}$

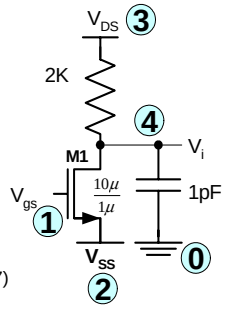
$$f_T = \frac{1}{2\pi}\frac{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)}{\frac{2}{3}WLC_{ox}} = \frac{1}{2\pi}\frac{\mu_n \frac{1}{L}(V_{GS} - V_T)}{\frac{2}{3}L} = \frac{1.5}{2\pi}\frac{\mu_n (V_{GS} - V_T)}{L^2}$$

Note: f_T increases when $V_{GS} - V_T$ increases or when L decreases

WinSpice 3 Input file

*Common-source amplifier

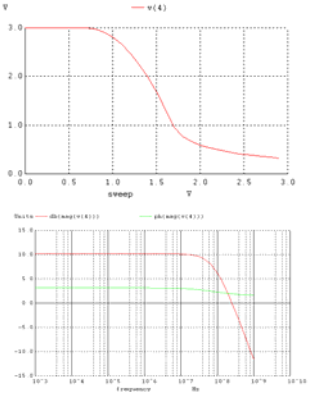
```
vds 3 0 3V
vss 2 0 0
vgs 1 0 1.5 ac 1
r1 3 4 2K
c1 4 0 1pF
m1 4 1 2 2 cmosn  l=1u w=10u
+ad=20p as=20p pd=24u ps=24u
.MODEL CMOSN NMOS ( LEVEL = 1 VTO=0.7
+ KP=200u GAMMA=0.5 LAMBDA=0.02 PHI=0.7)
.end
```



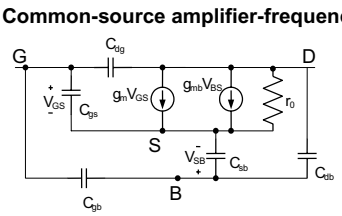

```
.control          $ can run in batch mode - $ is not a valid inline comment
op                $ runs dc operating point
print all         $ prints all node voltages
dc vgs 0 3 .1     $ runs dc analysis with input from 0 to 3V
plot v(4)         $ plots v(4), the output
ac dec 10 1K 1E9  $ runs ac analysis from 1KHZ to 1 GHZ with
                  $ 10 points per decade
plot vdb(4) vp(4) $ plots magnitude of v(4) in log scale, and phase of v(4)
.endc             $ ends batch mode
```

Output

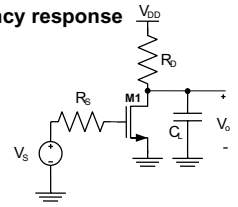
```
WinSpice 2 -> source example2.cir
Reading .\example2.cir
Circuit: *Common-source amplifier

DC Operating Point ...
v(1) = 2.000000e+00
v(2) = 0.000000e+00
v(3) = 3.000000e+00
v(4) = 5.926081e-01
vds#branch = -1.20370e-03
vgs#branch = 0.000000e+00
vss#branch = 1.203696e-03
AC analysis ...
```



Common-source amplifier-frequency response

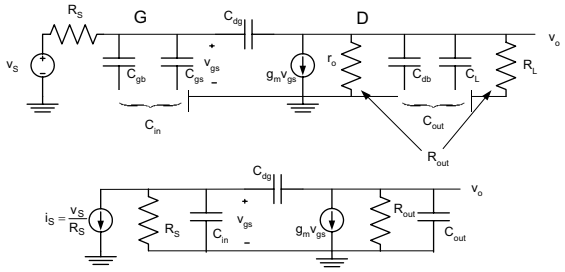


Complete small-signal MOSFET model

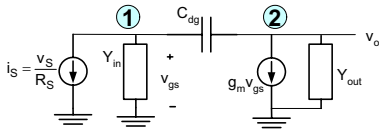


Common-source

Small-signal model for circuit



$C_{in} = C_{gb} + C_{gs}$; $C_{out} = C_{db} + C_L$; ; $R_{out} = r_o \| R_L$



$y_{in} = \dfrac{1}{R_s} + j\omega C_{in}$

$$y_{out} = \frac{1}{R_{out}} + j\omega C_{out}$$

Node 1

$$i_s = v_{gs}(y_{in}) + j\omega C_{gd}(v_{gs} - v_o)$$
$$i_s = (y_{in} + j\omega C_{gd})v_{gs} - j\omega C_{gd}v_o \qquad (1)$$

Node 2

$$g_m v_{gs} + y_{out}v_o = j\omega C_{gd}(v_{gs} - v_o)$$
$$(g_m - j\omega C_{gd})v_{gs} = -(y_{out} + j\omega C_{gd})v_o$$
$$\therefore v_{gs} = \frac{-(y_{out} + j\omega C_{gd})}{g_m - j\omega C_{gd}}v_o$$

Substitute for v_{gs} in (1)

$$i_s = (y_{in} + j\omega C_{gd})\left(\frac{-(y_{out} + j\omega C_{gd})}{g_m - j\omega C_{gd}}\right)v_o - j\omega C_{gd}v_o$$

$$i_s = \frac{-(y_{in} + j\omega C_{gd})(y_{out} + j\omega C_{gd}) - j\omega C_{gd}g_m - \omega^2 {C_{gd}}^2}{g_m - j\omega C_{gd}}v_o$$

$$i_s = \frac{-y_{in}y_{out} - j\omega C_{gd}(y_{in} + y_{out}) + \omega^2 {C_{gd}}^2 - j\omega C_{gd}g_m - \omega^2 {C_{gd}}^2}{g_m - j\omega C_{gd}}v_o$$

Expand the first two terms in the numerator

$$y_{in}y_{out} = \left(\frac{1}{R_S} + j\omega C_{in}\right)\left(\frac{1}{R_{out}} + j\omega C_{out}\right)$$
$$= \frac{1}{R_S R_{out}} + j\omega\frac{C_{in}}{R_{out}} + j\omega\frac{C_{out}}{R_S} - \omega^2 C_{in}C_{out}$$
$$= \frac{1}{R_S R_{out}}\left[1 + j\omega R_{out}C_{out} + j\omega R_S C_{in} - \omega^2 R_S R_{out}C_{in}C_{out}\right]$$

$$(y_{in} + y_{out})j\omega C_{gd} = j\omega C_{gd}\left(\frac{1}{R_S} + \frac{1}{R_{out}} + j\omega C_{in} + j\omega C_{out}\right)$$
$$= \frac{j\omega C_{gd}}{R_S R_{out}}\left[(R_S + R_{out}) + j\omega R_S R_{out}C_{in} + j\omega R_S R_{out}C_{out}\right]$$
$$= \frac{1}{R_S R_{out}}\left[j\omega(R_S + R_{out})C_{gd} - \omega^2 R_S R_{out}C_{gd}C_{in} - \omega^2 R_S R_{out}C_{gd}C_{out}\right]$$

Substitute these back in with $R_S R_{out}$ factored out

$$\therefore i_s = -v_o\frac{\left[1 + j\omega R_{out}C_{out} + j\omega R_S C_{in} + j\omega(R_S + R_{out})C_{gd} - \omega^2 R_S R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out}) + j\omega g_m C_{gd}R_S R_{out}\right]}{(g_m - j\omega C_{gd})R_S R_{out}}$$

$$i_S = \frac{v_o}{v_S}$$

$$\frac{v_o}{v_S} = \frac{-R_{out}(g_m - j\omega C_{gd})}{1 + j\omega\left[R_{out}C_{gd} + R_S C_{gd}(1 + g_m R_{out}) + R_{out}C_{out} + R_S C_{in}\right] - \omega^2 R_S R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out})}$$

$$\frac{v_o}{v_S} = \frac{-R_{out}g_m\left(1 - j\omega C_{gd}/g_m\right)}{1 + j\omega\left[R_{out}C_{gd} + R_S C_{gd}(1 + g_m R_{out}) + R_{out}C_{out} + R_S C_{in}\right] - \omega^2 R_S R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out})}$$

Observations

1) The transfer function has a zero at $\omega_Z = -\frac{g_m}{C_{gd}}$

   i.e. the voltage gain is zero when all the current through C_{gd} is the transconductance current & no current flows through the load i.e. v_o=0.

2) Recall the unity gain frequency for a MOSFET

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

$\Rightarrow \omega_Z >> \omega_T$ i.e. beyond the useful range of operation

3) The denominator of the transfer function is a second order polynomial i.e. there are two poles.

   For poles P_1 & P_2

$$D(\omega) = \left(1 + j\frac{\omega}{P_1}\right)\left(1 + j\frac{\omega}{P_2}\right)$$
$$= 1 + j\omega\left(\frac{1}{P_1} + \frac{1}{P_2}\right) - \frac{\omega^2}{P_1 P_2}$$

Let $\tau_1 = \frac{1}{P_1}$ & $\tau_2 = \frac{1}{P_2}$

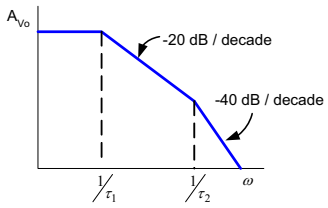
$$\Rightarrow D(\omega) = 1 + j\omega(\tau_1 + \tau_2) - \omega^2\tau_1\tau_2$$

For the transfer function

$$\tau_1 + \tau_2 = R_{out}C_{gd} + R_s C_{gd}(1 + g_m R_{out}) + R_s C_{in} + R_{out}C_{out}$$
$$\tau_1\tau_2 = R_s R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out})$$

4) The Bode plot of the 2-pole transfer function

$$A_v = \frac{A_{v_o}}{(1 + j\omega\tau_1)(1 + j\omega\tau_2)}$$



5) If the poles are widely separated (we will confirm this later) then

$$\tau_1 = \frac{1}{P_1} >> \tau_2 = \frac{1}{P_2}$$

where we have assumed $|P_2|>>|P_1|$ i.e. P_1 is the dominant pole.

$$\therefore D(\omega) \cong 1 + j\omega\tau_1 - \omega^2\tau_1\tau_2$$
$$\Rightarrow \tau_1 = R_s\left[C_{in} + C_{gd}(1 + g_m R_{out})\right] + R_{out}(C_{gd} + C_{out})$$

or $$P_1 = \frac{1}{R_s[C_{in} + C_{gd}(1 + g_m R_{out})] + R_{out}(C_{gd} + C_{out})}$$

$$P_2 = \frac{1}{P_1}\frac{1}{R_s R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out})}$$

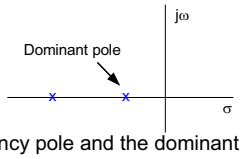
$$P_2 = \frac{R_s[C_{in} + C_{gd}(1 + g_m R_{out})] + R_{out}(C_{gd} + C_{out})}{R_s R_{out}(C_{in}C_{out} + C_{gd}C_{in} + C_{gd}C_{out})}$$

For $C_{out} \cong 0$; $P_2 = \frac{R_s[C_{in} + C_{gd}(1 + g_m R_{out})] + R_{out}C_{gd}}{R_s R_{out}C_{gd}C_{in}}$

$$P_2 = \frac{1}{R_{out}C_{gd}} + \frac{1}{R_s C_{in}} + \frac{1}{R_{out}C_{in}} + \frac{g_m}{C_{in}}$$

$$\frac{g_m}{C_{in}} = \frac{g_m}{C_{gs} + C_{gb}} \cong \frac{g_m}{C_{gs}} = \omega_T$$

$\therefore P_2 > \omega_T$



Consequently, P_2 is a high frequency pole and the dominant pole approximation can be made.

6) The capacitor C_{gd} appears as $C_{gd}(1+g_m R_{out})$ in the term with R_s

   i.e. $C_{gd}(1-(-g_m R_{out})) = C_{gd}(1-A)$

This multiplication by the gain is called the Miller effect and the capacitance $C_M = C_{gd}(1+g_m R_{out})$ is called the Miller capacitance.

So although C_{gd} is a small capacitance its effect is much larger depending on the gain of the amplifier.

We will use the Miller capacitance to simplify our analysis with the capacitor C_{gd} that couples the input & output. This is an approximation but works well as we shall see!

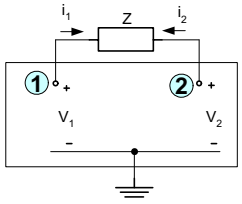
7) Examine the large time constant τ_1 corresponding to the dominant pole

$$\tau_1 = \underbrace{R_s[C_{in} + C_{gd}(1+g_m R_{out})]}_{\tau_a} + \underbrace{R_{out}(C_{gd}+C_{out})}_{\tau_b}$$

$\tau_1 = \sum \tau$, the sum of time constants

We will be able to determine τ_1 by an approximate technique known as zero-value time constants (to be done later).

Miller's Theorem (Miller Effect)



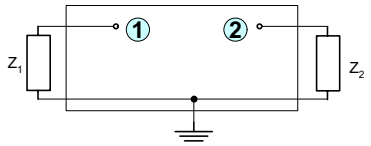
Let $k = \frac{v_2}{v_1}$ be a known quantity, which is a complex number.

$$i_1 = \frac{v_1 - v_2}{Z} = \frac{v_1 - kv_1}{Z} = \frac{v_1(1-k)}{Z}$$
$$= \frac{v_1}{Z/(1-k)} = \frac{v_1}{Z_M}$$

Therefore, if $Z_M = \frac{Z}{1-k}$ were shunted across terminal ① and ground, the current drawn from ① would be the same as that of the original circuit. This is the Miller effect.

Similarly $i_2 = \frac{v_2 - v_1}{Z} = \frac{v_2 - v_2/k}{Z}$
$$= \frac{v_2(k-1)/k}{Z} = \frac{v_2}{Z \cdot k/(k-1)}$$

So the original circuit can be transformed as



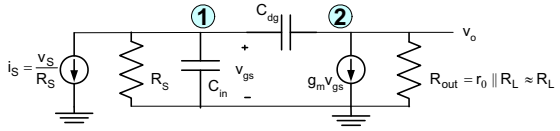
$Z_1 = \frac{Z}{1-k}$; $Z_2 = Z\frac{k}{k-1} \cong Z$ if k is large

Remarks

- k is the forward voltage ratio. The Miller effect can only be used to find the forward gain and input impedance. NEVER use it to calculate output impedance.
- Physically C_{gd} is getting multiplied by the voltage gain of the amplifier and hence has a larger effect at the input.

Application of Miller Approximation

For simplicity neglect C_{out}



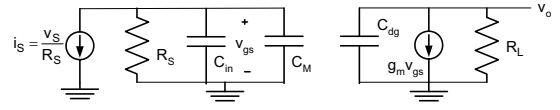
Assuming current through C_{gd} is small we can calculate the gain from ① to ②

$$k = \frac{v_2}{v_1} = \frac{v_o}{v_{gs}} = -g_m R_{out} = -g_m R_L$$

∴ C_{gd} reflected to the input is $C_{gd}(1-k) = C_{gd}(1+g_m R_L)$

$$C_M = C_{gd}(1+g_m R_L)$$

The circuit becomes



where we have assumed that $g_m R_L$ is large and $Z_2 \approx Z$.

This circuit is much simpler to analyze. Furthermore, we obtain a 1-time constant system

$$Y_{in} = \frac{1}{R_s} + s(C_{in} + C_M)$$

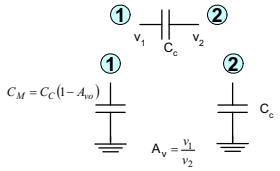
The time constant associated with the capacitance ($C_{in}+C_M$) is $R_s(C_{in}+C_M)$.

From the detailed analysis the time constant is

$$R_s[C_{in} + \underbrace{C_{gd}(1+g_m R_L)}_{\text{Miller capacitance}}] + \underbrace{R_L C_{gd}}_{\text{Output time constant}}$$

Key Points

1) Use Miller approximation for calculating ONLY input impedance and forward gain. DO NOT use for calculating output impedance.

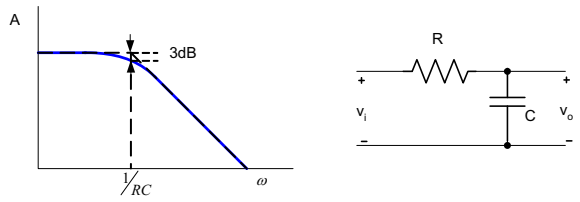


2) For calculation of time constants use the low frequency gain.

3) At low frequencies C_c appears as a capacitance at the input of value $C_M = C_C(1-A_v(0))$

4) For higher frequencies A_v is frequency dependent
⇒ the input is reflected as an admittance
$Y_M(s) = sC_c(1-A_v(s))$
C_c no longer appears as the pure Miller capacitance.

Calculation of bandwidth (-3dB frequency)



$$\omega_{-3dB} = \frac{1}{RC} \Rightarrow f_{-3dB} = \frac{1}{2\pi RC}$$

How do we get this information for complex circuits?

For the simple CS amplifier we have seen that

$$\tau_1 + \tau_2 = R_{out}C_{gd} + R_s(1 + g_m R_{out})C_{gd} + R_s C_{in} + R_{out}C_{out}$$

and if we assumed a dominant pole then

$$\tau_1 \cong R_{out}C_{gd} + R_s(1 + g_m R_{out})C_{gd} + R_s C_{in} + R_{out}C_{out}$$
$$= \sum_{\text{i = no. of caps}} R_i C_i$$

Let us revisit the dominant-pole approximation

Consider the transfer function

$$A(s) = \frac{k}{\left(1 - \frac{s}{P_1}\right)\left(1 - \frac{s}{P_2}\right)\cdots\left(1 - \frac{s}{P_n}\right)}$$

Where the zeros are not important in the frequency range of interest.

A(s) can also be written as

$$A(s) = \frac{k}{1 + b_1 s + b_2 s^2 + \cdots + b_n s^n}$$

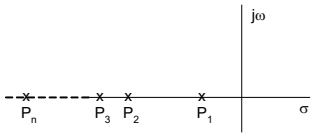
where

$$b_1 = \sum_{i=1}^{n}\left(-\frac{1}{P_i}\right)$$

Now consider a dominant pole say P_1 then

$|P_1| << |P_2|, |P_3|, \ldots..|P_n|$

Then $\left|\frac{1}{P_1}\right| >> \left|\sum_{i=2}^{n}\left(-\frac{1}{P_i}\right)\right|$



so that $b_1 \cong -\frac{1}{P_1}$ is the coefficient corresponding to the dominant pole

The magnitude |A(jω)| is

$$|A(j\omega)| = \frac{|k|}{\sqrt{\left[1 + \left(\frac{\omega}{P_1}\right)^2\right]\left[1 + \left(\frac{\omega}{P_2}\right)^2\right]\cdots\left[1 + \left(\frac{\omega}{P_n}\right)^2\right]}}$$

For a dominant pole P_1 this is approximated as

$$|A(j\omega)| \cong \frac{|k|}{\sqrt{1 + \left(\frac{\omega}{P_1}\right)^2}}$$

Remark

This approximation will be accurate until $\omega \cong |P_1|$, and the transfer function has no zeros.

$\omega_{-3dB} \cong |P_1|$

How can we calculate P_1 (at least a reasonable value) without having to evaluate the whole transfer function?

Answer: zero value time constants (ZVTC).

ZVTC Method

- yields a dominant pole if it exists ⇒ fairly accurate -3dB frequency
- Does not give any info about the zeros
  ⇒ for a circuit in which there is a dominant zero, the -3dB frequency calculated using ZVTC will be wrong.

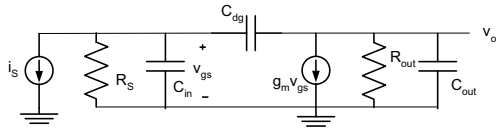
Procedure

- For each capacitor C_i in the circuit i=1, …., N,
  1) Open all other capacitors $C_1,\ldots..C_{i-1},C_{i+1},\ldots C_N = 0$
     i.e. set them to a '0' value
  2) Find the Thevenin resistance R_i seen by capacitor C_i (short independent voltage sources and open current sources)
  3) Calculate the product R_iC_i – this is the zero-value time constant associated with C_i.
- Sum up all the individual time constants.
  Then $b_1 = \sum R_i C_i$

Remark

This calculation of b_1 is exact.

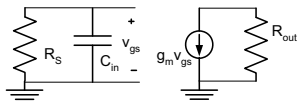
Example of ZVTC method with CS amplifier



3 Capacitors C_{in}, C_{gd}, C_{out}; Calculate R_i for each

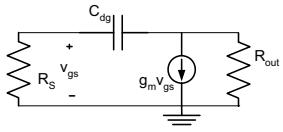
C_{in}

$R_i = R_s$



$\therefore$ time constant = $R_sC_{in} = \tau_{Cin}$

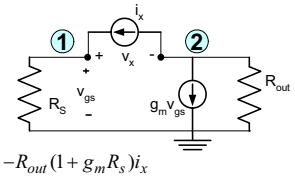
C_{gd}



Node ①:

$$v_{gs} = v_1 = i_x R_s$$

Node ②:



$$i_x + g_m v_{gs} + \frac{v_2}{R_{out}} = 0$$

$$\Rightarrow v_2 = -R_{out}(i_x + g_m v_{gs})$$
$$= -R_{out}(i_x + g_m R_s i_x) = -R_{out}(1 + g_m R_s) i_x$$

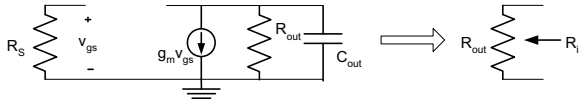
$$v_x = v_1 - v_2 = i_x R_s + R_{out}(1 + g_m R_s) i_x$$
$$= i_x[R_{out} + R_s(1 + g_m R_{out})]$$

$$\therefore\ R_i = \frac{v_x}{i_x} = R_{out} + R_s(1 + g_m R_{out})$$

$$\therefore\ \tau_{C_{gd}} = C_{gd}[R_{out} + R_s(1 + g_m R_{out})]$$

$$= C_{gd}R_{out} + \underbrace{R_s(1 + g_m R_{out})C_{gd}}_{\text{Miller capacitance}}$$

C_{out}



$$\tau_{C_{out}} = R_{out}C_{out}$$

Final Sum

$$b_1 = \sum \tau_{i_o} = R_s C_{in} + C_{gd}R_{out} + R_s(1 + g_m R_{out})C_{gd} + R_{out}C_{out}$$

Remark

This is the same expression we obtained from the exact analysis with a dominant-pole approx.

$$\therefore\ \omega_{-3dB} = \frac{1}{\sum \tau_{i_o}}$$

Numerical Example

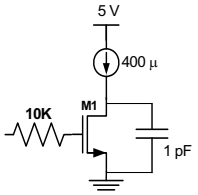
$$I_D = 400\mu A, \quad \frac{W}{L} = \frac{50\mu}{2\mu}$$

$$k' = 50\mu A/V^2,\ V_T = 1.0V$$

$$\lambda = 0.05V^{-1} \text{ for } L = 2\mu$$

$$C_{ox} = 1fF/\mu^2;$$

$$C_{ov} = C_{GSO} = C_{GDO} = 0.5fF/\mu m$$



For the device in saturation

$$C_{gd} = C_{ov}W = 0.5fF \times 50 = 25fF$$

$$C_{gs} \cong \frac{2}{3}WLC_{ox} = \frac{2}{3}(50)(2)(1)fF$$

$$= 67fF + 25fF = 92fF$$

Calculate g_m & r_o

$$g_m = \sqrt{2k'I_D\frac{W}{L}} = \sqrt{2 \times 50 \times 400\left(\frac{50}{2}\right)}\mu A/V$$

$$= 1mA/V$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05(400 \times 10^{-6})} = 50k\Omega$$

For this example R_{out} = 50kΩ, C_{out} = 1pF.

Compute various time constants:

$$\tau_{C_{in}} = R_s C_{in} = R_s C_{gs} = 10k \times 92fF = 0.92ns$$

$$\tau_{C_{gd}} = R_{out}C_{gd} + R_s(1 + g_m R_{out})C_{gd}$$

$$= (50k + 10k(1 + 50))25fF = 14ns$$

$$\tau_{C_{out}} = C_{out}R_{out} = 1.025pF(50k\Omega) = 51.25ns$$

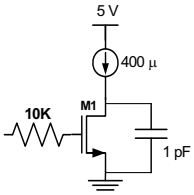
$\therefore$ the largest time constant is due to the load capacitance.

$$\omega_{-3dB} = \frac{1}{0.92 + 14 + 50} \times 10^9 rad/\sec$$

$$f_{-3dB} = \frac{1}{2\pi}\omega_{-3dB} = 2.46MHz$$

SPICE Simulation

```
* calculate poles and zeros

*input: 4, output: 1

*Power supplies
VDD 10 0 5

*circuit
M8 1 2 0 0 CMOSN L=2u W=50u
ID 10 1 400.0uA
rs 4 2 10K
cl 1 0 1p

*sources
vs 4 0 1.78 ac 1

.MODEL CMOSN NMOS( LEVEL=1 KP=50u VTO=1.0 LAMBDA=0.05
+TOX=34.5n CGDO=.5n)

.control
op
run
show m8 model
print all
tf v(1) vs
print all
pz 4 0 1 0 vol pz
print all
.endc
.end
```



SPICE Output

```
DC Operating Point ...
 Mos1: Level 1 MOSfet model with Meyer capaci
  device           m8
  model          cmosn
         id    0.0004
         is   -0.0004
         ig         0
         ib -4.02e-13
```



```
        vgs      1.78
        vds      1.04
        vbs         0
        von         1
      vdsat      0.78
         rs         0
         rd         0
         gm   0.00103
        gds   1.9e-05      ⇒ r_o = 52.6K
        gmb         0
        cbd         0
        cbs         0
        cgs  3.34e-14
        cgd         0

v(1) = 1.038790e+00
v(2) = 1.780000e+00
v(4) = 1.780000e+00
v(10) = 5.000000e+00
vdd#branch = -4.00000e-04
vs#branch = 1.646420e-20
Transfer function analysis ...
transfer_function = -5.39456e+01                    A_v
output_impedance_at_v(1) = 5.259697e+04
vs#input_impedance = 1.000000e+20
Pole-Zero analysis ...
Warning: Pole-zero iteration limit reached; g
pole(1) = -1.37590e+09,0.000000e+00                 ⇒ f1 = 219 MHz
pole(2) = -1.47954e+07,0.000000e+00                 ⇒ f2 = 2.35 MHz  versus 2.46 MHz by hand
zero(1) = 4.102564e+10,0.000000e+00                 ⇒ zero = 41 GHz
```

Remarks

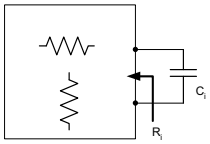
- $\sum \tau_o = \sum_{i=1}^{n}\left(-\frac{1}{P_i}\right)$ is valid in general

  i.e. the sum of zero-value time constants equals the sum of the reciprocals of all poles, whether or not a dominant pole exists.

- Setting $\omega_{-3dB} = \frac{1}{\sum \tau_o}$ can give an error if a dominant pole situation doesn't exist. However, the ω_{-3dB} will then be a pessimistic estimate.

- If parts of a circuit are isolated from the rest then the ZVTC will give the pole information associated with these parts.

Hence, the ZVTC could also be used to estimate non-dominant poles.



$$\tau_i = C_i R_i$$

$$\Rightarrow \text{ pole} = \frac{1}{C_i R_i}$$

Example of Error

Consider a circuit that has two identical negative real poles at ω_x

$$A(j\omega) = \frac{A_o}{\left(1 + j\frac{\omega}{\omega_x}\right)\left(1 + j\frac{\omega}{\omega_x}\right)}$$

$$|A(j\omega)| = \frac{A_o}{\sqrt{2}} \text{ at } \omega_{-3dB} \quad \Rightarrow \quad \frac{A_o}{\sqrt{2}} = \frac{A_o}{1 + \left(\frac{\omega_{-3dB}}{\omega_x}\right)^2}$$

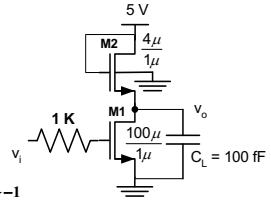
$$\Rightarrow \omega_{-3dB} = \omega_x\sqrt{(\sqrt{2}-1)} = 0.64\omega_x$$

Using ZVTC we will obtain $\sum \tau_o = \frac{1}{\omega_x} + \frac{1}{\omega_x} = \frac{2}{\omega_x}$

$$\Rightarrow \omega_{-3dB} = \frac{1}{\sum \tau_o} = \frac{\omega_x}{2} = 0.5\omega_x$$

i.e. ZVTC will result only in 22% error!

Example



$k' = 60\mu A/V^2$, $t_{ox} = 200A°$

$C_{GSO} = C_{GDO} = 0.3\,fF/\mu$

$C_{JO} = 0.8\,fF/\mu$

$\varphi_B = 0.6V$, $\phi = 0.6V$

$V_T = 0.7V$, $\gamma = 0.4V^{1/2}$, $\lambda = 0V^{-1}$

$V_o = 2.5V$, $MJ = 0.5$

i).Calculate small-signal low-frequency gain.
ii).Use ZVTC method for calculating -3dB frequency

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-13}\,F/cm}{0.2\times10^{-5}\,cm} = 1.725\,fF/\mu^2$$

DC analysis

$$V_o = 2.5V \Rightarrow V_{GS2} = 5 - 2.5 = 2.5V$$

$$V_{T2} = 0.7 + 0.4\left[\sqrt{2.5+0.6} - \sqrt{0.6}\right] = 1.1V$$

$$I_{D2} = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$= \frac{60}{2}\left(\frac{4}{1}\right)(2.5-1.1)^2 = 235\mu A$$

Gain

$$g_{m2} = \frac{2I_D}{V_{GS} - V_T} = \frac{2\times235}{2.5-1.1} \cong 336\mu A/V$$

$$g_{m1} = \sqrt{2k'I_D\left(\frac{W}{L}\right)} = \sqrt{2\times60\times235\left(\frac{100}{1}\right)} = 1.68mA/V$$

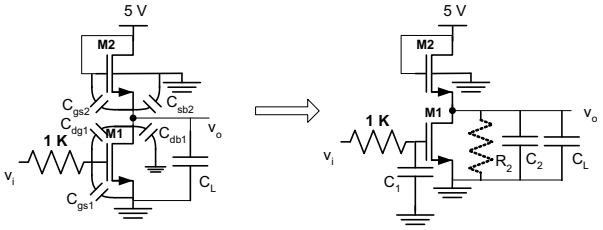
$$\text{Low - frequency gain} = -g_{m1}\cdot\frac{1}{g_{m2} + g_{mb2}}$$

$$= -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\frac{g_{mb2}}{g_{m2}}} = -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta}$$

$$\eta = \frac{\gamma}{2\sqrt{V_{SB} + \phi}} = \frac{0.4}{2\sqrt{2.5+0.6}} = 0.11$$

$$\therefore \quad A_{v_o} = -\frac{1.68\times10^3}{336}\frac{1}{1+0.11} = -4.5$$

ZVTC method



Calculate capacitances

$$C_1 = C_{GS1} + (1 + g_m R_{out})C_{GD1}$$

$$C_2 = C_{GD1} + C_{DB1} + C_{GS2} + C_{SB2}$$

$$R_1 = 1k\Omega; \qquad R_2 = \frac{1}{g_{m2} + g_{mb2}} = \frac{1}{g_{m2}(1.11)} = 2.68k\Omega$$

$$C_{DB1} = 0.3\,fF/\mu \times 100\mu = 30\,fF$$

$$C_{GS1} = \frac{2}{3}WLC_{ox} + WC_{GSO}$$

$$= \frac{2}{3}(100)(1)1.725 + 100(0.3) \quad fF$$

$$= 115 + 30 = 145\,fF$$

$$C_{GS2} = \frac{2}{3}(4)(1)1.725 + 4(0.3) \quad fF$$

$$= 4.6 + 1.2 = 5.8\,fF$$

$$C_{db1} = \frac{C_{J0}W}{\left(1+\frac{V_{DB1}}{\varphi_B}\right)^{0.5}} = \frac{0.8\times100}{\sqrt{1+\frac{2.5}{0.6}}} = 35.2\,fF$$

$$C_{sb2} = \frac{C_{J0}W}{\left(1+\frac{V_{SB2}}{\varphi_B}\right)^{0.5}} = \frac{0.8\times4}{\sqrt{1+\frac{2.5}{0.6}}} = 1.4\,fF$$

Calculate time constants

$$\tau_1 = C_1R_s = R_s[C_{GS1} + (1 + \underbrace{g_{m1}R_{out}}_{A_{v_o}\ \leftarrow \text{already calculated}})C_{GD1}]$$

$$= 1k[145 + (1+4.5)30]\,fF = 310\,ps.$$

$$\tau_2 = R_2(C_2 + C_L)$$

$$= 2.68k[C_{GD1} + C_{DB1} + C_{GS2} + C_{SB2} + C_L]$$

$$= 2.68k[30 + 35.2 + 5.8 + 1.4 + 100]\,fF$$

$$= 462\,ps.$$

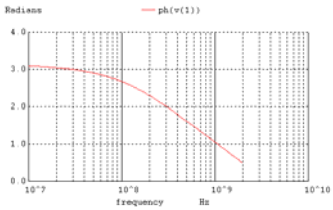
$$\therefore \tau_1 + \tau_2 = 310 + 462 = 772\,ps$$

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{772\times10^{-12}} = 206MHz$$

SPICE Simulation

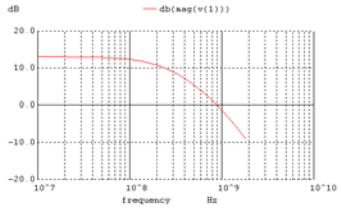
```
* calculate poles and zeros

*input: 4, output: 1

*Power supplies
VDD 5 0 5

*circuit
M2 5 5 1 0 CMOSN_2 L=1u W=4u
M1 1 2 0 0 CMOSN_1 L=1u W=100u
rs 4 2 1K
cl 1 0 100f

*sources
vs 4 0 .98 ac 1

.MODEL CMOSN_1 NMOS( LEVEL=1 KP=60u VTO=0.7 LAMBDA=0.0
+TOX=20n CGDO=.3n cgso=.3n cbd=80f cbs=80f phi=0.6
+pb=0.6 mj=0.5 gamma=0.4)
.MODEL CMOSN_2 NMOS( LEVEL=1 KP=60u VTO=0.7 LAMBDA=0.0
+TOX=20n CGDO=.3n cgso=.3n cbd=3.2f cbs=3.2f phi=0.6
+pb=0.6 mj=0.5 gamma=0.4)

.control
op
run
show m1 model m2 model
print all
tf v(1) vs
print all
pz 4 0 1 0 vol pz
print all
.endc
.end
```

5 V



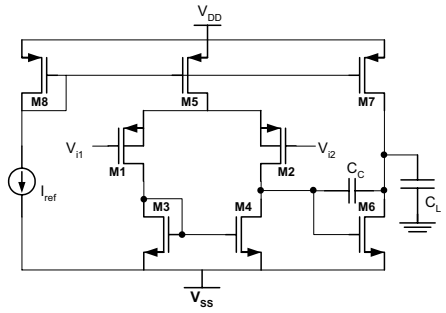
Output

```
DC Operating Point ...
 Mos1: Level 1 MOSfet model with Meyer capacitance model
 device            m1         m2
 model        cmosn_1    cmosn_2
        id  0.000235  0.000235
        is -0.000235 -0.000235
        ig         0          0
        ib -9.69e-13  -2.9e-12
       vgs      0.98       2.5
       vds       2.5       2.5
       vbs         0      -2.5
       von       0.7       1.1
     vdsat      0.28       1.4
        rs         0          0
        rd         0          0
        gm   0.00168   0.000336
```



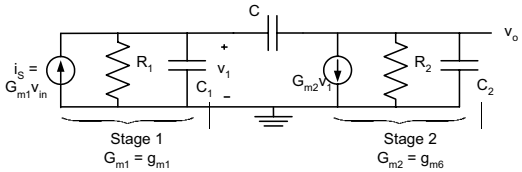

```
      gds         0          0
      gmb  0.000434   3.81e-05
      cbd   3.52e-14   1.05e-15
      cbs      8e-14   1.41e-15
      cgs  5.76e-14    2.3e-15
      cgd         0          0
      cgb         0          0
     cbd0      8e-14    3.2e-15
   cbdsw0         0          0
     cbs0      8e-14    3.2e-15
   cbssw0         0          0

v(1) = 2.504998e+00
v(2) = 9.800000e-01
v(4) = 9.800000e-01
v(5) = 5.000000e+00
vdd#branch = -2.35200e-04      I_D2
vs#branch = 3.430483e-20

Transfer function analysis ...
transfer_function = -4.49034e+00
output_impedance_at_v(1) = 2.672823e+03
vs#input_impedance = 1.000000e+20

Pole-Zero analysis ...
pole(1) = -8.30652e+09,0.000000e+00        1.32 GHz
pole(2) = -1.53808e+09,0.000000e+00        244 MHz  versus 206 MHz
zero(1) = 5.600000e+10,0.000000e+00        8.91 GHz
```


Frequency response of two-stage CMOS opamp



$R_1 = r_{o2} \parallel r_{o4}$
$R_2 = r_{o6} \parallel r_{o7}$

$C_1 = C_{gs6} + C_{gd4} + C_{db4} + C_{gd2} + C_{db2}$
$C_2 = C_L + C_{db6} + C_{gd7} + C_{db7}$
$C = C_c + C_{gd6}$



$$\frac{v_o}{i_s} = -\frac{(G_{m2} - sC)R_1R_2}{1 + s\left[R_1C_1 + R_2C_2 + R_2C + R_1C(1 + G_{m2}R_2)\right] + s^2R_2R_1(C_1C_2 + CC_1 + CC_2)}$$

The denominator is in the form of a 2-pole transfer function

$$D(s) = \left(1 - \frac{s}{P_1}\right)\left(1 - \frac{s}{P_2}\right) = 1 - s\left(\frac{1}{P_1} + \frac{1}{P_2}\right) + \frac{s^2}{P_1P_2}$$

If P_1 is the dominant pole then

$$D(s) \cong 1 - \frac{s}{P_1} + \frac{s^2}{P_1P_2}$$

$$\Rightarrow P_1 = -\frac{1}{R_1C_1 + R_2C_2 + R_2C + R_1C(1 + G_{m2}R_2)}$$

For large C & $G_{m2}R_2$

$$P_1 \cong -\frac{1}{G_{m2}R_1R_2C}$$

From the s^2 term: $$P_2 = \frac{1}{P_1}\frac{1}{R_2R_1(C_1C_2 + CC_1 + CC_2)}$$

$$P_2 \cong -\frac{G_{m2}C}{C_1C_2 + CC_1 + CC_2} = -\frac{G_{m2}C}{C_1C_2 + C(C_1 + C_2)}$$

Remark

As C increases $|P_1|$ decreases whereas $|P_2|$ increases

$\Rightarrow$ pole splitting. The limiting value of $|P_2|$ is $\frac{G_{m2}}{C_1 + C_2}$, a large frequency.

Pole splitting

When C = 0, we have 2 poles in the circuit.

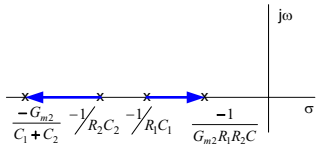
$$P_1 = -\frac{1}{R_1 C_1}$$

$$P_2 = -\frac{1}{R_2 C_2}$$

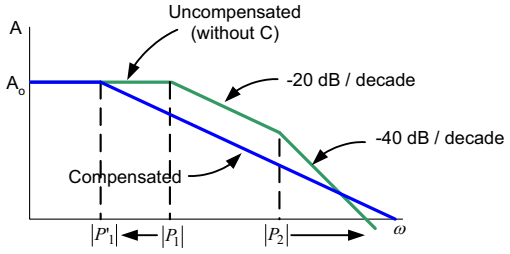
With the capacitor C

$$P_1 \cong -\frac{1}{G_{m2} R_1 R_2 C} \quad \to 0 \quad \text{as } C \uparrow$$

$$P_2 \cong -\frac{G_{m2} C}{C_1 C_2 + C(C_1 + C_2)} \quad \to -\frac{G_{m2}}{C_1 + C_2} \quad \text{as } C \uparrow$$



As C is increased, the poles split apart and a dominant pole situation is created.



Assuming a one-pole roll-off due to $|P_1'|$, we have

$$A_v(s) = \frac{G_{m1} R_1 G_{m2} R_2}{1 + s G_{m2} R_1 R_2 C}$$

Unity gain frequency = $|A_v|$ = 1

$$|A_v(\omega)| \cong \frac{G_{m1} R_1 G_{m2} R_2}{\omega_u G_{m2} R_1 R_2 C} = 1$$

$$\therefore \omega_u = \frac{G_{m1}}{C} = \frac{g_{m1}}{C}$$

How to choose C?

As we will see later, one choice is to make $|P_2'| = \omega_u$

$$\Rightarrow \frac{G_{m2} C}{C_1 C_2 + C(C_1 + C_2)} = \frac{G_{m1}}{C}$$

Can solve a quadratic to obtain C.

If $C_1 << C$, C_2 then

$$\frac{G_{m2} C}{C C_2} = \frac{G_{m1}}{C}$$

$$\text{or} \quad C = \frac{G_{m1}}{G_{m2}} C_2 \quad \Rightarrow \text{maximize } G_{m2} \text{ for smaller C.}$$

Remarks

$$\omega_{-3dB} = \frac{1}{G_{m2} R_1 R_2 C}; \quad A_v = G_{m1} R_1 G_{m2} R_2$$

$$\therefore A_v \cdot \omega_{-3dB} = \frac{G_{m1}}{C} = 1 \cdot \omega_u$$

i.e. Gain x bandwidth is a constant (GBW)

$$\omega_u \propto g_m; \quad A_v \propto \frac{g_m}{g_o} = \frac{2 I_D}{V_{GS} - V_T} \cdot \frac{1}{\lambda I_D}$$

Increasing $I_D \Rightarrow g_m \uparrow$ but $(V_{GS} - V_T) \uparrow \Rightarrow A_v \downarrow$

Design Example (2-stage op amp)

The dc and low-frequency gain were done previously. Now we look at the high frequency behavior with C_L=7.5pF.

Device Parameters

n-ch: C_{ov} = 0.5 fF/μ, C_{jo} = 0.1 fF/μ^2, $C_{js\omega o}$ = 0.5 fF/μ
PB = PBSW = 0.8, MJ = MJSW = 0.5
p-ch: C_{ov} = 0.5 fF/μ, C_{jo} = 0.3 fF/μ^2, $C_{js\omega o}$ = 0.35 fF/μ
PB = PBSW = 0.8, MJ = MJSW = 0.5
t_{ox} = 15 x 10^{-9} m = 150 Å; C_{ox} = 2.3 x 10^{-7} F/cm^2 = 2.3 fF/μ^2

For area and perimeter calculations use L_{diff} = 6μm for source and drain regions.

Calculate capacitances

$$C_{gs6} = \frac{2}{3} W \cdot L \cdot C_{ox} + C_{ov} \cdot W$$

$$= \frac{2}{3}(150)(3)(2.3) + 0.5(150) \text{ fF}$$

$$= 765 \text{ fF}$$

$$C_{gd6} = 0.5 \times 150 = 75 \text{ fF}$$

$$C_{gd7} = 75 \text{ fF}$$

$$C_{gd4} = 0.5 \times 75 = 37.5 \text{ fF}$$

$$C_{gd2} = 0.5 \times 150 = 75 \text{ fF}$$

$$C_{db4} = \frac{C_{jo} \cdot AD}{\left(1 + \frac{V_{db4}}{PB}\right)^{0.5}} + \frac{C_{js\omega_o} \cdot PD}{\left(1 + \frac{V_{db4}}{PB}\right)^{0.5}}$$

$$AD = 75 \times 6 = 450 \mu^2; \quad PD = 162 \mu$$

Drain of M4 is at -1.52 V, bulk is at -2.5V $\Rightarrow V_{DB}$ = 0.98V

$$\therefore C_{db4} = \frac{0.1 \times 450 + 0.5 \times 162}{\sqrt{1 + \frac{0.98}{0.8}}}$$

$$= 84.5 \text{ fF}$$

Drain of M6 at 0V, bulk at -2.5V $\Rightarrow V_{DB6}$ = 2.5V

$$\therefore C_{db6} = \frac{0.1 \times 900 + 0.5 \times 312}{\sqrt{1 + \frac{2.5}{0.8}}} \cong 121 \text{ fF}$$

Drain of M2 at -1.52V, bulk at V_s = 0.98V $\Rightarrow V_{DB2}$ = 2.5V

Drain of M7 at 0V, bulk at +2.5V $\Rightarrow V_{DB6}$ = 2.5V

$$\therefore C_{db2} = C_{db7} = \frac{0.3 \times 900 + 0.35 \times 312}{\sqrt{1 + \frac{2.5}{0.8}}} = 186.7 \text{ fF}$$

$$\therefore C_1 = C_{gs6} + C_{gd4} + C_{db4} + C_{gd2} + C_{db2}$$

$$= 765 + 37.5 + 84.5 + 75 + 186.7 = 1.15 \text{ pF}$$

$$C_2 = C_L + C_{db6} + C_{gd7} + C_{db7}$$

$$= 7.5 + (0.121 + 0.075 + 0.1867) \cong 7.88 \text{ pF}$$

$$C = C_C + C_{gd6} = C_C + 75 \text{ fF}$$

Calculate the unity gain frequency

We have $G_{m1} = g_{m1} = 353.5\mu A/V$, $G_{m2} = g_{m6} = 707\mu A/V$

$$\therefore \omega_u = \frac{G_{m1}}{C} \quad \text{where } C \cong \frac{G_{m1}}{G_{m2}} C_2$$

$$\therefore C \cong \frac{1}{2} \times 8\,\text{pF} = 4\,\text{pF}$$

$$\therefore C_C = 4 - 0.075\,\text{pF} \cong 4\,\text{pF}$$

$$\omega_u = \frac{353.5 \times 10^{-6}}{4 \times 10^{-12}} = 88\,\text{Mrad/sec}$$

$$f_u = 14\,\text{MHz}$$

Calculate the pole frequencies

$$R_1 = 333.34\ k\Omega; \quad R_2 = 166.67\ k\Omega$$

$$P_1 \cong -\frac{1}{707 \times 10^{-6}(333.34)(166.67)10^6 \times 4 \times 10^{-12}}$$

$$\omega_{p1} \cong 6.36\ krad/\text{sec} \quad \Rightarrow \quad f_{P1} = 1013\ kHz$$

$$P_2 = -\frac{707 \times 10^{-6} \times 4 \times 10^{12}}{1.2 \times 8 + 4(1.2 + 8)} = 60.9\ Mrad/\text{sec}$$

$$\therefore f_{P2} = 9.7\ MHz$$

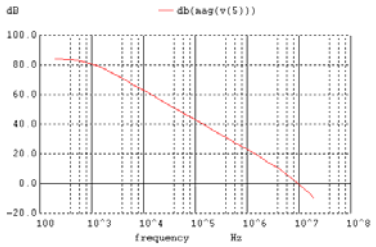
Remark

- A zero appears at $\omega_z = \frac{G_{m2}}{C} \cong 28MHz$ i.e. it is beyond the unity gain frequency.

- From SPICE the poles and zeros are
  poles: 855 Hz, 10 MHz, 17 MHz
  zeros: 17 MHz, 28.6 MHz
  f_{unity} = ~10 MHz

SPICE file

```
* Two-stage op-amp

*inputs: inverting node 7, noninverting node 8
vinp 7 0 0 ac 1
vinm 8 0 17.2745u
*Power supplies
VDD 10 0 2.5
Vss 20 0 -2.5

*load cap
c1 5 0 7.5p
*compensation cap
cc 5 4 4p
*Current mirror
M8 1 1 10 10 CMOSP L=3u W=75u AD=450p AS=450p PD=162u ps=162u
Iref 1 20 50.0uA
*Differential amp
*ISS
M5 2 1 10 10 CMOSP L=3u W=150u AD=900p AS=900p PD=312u ps=312u
*Drivers
M1 3 7 2 2 CMOSP L=3u W=150u AD=900p AS=900p PD=312u ps=312u
M2 4 8 2 2 CMOSP L=3u W=150u AD=900p AS=900p PD=312u ps=312u
*Active loads
M3 3 3 20 20 CMOSN L=3u W=75u AD=450p AS=450p PD=162u ps=162u
M4 4 3 20 20 CMOSN L=3u W=75u AD=450p AS=450p PD=162u ps=162u
*2nd stage
M7 5 1 10 10 CMOSP L=3u W=150u AD=900p AS=900p PD=312u ps=312u
M6 5 4 20 20 CMOSN L=3u W=150u AD=900p AS=900p PD=312u ps=312p

.MODEL CMOSN NMOS( LEVEL=1 KP=50u VTO=0.7 LAMBDA=0.03
+cgdo=0.5n cgso=0.5n cj=0.1m cjsw=0.5n mj=0.5 mjsw=0.5
+pb=0.8 tox=15n)
.MODEL CMOSP PMOS( LEVEL=1 KP=25u VTO=-0.7 LAMBDA=0.03
+cgdo=0.5n cgso=0.5n cj=0.3m cjsw=0.35n mj=0.5 mjsw=0.5
+pb=0.8 tox=15n)

.control
op
print all
ac dec 10 200 20meg
plot vdb(5)
pz 7 8 5 0 vol pz
print all
.endc
.end
```



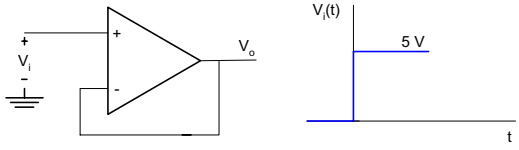
Output

```
Circuit: * Two-stage op-amp

DC Operating Point ...
v(1) = 1.406404e+00
v(2) = 9.745308e-01
v(3) = -1.51948e+00
v(4) = -1.52169e+00
v(5) = 1.238277e-06  (Near zero)
v(7) = 0.000000e+00
v(8) = 1.727450e-05
v(10) = 2.500000e+00
v(20) = -2.50000e+00
vdd#branch = -2.55340e-04
vinm#branch = 0.000000e+00
vinp#branch = 0.000000e+00
vss#branch = 2.553396e-04

AC analysis ...
Pole-Zero analysis ...
Warning: Pole-zero iteration limit reached; giving up after 264 trials
pole(1) = -3.24673e+08,1.030280e+08
pole(2) = -3.24673e+08,-1.03028e+08
pole(3) = -1.14110e+08,0.000000e+00
pole(4) = -6.51190e+07,0.000000e+00
pole(5) = -5.38023e+03,0.000000e+00
zero(1) = -3.27455e+08,0.000000e+00
zero(2) = -1.13284e+08,0.000000e+00
zero(3) = 1.875935e+08,0.000000e+00
```

Note that poles and zeros are in radians/sec

Slew Rate

Up to now we have looked at the small-signal behavior of our op amp. However, the behavior with large input signals is also of interest.



Unity gain configuration

Suppose that the circuit has a one pole transfer function then

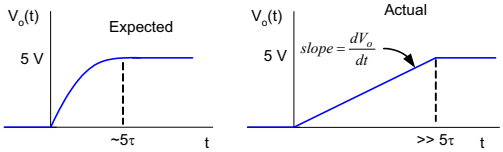
$$\frac{V_o}{V_i}(s) = \frac{1}{1 + s\tau}$$

$$\text{where} \quad \tau = \frac{1}{2\pi f_{-3dB}}$$

For $V_i(s) = \frac{5}{s}$ (i.e. a step input)

$$V_o(s) = \frac{1}{1 + s\tau} \cdot \frac{5}{s} = 5\left[\frac{\left(s + 1/\tau\right) - s}{s(s + 1/\tau)}\right] = \frac{5}{s} - \frac{5}{s + 1/\tau}$$

or $V_o(t) = 5(1 - e^{-t/\tau})$



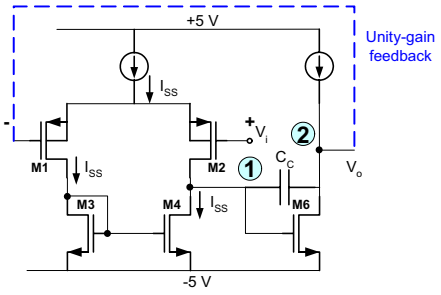
Slew rate = $\frac{dV_o}{dt}$ (usually specified in V/μs)

Examine the operation of the 2-stage CMOS opamp

The origin of the constant slope region is a large signal behavior.

At time=0, V_i^+ steps to 5V, the output voltage cannot respond immediately $\Rightarrow V_o = 0$

$\Rightarrow V_i^- = 0$ & $V_i^+ = 5V$



$\therefore$ M2 cuts off and current I_{ss} flows through M1 & M3;
M3 - M4 current mirror $\Rightarrow$ I_{ss} is drawn through C_C

A constant current I_{ss} flowing through C_C generates a voltage ramp whose slope is

$$\frac{\Delta V}{\Delta t} = \frac{I_{ss}}{C_C}$$

Voltage at node 1 fixed because of M6
$\Rightarrow$ V_o increases as a ramp voltage

The 5V input signal drives the input-stage out of its linear region of operation (i.e. small-signal). The circuit operates nonlinearly and therefore we cannot expect a linear analysis to predict correct operation.

For a large negative input step, M2 is heavily on, M1 cuts off
$\Rightarrow$ M3-M4 current mirror is off
$\Rightarrow$ current I_{ss} flows through C_c

Node 1 is fixed by M6 $\Rightarrow$ V_o is a negative ramp of slope $\frac{I_{SS}}{C_C}$

The slew rate (SR) $= \frac{I_{SS}}{C_C}$

Relationship between SR & Unity Gain BW (UGBW)

$$\omega_u = \frac{g_{m1}}{C_C}$$

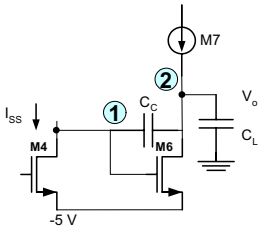
$$SR = \frac{I_{ss}}{C_C} = \frac{I_{ss}}{g_{m1}} \cdot \frac{g_{m1}}{C_C} = \frac{I_{ss}}{g_{m1}} \omega_u$$

$$\therefore \quad \frac{SR}{\omega_u} = \frac{I_{ss}}{g_{m1}} = \frac{I_{ss}}{2 I_D / (V_{GS} - V_T)} = V_{GS} - V_T$$

Since $I_{ss} = 2 I_D$

What about C_L?
When C_L is large, the slew rate could be determined by C_L.

Positive step at input
$\Rightarrow$ C_L is charging up
Current to charge up C_L is only I_{D7} - I_{SS} since I_{SS} goes to C_C.



V_1 drops so current through M6 is reduced $\Rightarrow$ I_{D7} - I_{SS} is available to charge C_L.

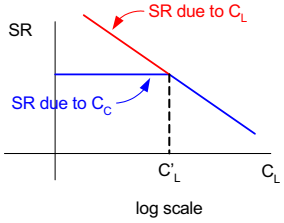
$$\therefore \quad SR_L = \frac{\Delta V}{\Delta t} = \frac{I_{D7} - I_{SS}}{C_L}$$

Negative step at input
M6 can discharge C_L when it is overdriven so this is not a problem.

At C_L' : $\frac{I_{D7} - I_{SS}}{C_L'} = \frac{I_{SS}}{C_C}$

or $C_L' = \frac{I_{D7} - I_{SS}}{I_{SS}} C_C$

$$= \left(\frac{I_{D7}}{I_{SS}} - 1 \right) C_C$$



Usually would like SR to be independent of C_L, since C_L is not a design parameter.

$\therefore$ Take $SR_L > SR$

or $\frac{I_{D7} - I_{SS}}{C_L} > \frac{I_{SS}}{C_C}$

or $I_{D7} > I_{SS} + \frac{C_L}{C_C} I_{SS}$

$$\Rightarrow I_{D7} > I_{SS} \left(1 + \frac{C_L}{C_C} \right)$$

How to improve Slew Rate?

$$SR = \frac{I_{SS}}{C_C}$$

$\Rightarrow$ increase I_{SS} and/or decrease C_C.

Increasing I_{SS} increases power dissipation
$\Rightarrow$ use class AB input stage
- low dc current
- under transient conditions current for charging C_C can be significantly increased.

Circuit can deliver large positive and negative currents to charge C_C or C_L and may not display slew rate limiting. We will look at one such circuit later.

Key Points

- $SR = \frac{I_{SS}}{C_C} = \frac{I_{SS}}{g_{m1}} \omega_u$
- $\frac{SR}{\omega_u} = \frac{I_{SS}}{g_{m1}} = \frac{I_{SS}}{I_{SS} / (V_{GS} - V_T)_1} = (V_{GS} - V_T)_1$

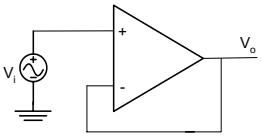
"Full-power" bandwidth

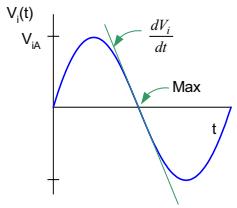
Slew-rate limitations also affect performance of the circuit when handling large sinusoidal signals at higher frequencies.

$$V_i = V_{iA}\sin(\omega t)$$

$$\Rightarrow \frac{dV_i}{dt} = \omega V_{iA}\cos(\omega t)$$

$$\therefore \left.\frac{dV_i}{dt}\right|_{max} = \omega V_{iA}$$

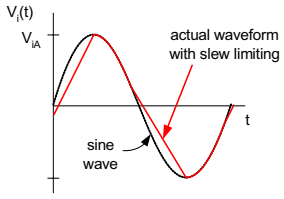




For $\left.\frac{dV_i}{dt}\right|_{max} < SR$, the output will follow input. However, for larger values waveform distortion will occur.

Since $\left.\frac{dV_i}{dt}\right|_{max} \propto \omega$

$\Rightarrow$ slew limiting will occur as the frequency is increased when $V_{iA}=V_{DD}$



The frequency at which this occurs is the "full-power" bandwidth

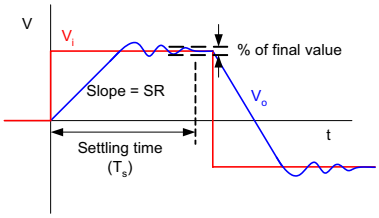
$$\omega_{fP} = \frac{SR}{V_{iA}}$$

Example

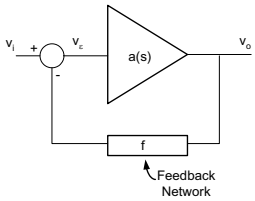
V_{DD}=5 V; SR=1 V/μs $\Rightarrow$ $\omega_{fP} = \frac{10^6}{5} rad/\sec$

$\therefore$ f_{fP}=31.8 kHz (full-power bandwidth)

Settling time



Stability of feedback amplifiers



If the amplifier is represented by a single pole transfer function

$$\Rightarrow a(s) = \frac{a_o}{1-\frac{s}{P_1}}$$

a_0 = low frequency gain
P_1 = pole frequency in radians/sec

Assume a purely resistive feedback path $\Rightarrow$ f constant

$$V_o = V_e a(s), \quad V_e = V_i - fV_o$$

$$\therefore A(s) = \frac{V_o}{V_i} = \frac{a(s)}{1+a(s)f} = \frac{a(s)}{1+T(s)}$$

where T(s) = a(s)f is the loop gain

$$A(s) = \frac{a_o/(1-s/P_1)}{1+\frac{a_o}{(1-s/P_1)}f}$$

$$= \frac{a_o}{1-\frac{s}{P_1}+a_o f} = \frac{a_o}{(1+a_o f)-\frac{s}{P_1}}$$

$$= \frac{a_o}{1+a_o f}\frac{1}{1-\frac{s}{P_1}\cdot\frac{1}{1+a_o f}}$$

The low-frequency closed-loop gain is

$$A_o = \frac{a_o}{1+a_o f} = \frac{a_o}{1+T_o}$$

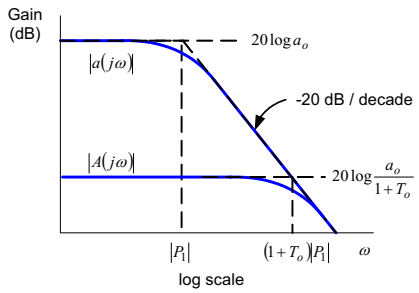
where $T_o=a_o f$ is the low-frequency loop gain.

The pole frequency for the closed-loop system is $P_1(1+a_o f)$

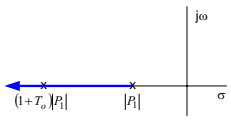
$\Rightarrow \omega_{-3dB} = |P_1|\,(1+a_o f) = |P_1|\,(1+T_o)$

Remarks

- The gain a_o has been reduced by a factor $1+T_o$
- The bandwidth has been increased by $(1+T_o)$
- $Gain \times BW = a_o|P_1| = \frac{a_o}{1+T_o}\cdot|P_1|(1+T_o)$ is a constant.
- Designer can use negative feedback to trade gain for bandwidth.



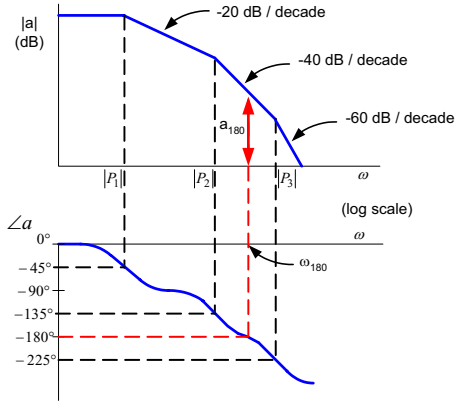
Gain curves for any T_o are contained in an envelope bounded by curve of $|a(j\omega)|$



Consider a 3-pole transfer function typical of many op amps before compensation.

$$a(s) = \frac{a_o}{\left(1-\frac{s}{P_1}\right)\left(1-\frac{s}{P_2}\right)\left(1-\frac{s}{P_3}\right)}$$

Bode plots



Consider a(s) in a feedback loop with f constant
∴ T(jω) = a(jω)f and will have same frequency variation as a(jω).

For a system to be stable all poles must be in the left-half plane.

$$A(j\omega) = \frac{a(j\omega)}{1+a(j\omega)f}$$

at ω_{180} $\quad A(j\omega_{180}) = \frac{a_{180}\angle 180}{1+a_{180}\angle 180\, f} = \frac{a_{180}\angle 180}{1-a_{180}f}$

If $T = a_{180}f = 1$ then $A(j\omega_{180}) \to \infty$

$\Rightarrow$ unstable

Remark
If |T(jω)| > 1 at the frequency where ∠T(jω) = -180°, then the amplifier is unstable (Linear system feedback theory)

There are two measures of stability: Phase Margin and Gain margin. Phase Margin is the more common specification.

Phase Margin = 180° + ∠T(jω) at frequency where |T(jω)| = 1. Must be > 0° for stability.

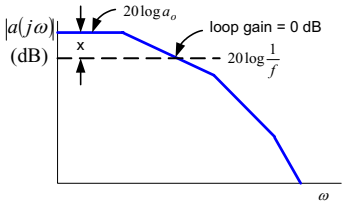
Gain Margin the value of T(jω) in dB at the frequency where ∠T(jω) = -180°. Must be < 0 dB for stability.

How do we determine where |T(jω)| = 0 dB given the magnitude Bode plot of a(jω)?

Consider $x = 20\log|a(j\omega)f| = 20\log|a(j\omega)| + 20\log f$

$$= 20\log|a(j\omega)| - 20\log\frac{1}{f}$$

The vertical distance between the curve 20log|a(jω)| and the line 20log(1/f) is a direct measure of the loop-gain magnitude in dBs.

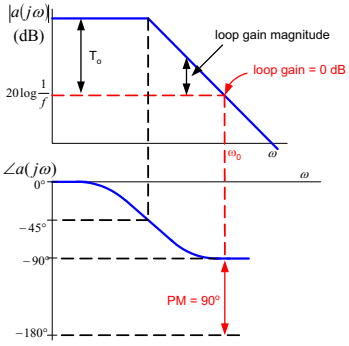


Remarks

- the point where 20log |a(jω)| intersects the line 20log(1/f) is the point where loop-gain magnitude is unity or 0-dB
- Can take the curve |a(jω)| as a curve for |T(jω)| if 20log(1/f) is taken as the zero axis.
- 20log(1/f) ≅ 20logA_o i.e. the low-frequency gain in dB

because $A_o = \frac{a_o}{1+a_o f} \cong \frac{1}{f}$ if $a_o f >> 1$

Consider the single-pole example:



For this case PM=90° and this is a very stable amplifier. A typical lower value for PM is 45°; 60° is more common.

Case 1 PM=45°; f real & constant
$\Rightarrow \angle T(j\omega_o) = -135$
where ω_o is the frequency for which $|T(j\omega_o)| = 1$

$$|T(j\omega_o)| = |a(j\omega_o)f| = 1 \quad \Rightarrow \quad |a(j\omega_o)| = \frac{1}{f}$$

$$A(j\omega) = \frac{a(j\omega)}{1+T(j\omega)}$$

at ω_o : $\quad T(j\omega) = 1\angle -135° = 1e^{-j135°}$

$$\therefore \quad A(j\omega_o) = \frac{a(j\omega_o)}{1+e^{-j135°}} = \frac{a(j\omega_o)}{1-0.7-0.7j} = \frac{a(j\omega_o)}{0.3-0.7j}$$

$$(\sqrt{0.58} = 0.76)$$

$$\therefore \quad |A(j\omega_o)| = \frac{|a(j\omega_o)|}{0.76} = \frac{1.3}{f} \cong 1.3A_o$$

At frequency ω_o, $|T(j\omega_o)| = 1$. This is the point at which the basic amplifier has a -3dB frequency (single-pole amplifier). However, in this case there is a 1.3x of peaking above the low-frequency gain.

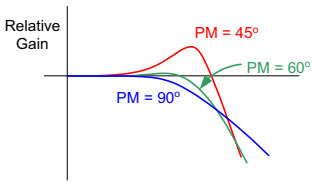
Case 2 PM = 60°
$\Rightarrow \angle T(j\omega_o) = -120°$, $\quad |T(j\omega_o)| = 1$

$$\therefore \quad |A(j\omega_o)| = \frac{1}{f}\frac{1}{|1+e^{-j120°}|} = \frac{1}{f}\frac{1}{|1-j0.866-0.5|}$$

$$= \frac{1}{f(1)} = \frac{1}{f}$$

Case 3 PM = 90°

$$|A(j\omega_o)| = \frac{0.7}{f}$$



Peaking of gain for PM < 60°

Example 1

The loop-gain of a feedback system has two poles $-\omega_1$ & $-5\,\omega_1$. Find the dc gain of the loop-gain for a phase-margin of 60°.

$$T(j\omega) = \frac{T_o}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{5\omega_1}\right)}$$

For phase margin: $|T(j\omega_o)| = 1$ when $\angle T(j\omega_o) = -120°$

$$\angle T(j\omega_o) = -\tan^{-1}\frac{\omega_o}{\omega_1} - \tan^{-1}\frac{\omega_o}{5\omega_1} = -120°$$

$$\Rightarrow \tan\left(\tan^{-1}\frac{\omega_o}{\omega_1} + \tan^{-1}\frac{\omega_o}{5\omega_1}\right) = \tan 120° = -1.732$$

$$\tan(A+B) = \frac{\tan(A)+\tan(B)}{1-\tan(A)\tan(B)}$$

$$\therefore \quad \frac{\frac{\omega_o}{\omega_1} + \frac{\omega_o}{5\omega_1}}{1 - \left(\frac{\omega_o}{\omega_1}\right)\left(\frac{\omega_o}{5\omega_1}\right)} = -1.732$$

Let $x = \frac{\omega_o}{\omega_1} \quad \Rightarrow \quad \frac{x + \frac{x}{5}}{1 - x^2/5} = -1.732$

$$\frac{6x}{5 - x^2} = -1.732$$

$$\text{or} \quad x^2 - 5 = \frac{6x}{1.732} = 3.464x$$

$$x = \frac{3.464 \pm \sqrt{(3.464)^2 + 20}}{2} = 4.56$$

Since the value of x>0

$$\frac{\omega_o}{\omega_1} = 4.56$$

Check: $\angle T(j\omega_o) = -\tan^{-1} 4.56 - \tan^{-1}\frac{4.56}{5} \cong -120°$

Now $|T(j\omega_o)| = 1 \Rightarrow \frac{T_o}{\sqrt{1+\left(\frac{\omega_o}{\omega_1}\right)^2}\sqrt{1+\left(\frac{\omega_o}{5\omega_1}\right)^2}} = 1$

$$\therefore \quad \frac{T_o}{\sqrt{1+(4.56)^2}\sqrt{1+\left(\frac{4.56}{5}\right)^2}} = 1 \Rightarrow T_o = 6.3$$

$\therefore$ dc gain of the loop-gain is 6.3.

Example 2

At what value of T_o will system become unstable.

$|T(j\omega_x)| = 1$ when $\angle T(j\omega_x) = -180°$

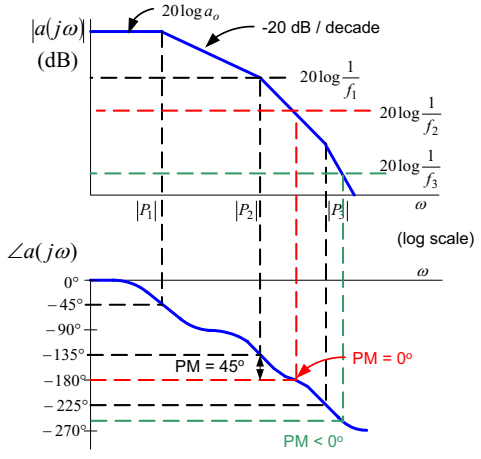
$\angle T(j\omega) = -180°$ as $\omega \to \infty$

$\therefore$ system is stable for finite values of T_o

Compensation

The process of making an amplifier stable that would otherwise be unstable in a feedback configuration.

Consider the Bode plots shown below:



For a feedback factor f_1, phase margin = 45°

f_2, " " = 0°

f_3, " " < 0°

Thus the amplifier will be unstable with a loop gain larger than $a_o f_2$; otherwise need <u>compensation</u>.

How do we make this amplifier stable?

<u>Observation</u>

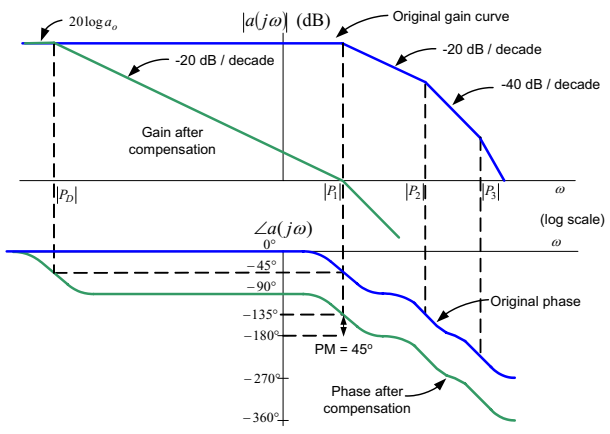
For a feedback factor of f_3 the magnitude of the loop-gain becomes unity (0 dB) well below -180°. So we should make the gain go to unity <u>before</u> the phase crosses -180°.

One solution

Introduce a dominant pole P_D at a sufficiently low frequency such that the gain rolls off and crosses 0 dB before the phase reaches 180°.

<u>Remarks</u>

1) This reduces the bandwidth of the amplifier. The process is known as narrow banding.
2) The most difficult case to compensate is for f=1.



If P_D is chosen so that |a(jω)| = 1 at the frequency $|P_1|$ then the phase margin is 45° as shown.

$$a(j\omega) = \frac{a_o}{\left(1+j\frac{\omega}{|P_D|}\right)\left(1+j\frac{\omega}{|P_1|}\right)\left(1+j\frac{\omega}{|P_2|}\right)\left(1+j\frac{\omega}{|P_3|}\right)}$$

The amplifier is now stable in a unity-gain or other feedback configurations. The original amplifier was unstable in a unity-gain feedback.

Remarks

- The basic amplifier has a UGBW of only $|P_1|$ which is much less than before.
- Loop gain begins to diminish at $|P_D|$ and all benefits due to feedback diminish.

Example

$$a_o = 5000;$$

$$-\frac{P_1}{2\pi} = 300kHz, \quad -\frac{P_2}{2\pi} = 2MHz, \quad -\frac{P_3}{2\pi} = 25MHz.$$

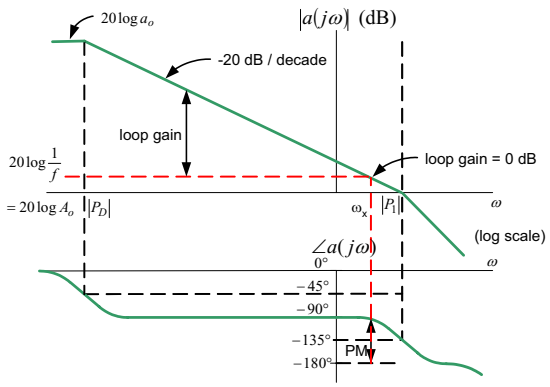
Find $|P_D|$ to compensate the amplifier for f=1 & PM=45°.

$$\boldsymbol{PM = 45° \Rightarrow UGBW = |P_1|}$$

$$\boldsymbol{GBW = a_o|P_D| = 1\cdot|P_1| \Rightarrow |P_D| = \frac{1}{a_o}|P_1|}$$

$$\boldsymbol{f_D = \frac{|P_D|}{2\pi} = \frac{1}{5000}(300K) = 60Hz}$$

Now consider the amplifier that we compensated for f=1, in a feedback arrangement with f<1.



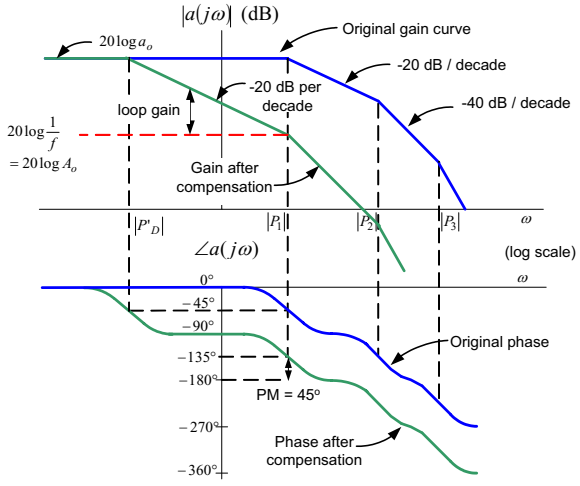
$|T(j\omega)| = 1$ at $\omega = \omega_x \Rightarrow \omega_{-3dB} = \omega_x$

i.e. bandwidth is being wasted. The circuit has more compensation than needed because PM ≅ 90°.

Remark

- Optimum bandwidth can be achieved in circuits if compensation is added by the user. Gain can be tailored for higher bandwidths.

Add a pole $|P_D'|$ for a PM of 45° in a feedback configuration.



- frequency $|P_D'|$ >> $|P_D|$
- ω_{-3db} is $|P_1|$. For unity-gain compensation $\omega_x = \frac{|P_1|}{A_o}$
-
- For Large A_o the improvement is significant (in BW)

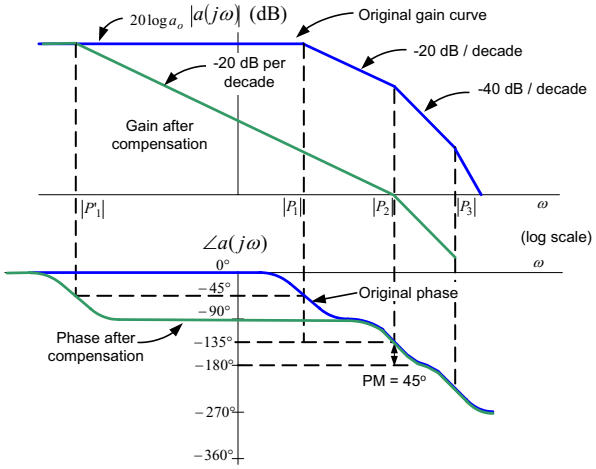
Observation

In the above compensation scheme an additional dominant pole was added to the amplifier. An efficient way to compensate the amplifier is to add capacitance to the circuit in a manner such

that $|P_1|$ (the dominant pole) is reduced & performs the compensation function.

⇒ pole-splitting compensation or Miller compensation.

Consider the situation in which only $|P_1|$ is reduced.

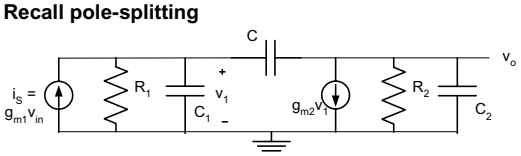


$|P_1'|$ causes gain to be unity at frequency $|P_2|$

⇒ phase margin = 45°

⇒ BW is $|P_2|$. i.e. substantial improvement compared to previous scheme since $|P_2| \approx 10|P_1|$ in practical amplifiers.

Recall pole-splitting



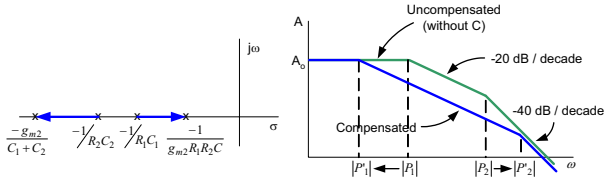
When C = 0: $$P_1 = \frac{1}{R_1 C_1}$$

$$P_2 = \frac{1}{R_2 C_2}$$

With the capacitor C

$$P_1 \cong -\frac{1}{g_{m2} R_1 R_2 C}$$

$$P_2 \cong -\frac{g_{m2} C}{C_1 C_2 + C(C_1 + C_2)}$$



Advantages of pole-splitting or Miller compensation

- Due to Miller multiplication, a small capacitor value yields an effective large capacitance (~$Cg_{m2}R_2$) ⇒ a low frequency pole
- The second pole is moved to a higher frequency ⇒ maximum unity-gain frequency is increased.

Disadvantage

- A right-half-plane zero is introduced. If g_{m2} is not high enough (as for MOSFETs) this can lead to some problems.

Let us now consider the zero

Recall

$$\frac{v_o}{i_s} = \frac{-(g_{m2} - sC)R_1 R_2}{1 + s[R_1C_1 + R_2C_2 + R_2C + R_1C(1 + g_{m2}R_2)] + s^2 R_2 R_1 (C_1C_2 + CC_1 + CC_2)}$$

$$P_1 \cong -\frac{1}{g_{m2} R_1 R_2 C}$$

$$P_2 \cong -\frac{g_{m2} C}{C_1 C_2 + C(C_1 + C_2)} \rightarrow -\frac{g_{m2}}{C_1 + C_2}$$

$$z = \frac{g_{m2}}{C}$$

For a one-pole roll off we had $\omega_u = \frac{g_{m1}}{C}$

Relative to ω_u $$\left|\frac{P_2}{\omega_u}\right| \cong \frac{g_{m2}}{g_{m1}} \frac{C}{C_1 + C_2}$$

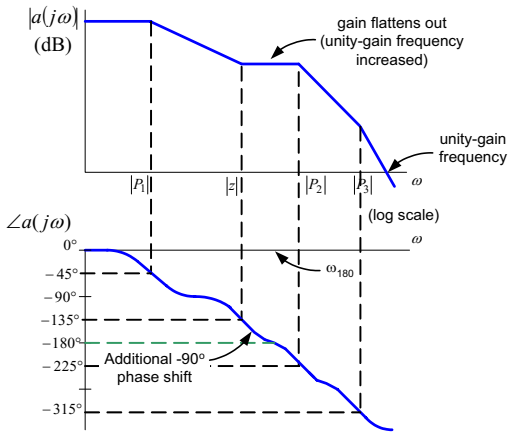
$$\left|\frac{z}{\omega_u}\right| = \frac{g_{m2}}{g_{m1}}$$

In MOS amplifiers g_{m1} & g_{m2} are similar.

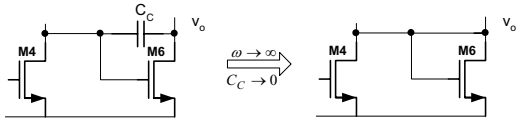
What happens if the break frequency caused by the zero is below the nominal unity-gain frequency of the amplifier?

- Zero flattens out gain
- Causes an additional 90° phase-shift

This is double trouble for stabilizing the amplifier.
⇒ increase ω_z or eliminate the zero!

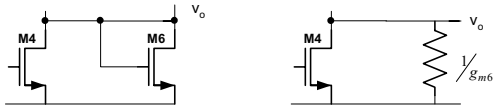


What is causing this zero?



Thus C provides a feed forward path that does not have the 180° phase shift of the common-source second gain stage. The gain path loses an inverting stage!

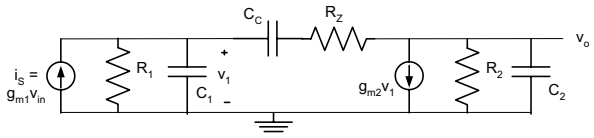
⇒ any feedback that was initially negative becomes positive resulting in oscillations (unstable)



The second stage is diode connected ⇒ a resistive load of $1/g_{m2}$ to the first stage.

$$\therefore \quad \frac{v_o}{v_i} = g_{m1} \cdot \frac{1}{g_{m2}}$$

A simpler approach is the use of nulling resistor in series with C.



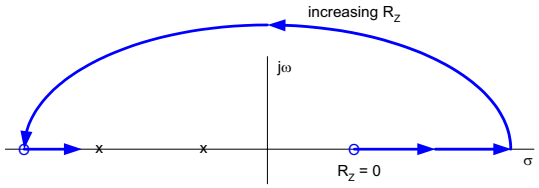
$|P_1|$ & $|P_2|$ are approximately the same as before but

$$z = \frac{1}{C_C\left(\frac{1}{g_{m2}} - R_Z\right)}$$

When $R_Z = \frac{1}{g_{m2}}$; $\quad z = \infty$ i.e. the zero is eliminated.

Remark

- The nulling resistor can be made larger to move the zero into the left half plane and improve the amplifier phase margin.



In fact, R_2 could also be used to cancel a pole.

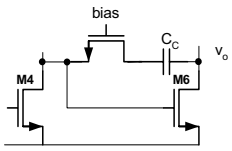
R2 is implemented as a MOSFET biased in non-saturation (linear region)

In non-saturation

$$g_d = k'\frac{W}{L}\left[(V_{GS} - V_T) - V_{DS}\right]$$

The resistor is biased with I=0.

i.e. $g_d = k'\frac{W}{L}(V_{GS} - V_T)$



Negative feedback

Benefits

- Stabilize gain of an amplifier against parameter changes in devices due to supply voltage variation, temperature changes, or device aging.
- Modify input and output impedances to suit needs.
  e.g. Voltage amplifier: large input impedance and small output impedance.
- Reduce distortion in amplifiers (the input-output transfer characteristics become more linear)
  - all audio amplifiers
- Increase bandwidth of circuits
  - widely used in broadband amplifiers.

Disadvantages

- Gain is reduced in almost direct proportion to other benefits (add extra gain stages)
- Feedback causes instability and there is a tendency for oscillation. An amplifier may become an oscillator!

Feedback Equation (Ideal)

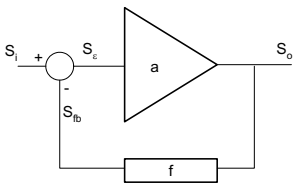
$$\frac{S_o}{S_i} = A = \frac{a}{1+af}$$

T = af = loop gain

A = closed-loop gain

$$A = \frac{a}{1+T}$$

For T >> 1 $\quad A \cong \frac{1}{f}$



Remarks

- Since the feedback network is usually formed from stable, passive elements, f is well defined and so is the overall amplifier gain.
- The feedback loop operates by forcing S_{fb} to be nearly equal S_i.

$$S_\varepsilon = S_i - S_{fb} = S_i - fS_o$$

$$= S_i - f\frac{a}{1+af}S_i = \frac{S_i}{1+af}$$

$$\therefore \quad \frac{S_\varepsilon}{S_i} = \frac{1}{1+af} = \frac{1}{1+T}$$

$$\frac{S_{fb}}{S_i} = f\frac{a}{1+af} = \frac{T}{1+T}$$

For T >> 1 $S_{fb} \cong S_i$; $S_\varepsilon << S_i$ i.e. the feedback loop minimizes the error signal S_ε.

Gain sensitivity

$$A = \frac{a}{1+af}$$

$$\therefore \quad \frac{dA}{da} = \frac{(1+af)-af}{(1+af)^2} = \frac{1}{(1+af)^2}$$

If a changes by Δa, then A changes by ΔA

$$\Delta A = \frac{\Delta a}{(1+af)^2}$$

$$\therefore \quad \frac{\Delta A}{A} = \frac{\Delta a}{(1+af)^2}\cdot\frac{1}{\frac{a}{(1+af)}} = \frac{\Delta a/a}{(1+af)} = \frac{\Delta a/a}{1+T}$$

$\therefore$ a fractional change in 'a' shows up as a fractional change in A reduced by (1+T)

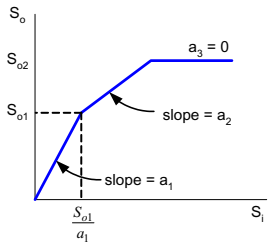
Example

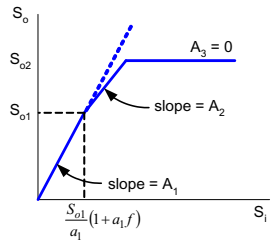
$$T = 100, \quad \frac{\Delta a}{a} = 10\%$$

$$\frac{\Delta A}{A} \cong \frac{10}{100}\% = 0.1\%$$

Effect on Distortion

- negative feedback keeps overall gain A approximately constant $\Rightarrow$ it should be effective in reducing distortion, because distortion is caused by changes in 'a' of the basic-amplifier transfer curves.



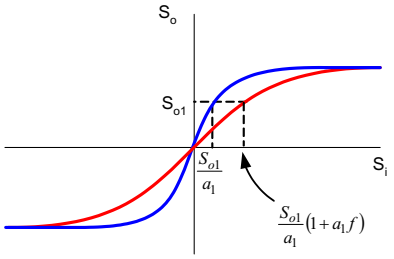


With feedback the slopes of transfer function curves are given by

$$A_1 = \frac{a_1}{1+a_1 f} = \frac{1}{f+\frac{1}{a_1}} \cong \frac{1}{f}$$

$$A_2 = \frac{a_2}{1+a_2 f} = \frac{1}{f+\frac{1}{a_2}} \cong \frac{1}{f}$$

$\Rightarrow$ the transfer characteristic will be much less nonlinear that the original amplifier.

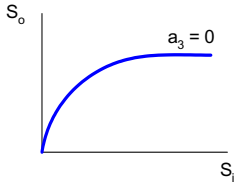


Negative feedback reduces the gain but improves the linearity.

Remark

When the output shows hard saturation then the gain is zero and negative feedback cannot improve the situation.

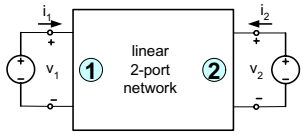
$$A_3 = \frac{a_3}{1+a_3 f} = \frac{0}{1} = 0$$



Review of 2-port representations

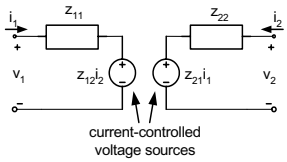
Linear 2-port

Currents flow into the network



z-parameters

$$v_i = z_{11} i_1 + z_{12} i_2$$
$$v_2 = z_{21} i_1 + z_{22} i_2$$
$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

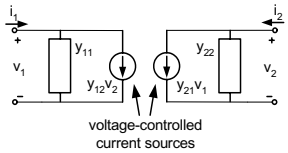


$$z_{11} = \left.\frac{v_1}{i_1}\right|_{i_2=0} \qquad z_{12} = \left.\frac{v_1}{i_2}\right|_{i_1=0}$$
$$z_{22} = \left.\frac{v_2}{i_2}\right|_{i_1=0} \qquad z_{21} = \left.\frac{v_2}{i_1}\right|_{i_2=0}$$

$\underline{v} = \underline{z}\,\underline{i}$

y-parameters

$$i_1 = y_{11} v_1 + y_{12} v_2$$
$$i_2 = y_{21} v_1 + y_{22} v_2$$
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

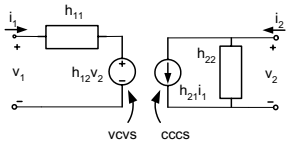


$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} \qquad y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0}$$
$$y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} \qquad y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}$$

$\underline{i} = \underline{y}\,\underline{v}$

h-parameters

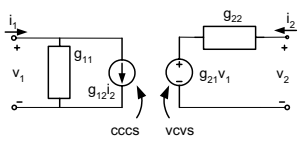
$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$
$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$$



$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0} \qquad h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0}$$
$$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0} \qquad h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0}$$

g-parameters

$$i_1 = g_{11} v_1 + g_{12} i_2$$
$$v_2 = g_{21} v_1 + g_{22} i_2$$
$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$$

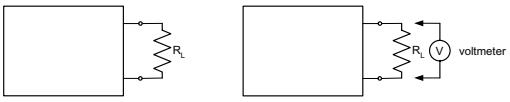


$$g_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} \qquad g_{12} = \left.\frac{i_1}{i_2}\right|_{v_1=0}$$
$$g_{22} = \left.\frac{v_2}{i_2}\right|_{v_1=0} \qquad g_{21} = \left.\frac{v_2}{v_1}\right|_{i_2=0}$$

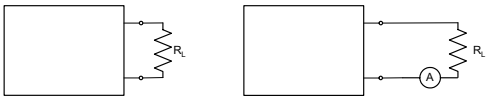
Feedback Configurations

At the output can sample either voltage or current

Voltage sampling $\Rightarrow$ sense output voltage. This is done by connecting a network in parallel (shunt)



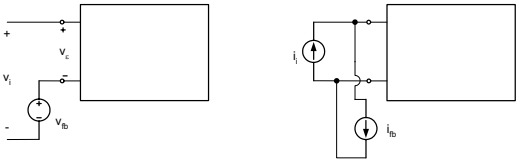
Current sampling $\Rightarrow$ sense output current. This is done by connecting a network in series.



At the input the feedback signal can be a voltage or current.

voltage feedback $\Rightarrow$ voltage in series

current feedback $\Rightarrow$ shunt



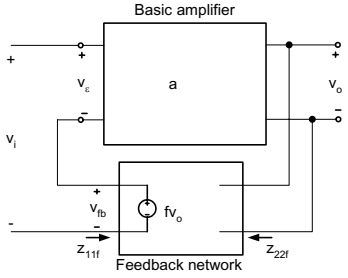
So four possible combinations:

Input	Output
Series	Shunt
Shunt	Shunt
Series	Series
Shunt	Series

Consider a voltage amplifier whose output voltage is to be stabilized with feedback.

- sample output voltage (shunt)
- feedback a voltage proportional to the output. This voltage is to be subtracted from the input voltage ⇒ in series with input

i.e. Series - Shunt feedback
↑ ↑
Input Output



Ideal case

$z_{22f} = \infty, \quad z_{11f} = 0;$ unilateral networks

$v_o = av_\varepsilon \;\; ; \;\; v_{fb} = fv_o$

$v_\varepsilon = v_i - v_{fb} = v_i - fv_o$

$\Rightarrow v_o = a(v_i - fv_o)$

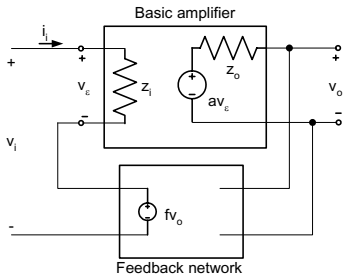
or $(1+af)v_o = av_i$

$$\frac{v_o}{v_i} = \frac{a}{1+af}$$ i.e. the ideal feedback equation

Transfer function that is stabilized is $\frac{v_o}{v_i}$

Effect on terminal impedances

Introduce terminal impedances in the amplifier z_i & z_o



$v_o = av_\varepsilon$

$v_i = v_\varepsilon + fv_o = v_\varepsilon + f(av_\varepsilon) = v_\varepsilon(1+af)$

Since $i_i = \frac{v_\varepsilon}{z_i} \quad \Rightarrow \quad i_i = \frac{v_i}{1+af}\frac{1}{z_i}$

$i_i = \frac{v_i}{z_i}\frac{1}{1+af}$ or $\frac{v_i}{i_i} = z_i(1+T)$

The input impedance with feedback is Z_i

$$Z_i = z_i(1+T)$$

Series feedback at the input always raises the input impedance by (1+T)

Example

z_i = 10kΩ, loop gain (T) = 1000
⇒ $Z_i \cong$ 10k(1000) = 10MΩ

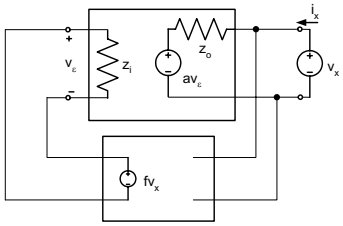
Output Impedance

$0 = v_\varepsilon + fv_x$ (input short)

and $i_x = \frac{v_x - av_\varepsilon}{z_o}$

$= \frac{v_x - a(-fv_x)}{z_o}$

$= \frac{v_x}{z_o}(1+af)$



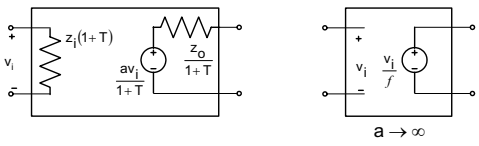
$\therefore \quad Z_o = \frac{v_x}{i_x} = \frac{z_o}{1+af} = \frac{z_o}{1+T}$

Shunt feedback always lowers output impedance by (1+T)

Remarks

1) Series-Shunt feedback results in an amplifier with high input impedance and low output impedance.
2) This is a desirable feature for "voltage-to-voltage" amplifiers
   - high Z_i to prevent loading of the source
   - low Z_o (like a good voltage source)

Equivalent 2-port representation



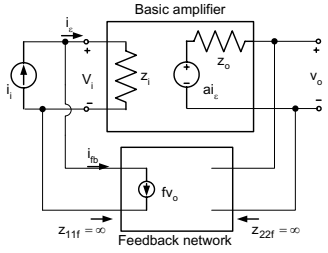
Transresistance amplifier

current input - voltage output

Output quantity to be stabilized is a voltage
⇒ feedback network is connected in shunt at the output

Input is a current
⇒ a current proportional to the output voltage has to be feedback in shunt with the input.

This is a shunt-shunt feedback



$a = \frac{v_o}{i_\varepsilon}$ where a is a transresistance

$i_{fb} = fv_o$ ⇒ f is a transconductance

Transfer function

$v_o = ai_\varepsilon$

$i_\varepsilon = i_i - i_{fb} = i_i - fv_o$

⇒ $v_o = a(i_i - fv_o)$

⇒ $\frac{v_o}{i_i} = \frac{a}{1+af}$ i.e. the ideal feedback eqn.

Note

'a' has dimensions of resistance
'f' has dimensions of conductance
T = af is dimensionless.

Remark

T will always be dimensionless.

Input impedance

$$i_\varepsilon = i_i - i_{fb} \quad \Rightarrow \quad i_\varepsilon = i_i(1 - f\frac{a}{1+af}) = \frac{i_i}{1+af}$$

$$Z_i = \frac{v_i}{i_i}$$

$$v_i = i_\varepsilon z_i = \frac{z_i}{1+af} i_i$$

$$\therefore Z_i = \frac{v_i}{i_i} = \frac{z_i}{1+af} = \frac{z_i}{1+T}$$

i.e. Z_i is reduced by a factor $(1+T)$

Output impedance

$$Z_o = \frac{z_o}{1+T}$$

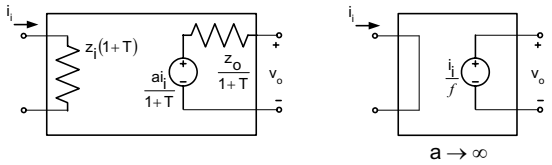
$\therefore$ Shunt-shunt feedback reduces both z_i & z_o

Remarks

1) Shunt-shunt feedback amplifiers take a current input and deliver a voltage output
2) To sense input current need a virtual short at the input (like an ammeter), which is what shunt-shunt feedback, produced.
3) For an ideal voltage source type of output need low output resistance, as is the case here.

Shunt-shunt feedback $\Rightarrow$ good current-to-voltage conversion
i.e. transresistance amplifier

Equivalent Circuits

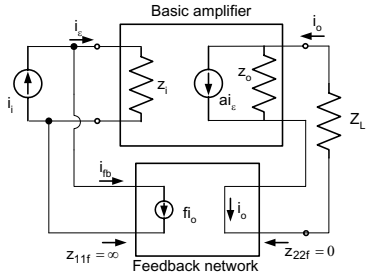


Current Amplifier

a current input & current output

$\Rightarrow$ sense current at the output i.e. connect feedback network in series with the output.
$\Rightarrow$ current feedback to the input in shunt.

shunt-series feedback

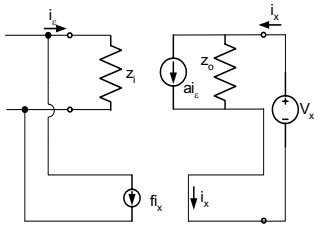


For $z_L << z_o$

$$\frac{i_o}{i_i} = \frac{a}{1+af}$$

$$Z_i = \frac{z_i}{1+T}$$

Output impedance



$$i_\varepsilon = -fi_x$$

$$i_x = ai_\varepsilon + \frac{v_x}{z_o}$$

$$\Rightarrow i_x = a(-fi_x) + \frac{v_x}{z_o}$$

$$(1+af)i_x = \frac{v_x}{z_o}$$

$$\Rightarrow Z_o = \frac{v_x}{i_x} = z_o(1+af) = z_o(1+T)$$

Remark

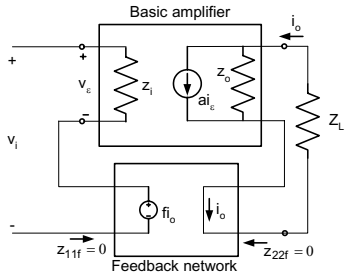
Approaches an ideal current amplifier. Low z_{in} & high z_{out}

Transconductance Amplifier

voltage input – current output

$\Rightarrow$ sense output current i.e. feedback network in series with the output.
$\Rightarrow$ voltage input, convert current to voltage and feedback in series to the input.

series-series feedback



'a' is a transconductance
'f' is a transresistance

$$\frac{i_o}{v_i} = \frac{a}{1+af} \quad \Rightarrow \text{ good transconductance amplifier}$$

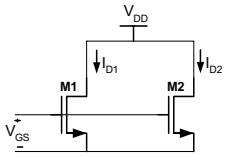
$$Z_i = z_i(1+T)$$

$$Z_o = z_o(1+T)$$

Matching in Transistor Current Sources

Goal

Generation of two or more current sources of identical values



However, there is a mismatch due to mismatches in W/L and V_T's

Noticing that

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS}-V_T)^2$$

$$\frac{\partial I_D}{\partial\left(\frac{W}{L}\right)} = \frac{I_D}{\left(\frac{W}{L}\right)} \quad and \quad \frac{\partial I_D}{\partial V_T} = -\frac{2I_D}{(V_{GS}-V_T)}$$

we get $\frac{\Delta I_D}{I_D} = \frac{\Delta\left(W/L\right)}{W/L} - \frac{2\Delta V_T}{V_{GS}-V_T}$

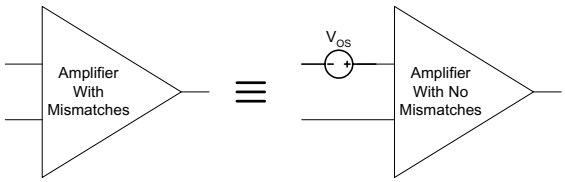
The first term is bias independent while the second term is bias dependent.

Remarks

- The second term can be reduced by using large V_{GS}-V_T
- Since V_T has a considerable gradient with distance across a wafer, care must be taken in biasing current sources from the same bias line when devices are physically separated by large distances

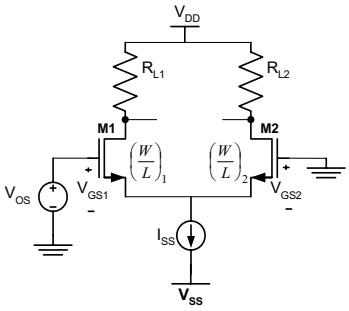
Input offset voltage

For MOS differential amplifiers the effect of mismatches on dc performance is represented by an input offset voltage



V_{OS} = differential input voltage that must be applied to drive the differential output voltage to zero. i.e. V_{id} for V_{od} = 0.

The predominate sources of offset are mismatches in W, L, V_T and R_L. The input offset voltage is a superposition of these different components.



$$V_{os} - V_{gs1} + V_{gs2} = 0$$

$$V_{os} = V_{gs1} - V_{gs2} = \left(V_{T1} + \sqrt{\frac{2I_{D1}}{K'\left(W/L\right)_1}}\right) - \left(V_{T2} + \sqrt{\frac{2I_{D2}}{K'\left(W/L\right)_2}}\right)$$

Define difference and average quantities

$$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2 \qquad \frac{W}{L} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$$

$$\Delta I_D = I_{D1} - I_{D2} \qquad I_D = \frac{1}{2}\left(I_{D1} + I_{D2}\right)$$

$$\Delta V_T = V_{T1} - V_{T2} \qquad V_T = \frac{1}{2}\left(V_{T1} + V_{T2}\right)$$

$$\Delta R_L = R_{L1} - R_{L2} \qquad R_L = \frac{1}{2}\left(R_{L1} + R_{L2}\right)$$

$$V_{os} = \left(V_T + \frac{\Delta V_T}{2}\right) - \left(V_T - \frac{\Delta V_T}{2}\right) + \sqrt{\frac{2\left(I_D + \frac{\Delta I_D}{2}\right)}{K'\left(W/L + \frac{\Delta W/L}{2}\right)}} - \sqrt{\frac{2\left(I_D - \frac{\Delta I_D}{2}\right)}{K'\left(W/L - \frac{\Delta W/L}{2}\right)}}$$

Note that V_{os} is in the form

$$g(x) = f(x + \Delta x/2, y + \Delta y/2, \ldots) - f(x - \Delta x/2, y - \Delta y/2, \ldots)$$

where $f = V_T + \sqrt{\frac{2I_D}{K'\left(W/L\right)}}$

$$g(x) = \frac{\partial f}{\partial x}\Delta x + \frac{\partial f}{\partial y}\Delta y + \ldots$$

Thus

$$V_{os} = \frac{\partial f}{\partial V_T}\Delta V_T + \frac{\partial f}{\partial I_D}\Delta I_D + \frac{\partial f}{\partial\left(W/L\right)}\Delta\left(W/L\right)$$

$$V_{os} = \Delta V_T + \frac{1}{2}\left(\frac{2I_D}{K'\left(W/L\right)}\right)^{-\frac{1}{2}}\frac{2}{K'\left(W/L\right)}\Delta I_D + \frac{1}{2}\left(\frac{2I_D}{K'}\right)^{-\frac{1}{2}}\frac{-2}{K'\left(W/L\right)^2}\Delta\left(W/L\right)$$

$$V_{os} = \Delta V_T + \frac{1}{2}\sqrt{\frac{2I_D}{K'\left(W/L\right)}}\left[\frac{\Delta I_D}{I_D} - \frac{\Delta\left(W/L\right)}{\left(W/L\right)}\right]$$

Now V_{od} = 0 so $\Delta\left(I_D R_L\right) = 0$

$$\Rightarrow R_L\Delta I_D + I_D\Delta R_L = 0$$

$$R_L\Delta I_D = -I_D\Delta R_L$$

$$\frac{\Delta I_D}{I_D} = -\frac{\Delta R_L}{R_L}$$

Remembering that

$$V_{GS} - V_T = \sqrt{\frac{2I_D}{K'\left(W/L\right)}} \quad \text{gives}$$

$$V_{os} = \Delta V_T + \frac{V_{GS}-V_T}{2}\left[-\frac{\Delta R_L}{R_L} - \frac{\Delta\left(W/L\right)}{\left(W/L\right)}\right]$$

Remark

For a given percentage mismatch in R_L and (W/L), the offset scales directly as (V_{GS}-V_T)

The ΔV_T component is independent of bias

V_{os} ~ 5 –15 mV for MOS

The signs of individual terms not significant since mismatch factors can be + or -.

Worst case offset occurs when the terms have signs such that the individual contributions add.

i.e. $V_{os}(worst\ \ case) = |\Delta V_T| + \frac{V_{GS}-V_T}{2}\left[\left|\frac{\Delta R_L}{R_L}\right| + \left|\frac{\Delta\left(W/L\right)}{\left(W/L\right)}\right|\right]$

Example

I_{SS} = 50μA, λ = 0, K' = 600 μA/V^2
W = 8μ, L = 100μ, V_T identical, R_L identical

worst case W/L mismatch = 2% $\Rightarrow \frac{\Delta\left(W/L\right)}{\left(W/L\right)} = 0.02$

$$V_{os} = \frac{V_{GS} - V_T}{2}\frac{\Delta\left(W/L\right)}{\left(W/L\right)}$$

$$V_{GS} - V_T = \sqrt{\frac{2I_D}{K'\left(W/L\right)}} = \sqrt{\frac{I_{SS}}{60\mu\left(8/100\right)}} = \sqrt{\frac{50\mu}{60\mu\left(8/100\right)}} = 3.23V$$

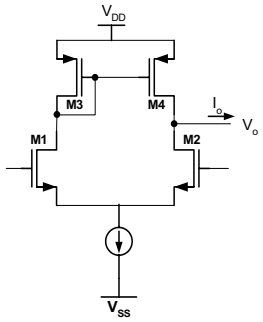
$$\therefore V_{os}(worst\ \ case) = \frac{3.23V}{2}(0.02) = 32mV$$

If in addition $\frac{\Delta R_L}{R_L} = 1\% = 0.01$ then

$$V_{os}(wc) = \frac{3.23V}{2}(0.02 + 0.01) = 48mV$$

Input offset voltage for SC-pair with active load

V_{os} = differential input voltage for which I_o = 0.



For this condition to be true

$$\frac{\Delta I_{D1-2}}{I_{D1-2}} = \frac{\Delta I_{D3-4}}{I_{D3-4}}$$

For a SC pair we have

$$V_{os} = V_{gs1} - V_{gs2}$$

$$V_{os} = \Delta V_{T1-2} + \frac{(V_{GS} - V_T)_{1-2}}{2}\left[-\frac{\Delta I_{D1-2}}{I_{D1-2}} - \frac{\Delta\left(W/L\right)_{1-2}}{\left(W/L\right)_{1-2}}\right]$$

From the previous current source mismatch analysis

$$\frac{\Delta I_{D3-4}}{I_{D3-4}} = \frac{\Delta\left(W/L\right)_{3-4}}{\left(W/L\right)_{3-4}} - \frac{2\Delta V_{T3-4}}{(V_{GS} - V_T)_{3-4}}$$

$$\therefore V_{os} = \Delta V_{T1-2} + \frac{(V_{GS} - V_T)_{1-2}}{2}\left[-\frac{\Delta\left(W/L\right)_{3-4}}{\left(W/L\right)_{3-4}} + \frac{2\Delta V_{T3-4}}{(V_{GS} - V_T)_{3-4}} - \frac{\Delta\left(W/L\right)_{1-2}}{\left(W/L\right)_{1-2}}\right]$$

$$V_{os} = \Delta V_{T1-2} + \Delta V_{T3-4}\frac{(V_{GS} - V_T)_{1-2}}{(V_{GS} - V_T)_{3-4}} - \frac{(V_{GS} - V_T)_{1-2}}{2}\left[-\frac{\Delta\left(W/L\right)_{3-4}}{\left(W/L\right)_{3-4}} + \frac{\Delta\left(W/L\right)_{1-2}}{\left(W/L\right)_{1-2}}\right]$$

now $(V_{GS} - V_T)_{1-2} = \frac{2I_D}{g_{m1}}$ *and* $(V_{GS} - V_T)_{3-4} = \frac{2I_D}{g_{m3}}$

$$\Rightarrow V_{os} = \underbrace{\Delta V_{T1-2}}_{\text{Term 1}} + \underbrace{\Delta V_{T3-4}\frac{g_{m3}}{g_{m1}}}_{\text{Term 2}} - \underbrace{\frac{(V_{GS} - V_T)_{1-2}}{2}\left[-\frac{\Delta\left(W/L\right)_{3-4}}{\left(W/L\right)_{3-4}} + \frac{\Delta\left(W/L\right)_{1-2}}{\left(W/L\right)_{1-2}}\right]}_{\text{Term 3}}$$

Term 1 is threshold mismatch of input transistors
Term 2 is threshold mismatch of load devices
Term 3 is W/L mismatches in input and load transistors

Remarks

- Term 2 is minimized by choosing W/L of load transistors so that g_{m3} is small w.r.t. g_{m1}
- Term 3 is minimized by operating the input transistors at low values of V_{GS}-V_T
- Term 1 is independent of the bias current as is the case for the simple SC pair