Advanced Computer Architecture
Bonus Assignment 1 — Caches and the Memory System

Instructions

- The assignment should be solved *individually*.
- Solutions should be properly *motivated*, a few short sentences is usually enough.
- Answer the questions in *your* own words. Copying answers from other sources, such as the text book, is not acceptable. You may quote other sources, in that case, make sure to include the source and say how you interpret the quoted text.
- Solutions should be given in *English* or *Swedish*. English is preferred.
- Solutions should be handed in *before* the deadline by:
  - Posting them in *Andreas Sembrant's* mailbox (house 1, floor 2).
  - Sending an email to `andreas.sembrant@it.uu.se`. The *answers should be in the message body*, solutions attached as Word documents, or similar, will be ignored. If you need to include graphics use one of the following formats: PNG, JPEG, SVG, PDF, EPS, PS
- Fill out and include this cover page when you hand in your solution. If you are submitting by email, make sure to include the same information in the email.
- Unreadable solutions will be treated as incorrect.
- You need to score at least 20 points to get a bonus point on the exam.

Deadline

Solutions handed in after the deadline specified on the course homepage will be marked on a best effort basis and will not result in any bonus on the exam.

Student

Name

Civic registration number (personnummer)

Email address

Date

1 Cache Design

You have already written your civic registration number (personnummer) on the cover page in the format *YyMmDd-XXXX*. Use the following formulas to calculate the parameters of your caches:

$$S = 32 * 2^d \text{ kB} \quad (1)$$

$$L = 32 * 2^D \text{ B} \quad (2)$$

$$A = 2 * 2^m \bmod 4 \quad (3)$$

$$W = 16 * 2^y \bmod 4 \text{ b} \quad (4)$$

1. Assume that you have a direct mapped cache of size S (Equation 1) with the line size L (Equation 2). The cache is physically indexed and tagged. The physical address is 50 bits, numbered from 0 to 49 (with 0 being the least significant bit). The machine has a word size of W bits (Equation 4) and the memory is byte-addressable.

   a. Write your personal values of the parameters S, L, A and W (along with the parameters y, d, D and m).

   b. Make a schematic drawing of the cache. (2)

   c. Describe which bits are used to index the cache, i.e. used to select the row in the cache. (1)

   d. Which bits are compared with the address tag? (1)

   e. Which bits are used to select a word from the selected cache line? (1)

1.1 Associative Cache

2. Now, assume that you have an A-way (Equation 3) set associative cache of size S (Equation 1) and cache line size L (Equation 2).

   a. Make a schematic drawing of the cache. (2)

   b. Describe which bits are used to index the cache, i.e. used to select the row in the cache. (1)

   c. Which bits are compared with the address tag? (1)

   d. Which bits are used to select the word to read from the selected cache line? (1)

2 More on Caches

3. Describe how the *LRU* and *RANDOM* replacement policies work. (2)

4. Why would a computer architect choose to implement:

   a. *LRU* instead of *RANDOM*? (1)

b. *RANDOM* instead of *LRU*? (1)

5. Explain when the following miss types occur and how they can be avoided:

   a. *Compulsory* misses (1)

   b. *Capacity* misses (1)

   c. *Conflict* misses (1)

3 Virtual Memory

6. Describe two reasons for implementing virtual memory. (2)

7. Give at least one reason why a computer system with virtual memory should have a TLB. (1)

8. What is the reach of a TLB with the page size 4 kB and 512 entries? (1)

9. What is the benefit of using a *virtual indexed* and *physically tagged* cache? Are there any problems? (2)

10. What is the benefit of using a *virtually indexed* and *virtually tagged* cache? Are there any problems? (2)