

IDF2012
INTEL DEVELOPER FORUM

Silicon Technology Leadership for the Mobility Era

Mark Bohr, Intel Senior Fellow

SPCS008

Sponsors of Tomorrow: 

Agenda

- Transistor Scaling Trends
- 32 nm SoC Technology
- 22 nm CPU Technology
- 22 nm SoC Technology

The PDF for this Session presentation is available from our Technical Session Catalog at the end of the day at:

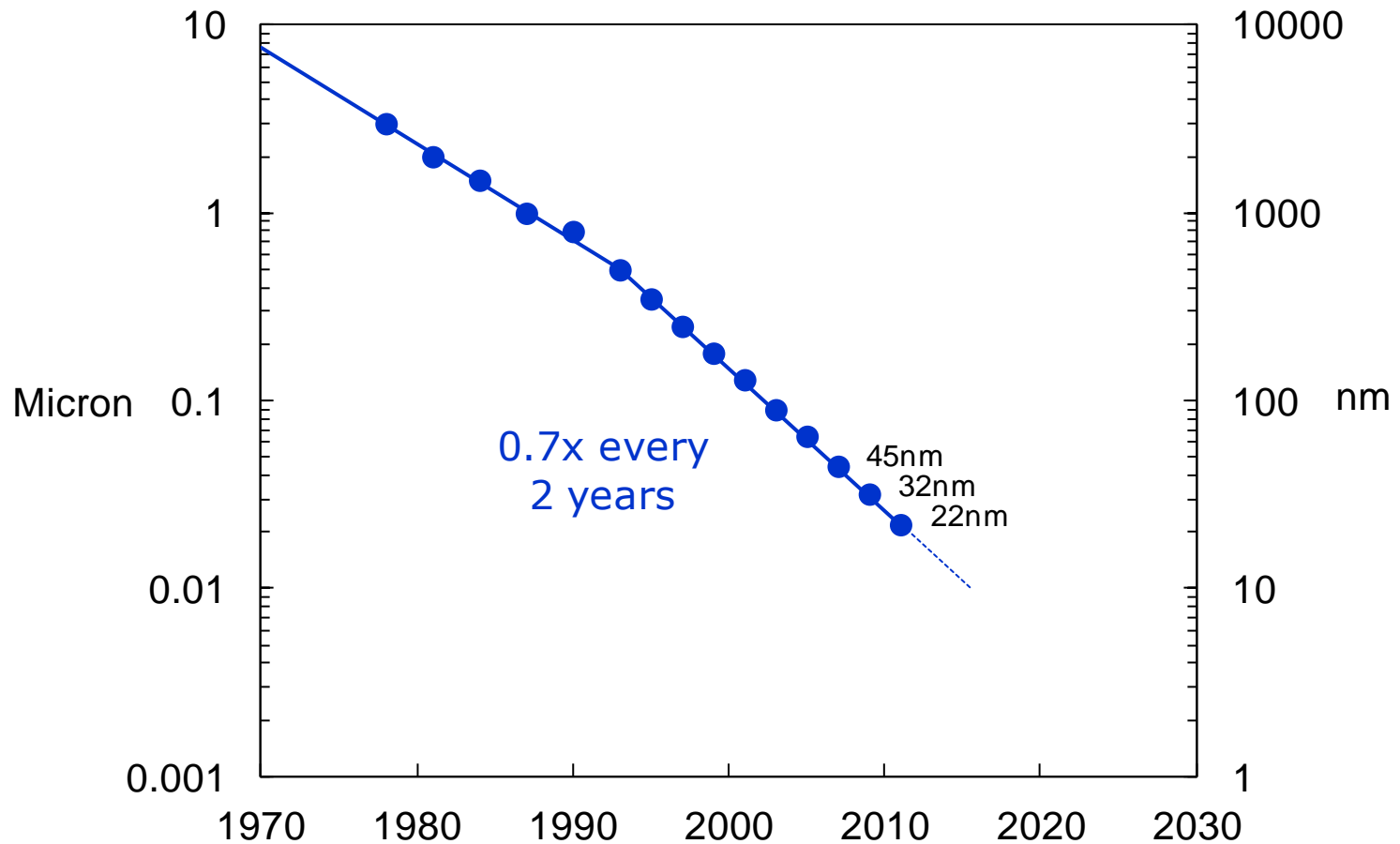
intel.com/go/idfsessions

URL is on top of Session Agenda Pages in Pocket Guide

Agenda

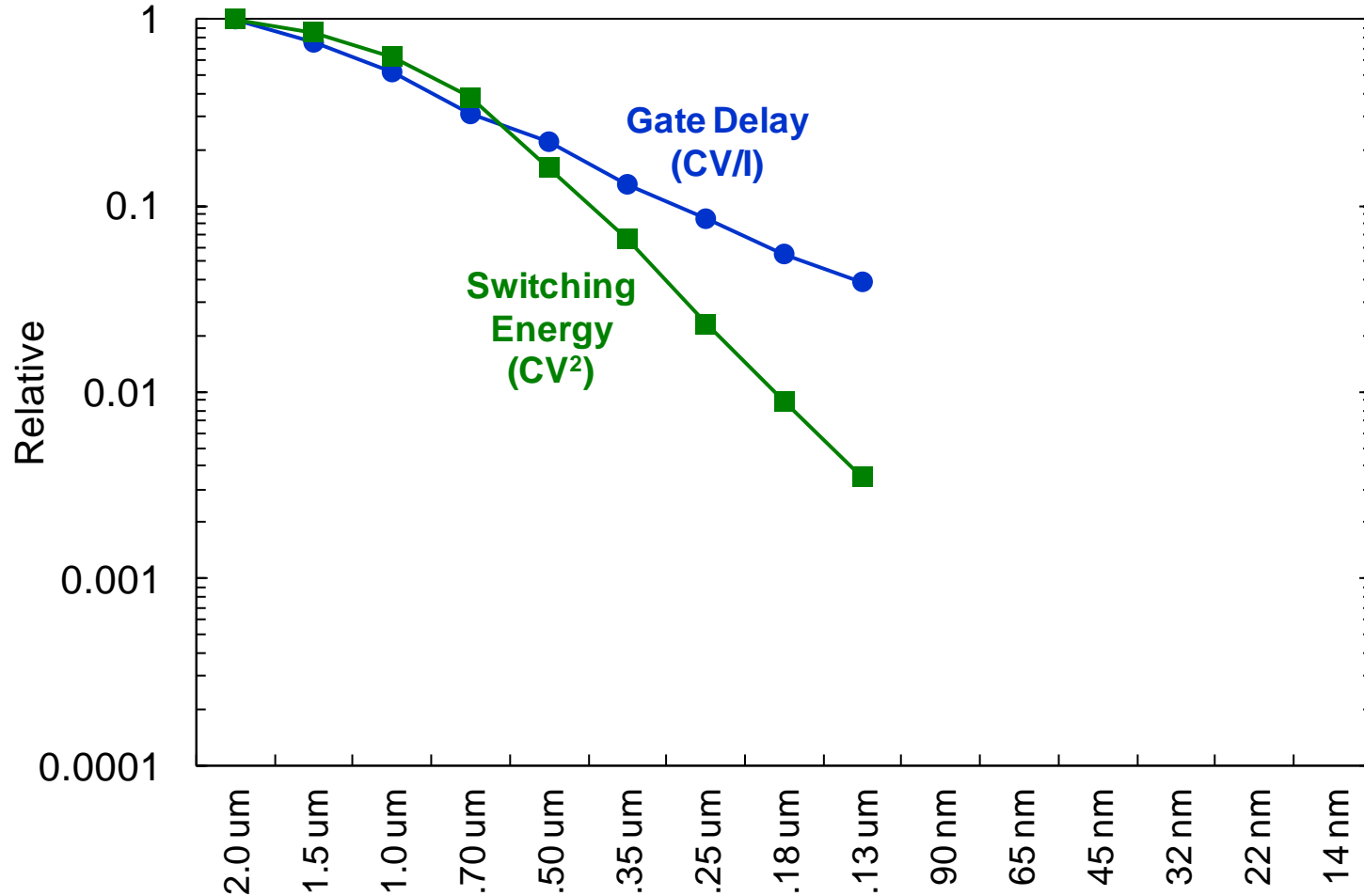
- Transistor Scaling Trends
- 32 nm SoC Technology
- 22 nm CPU Technology
- 22 nm SoC Technology

Transistor Scaling



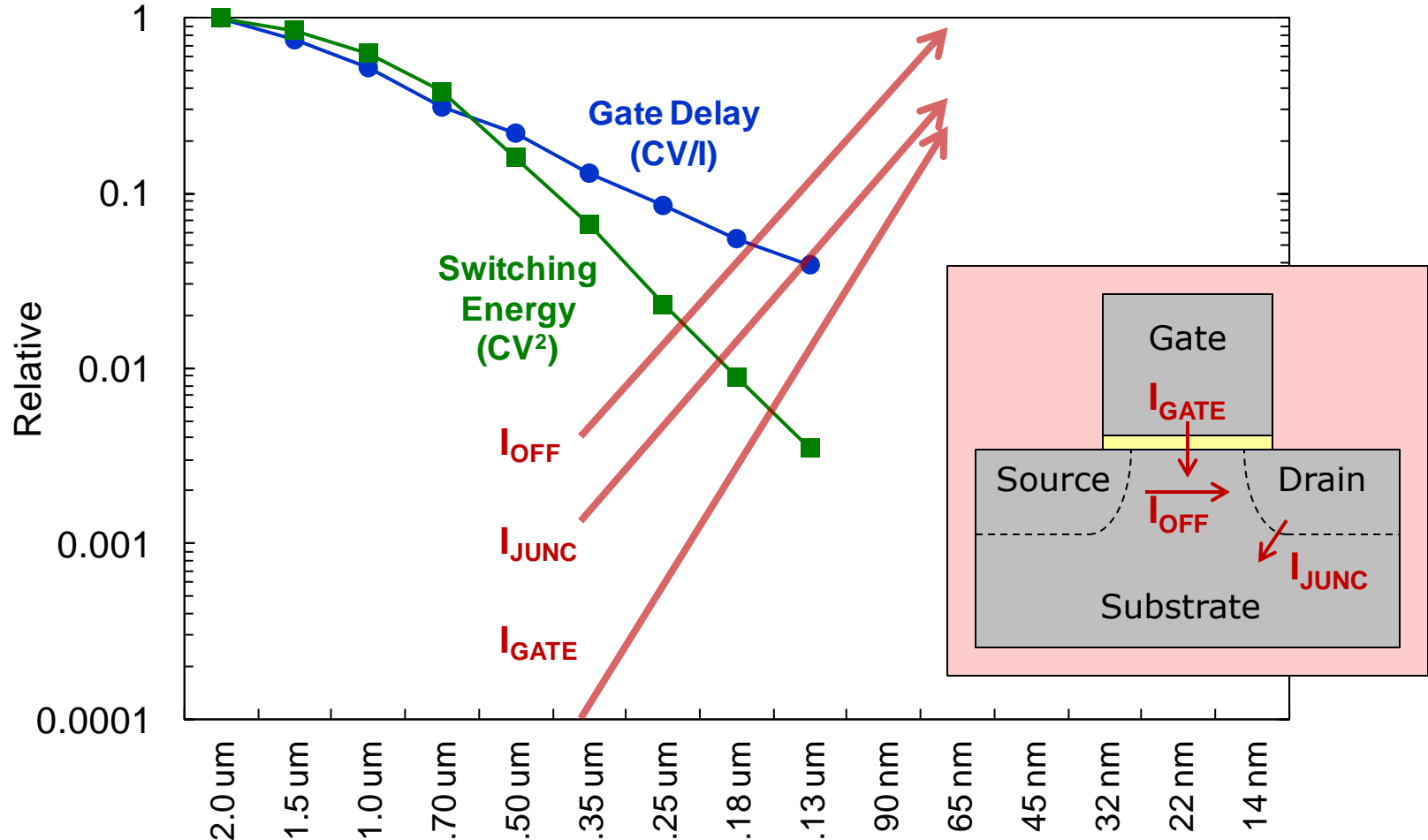
Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor

Transistor Performance and Power



"Classical" transistor scaling provided improvements in performance (gate delay) and active power (switching energy)

Transistor Performance and Power

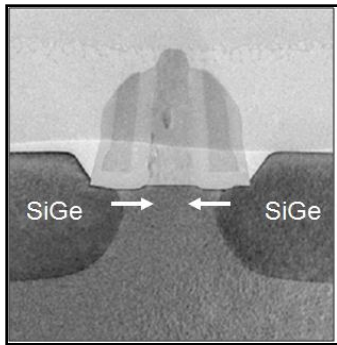


... but at the expense of increased leakage current

Non-Classical Scaling

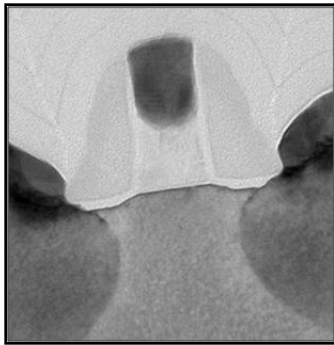
90 nm

2003



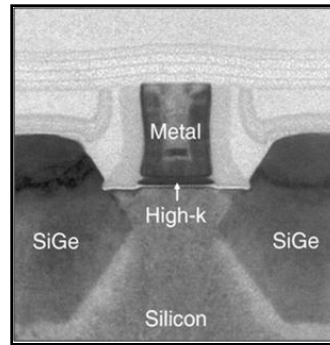
65 nm

2005



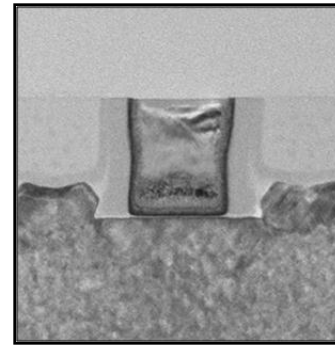
45 nm

2007



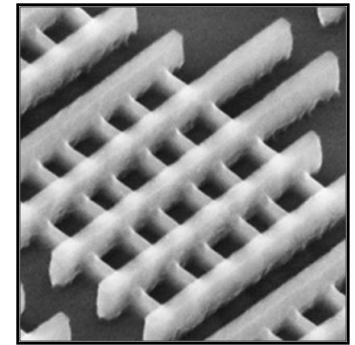
32 nm

2009



22 nm

2011



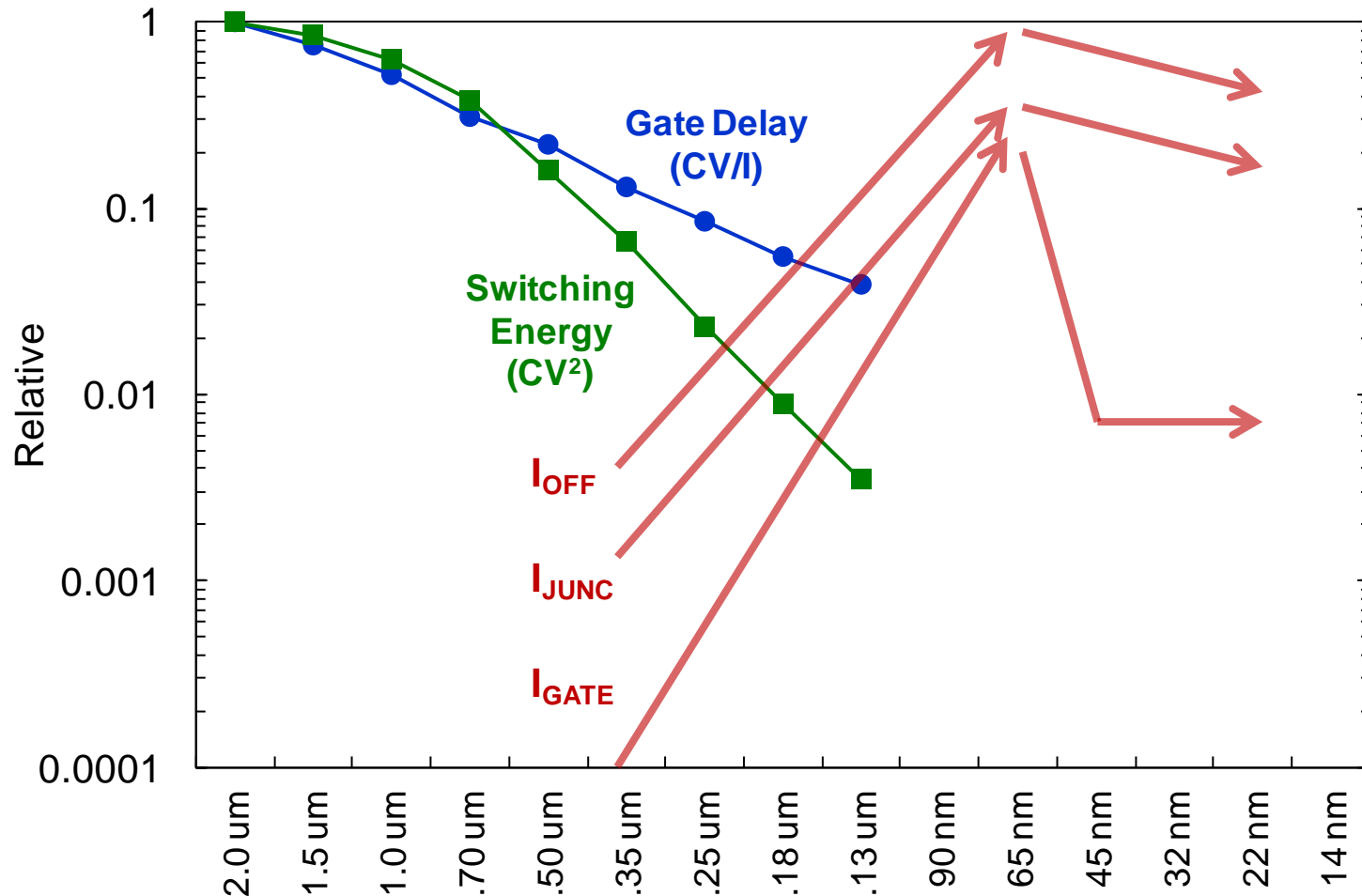
Strained Silicon

High-k Metal Gate

Tri-Gate

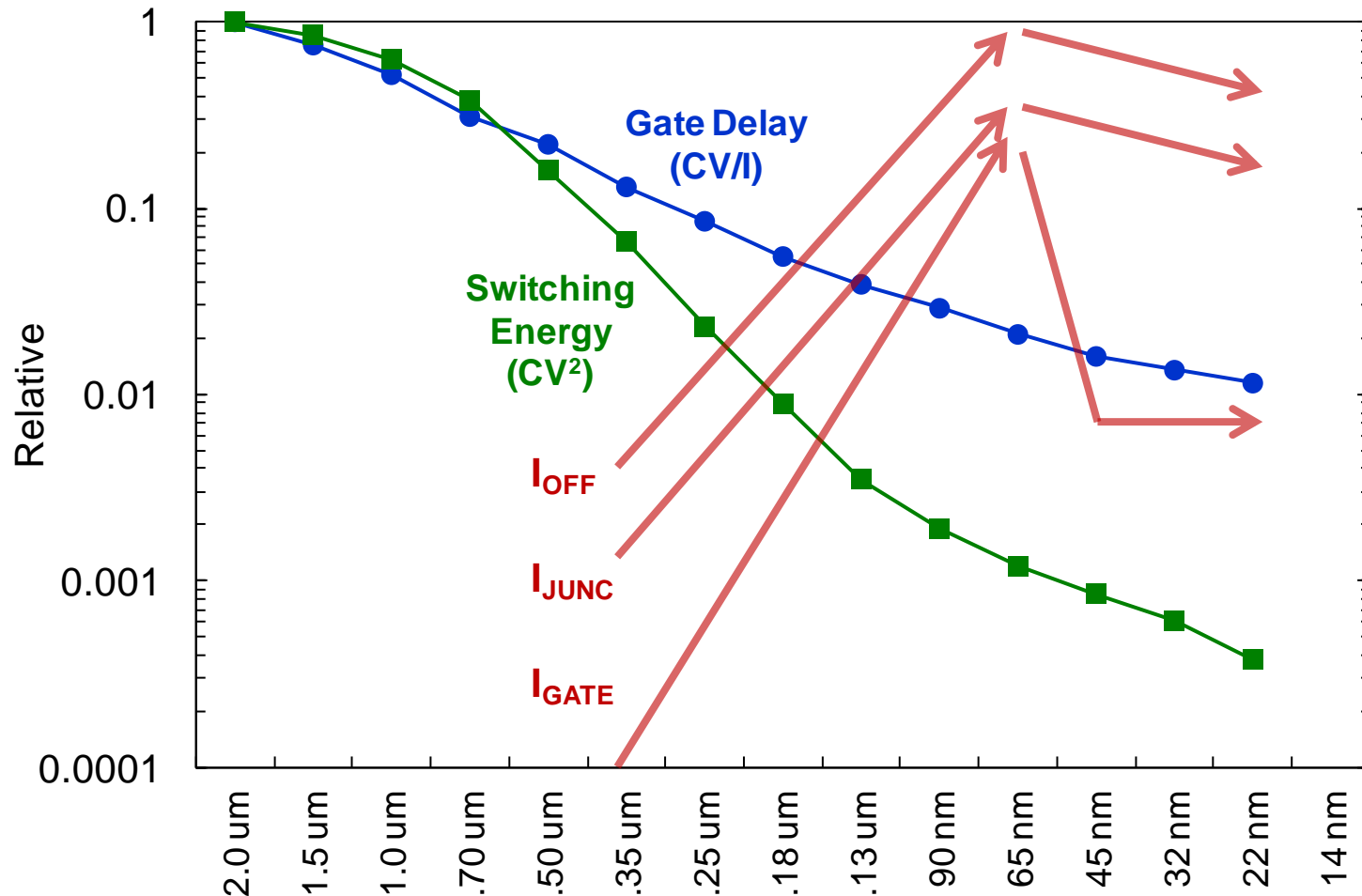
***Scaling now requires continual innovations
in transistor structure and materials***

Transistor Performance and Power



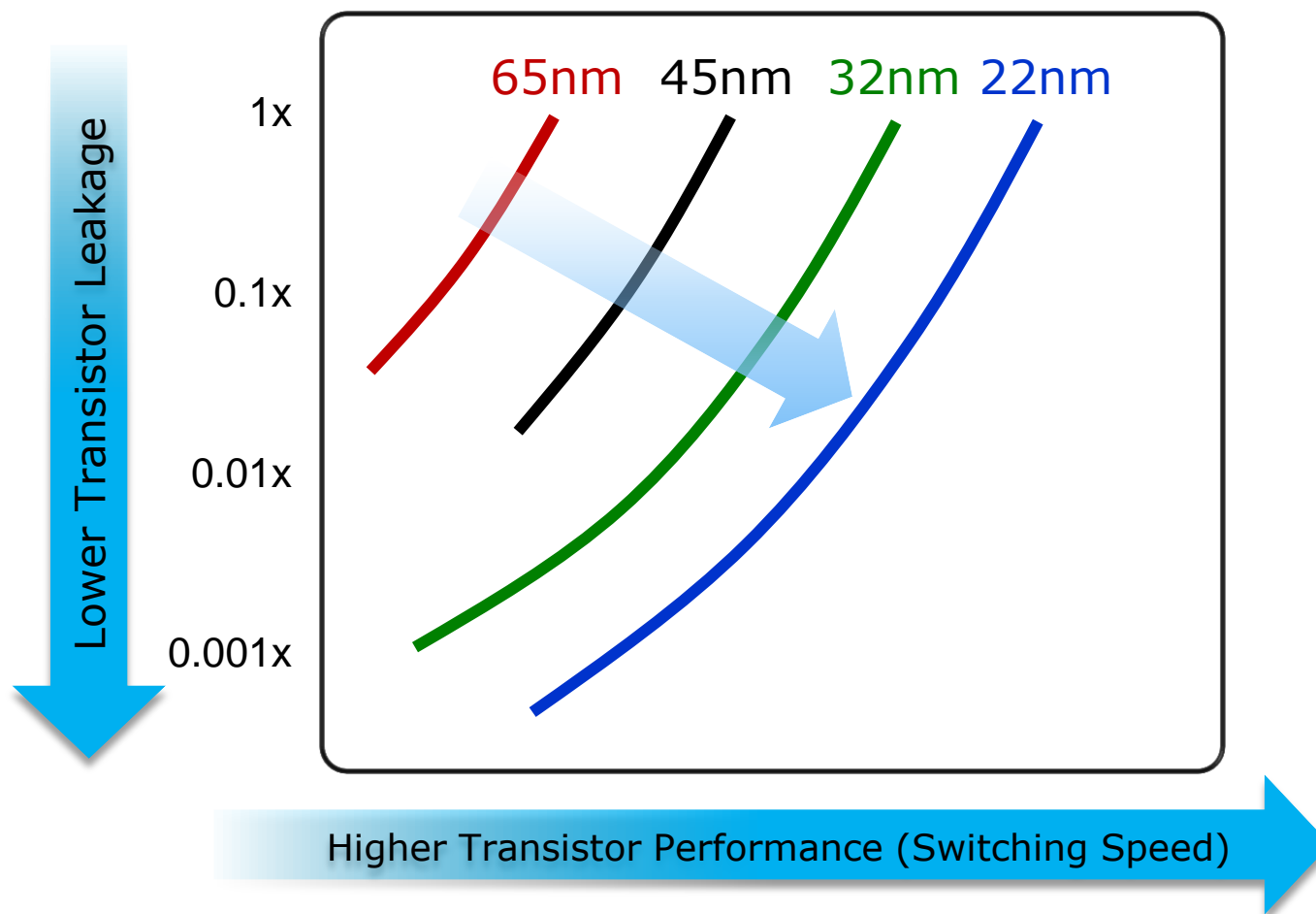
Transistor scaling now focuses on reducing leakage

Transistor Performance and Power



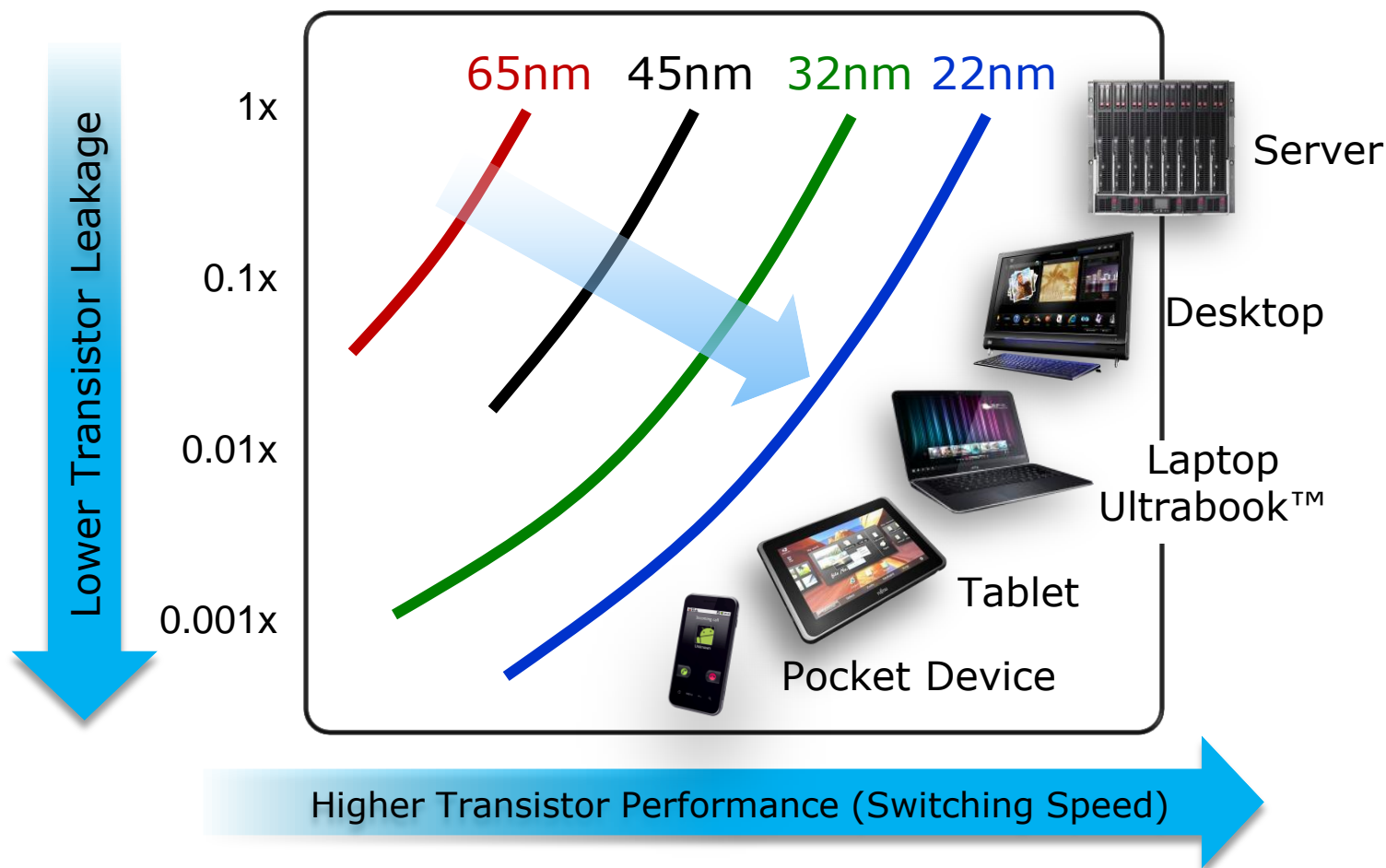
... and continues to improve performance and power

Transistor Performance vs. Leakage



Transistors now improve on both performance and leakage vectors

Transistor Performance vs. Leakage



Wider range of transistors to support a wider range of products

Intel® Technology Roadmap

	32 nm		22 nm		14 nm	
Name:	P1268	P1269	P1270	P1271	P1272	P1273
Products:	CPU	SoC	CPU	SoC	CPU	SoC

Intel develops both CPU and SoC versions of each generation

Intel® Technology Roadmap

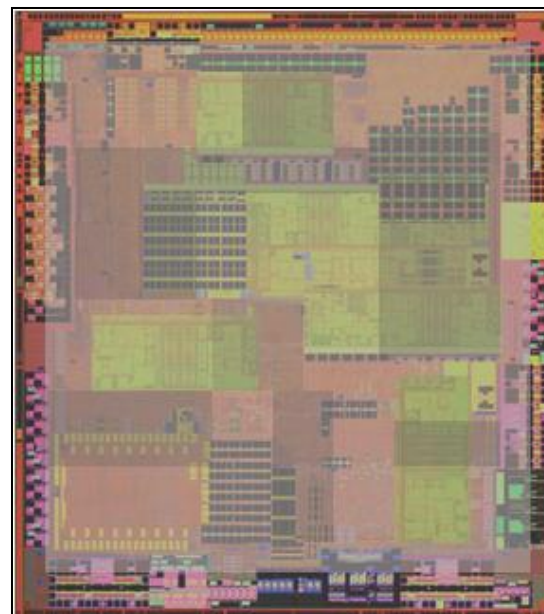
	32 nm		22 nm		14 nm	
Name:	P1268	P1269	P1270	P1271	P1272	P1273
Products:	CPU	SoC	CPU	SoC	CPU	SoC

Intel develops both CPU and SoC versions of each generation

Low Power Smartphone Products



Medfield Phone



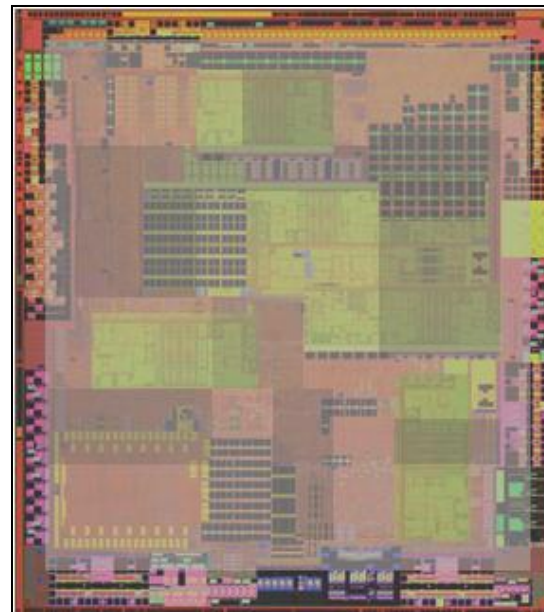
32 nm Intel® Atom™
processor (Medfield) SoC
432 million transistors, 64 mm²

Low Power Smartphone Products

32 nm SoC Technology Feature Menu

Logic Transistor	I/O Trans Voltage	Metal	Advanced Passives	Embedded Memory
High Performance	1.2V Low Power	9 Layer High Perf	Precision Resistor	Dense SRAM
Std Performance	1.8V Thick Gate	7-11 Layer Hi Dense	Precision Capacitor	Low Voltage SRAM
Low Power	3.3V Thick Gate		High Q Inductor	High Speed SRAM

32 nm SoC process offers a rich mix-and-match feature set



Intel Developer Forum, Sep. 2009

32 nm SoC Technology

32 nm Intel® Atom™
processor (Medfield) SoC
432 million transistors, 64 mm²

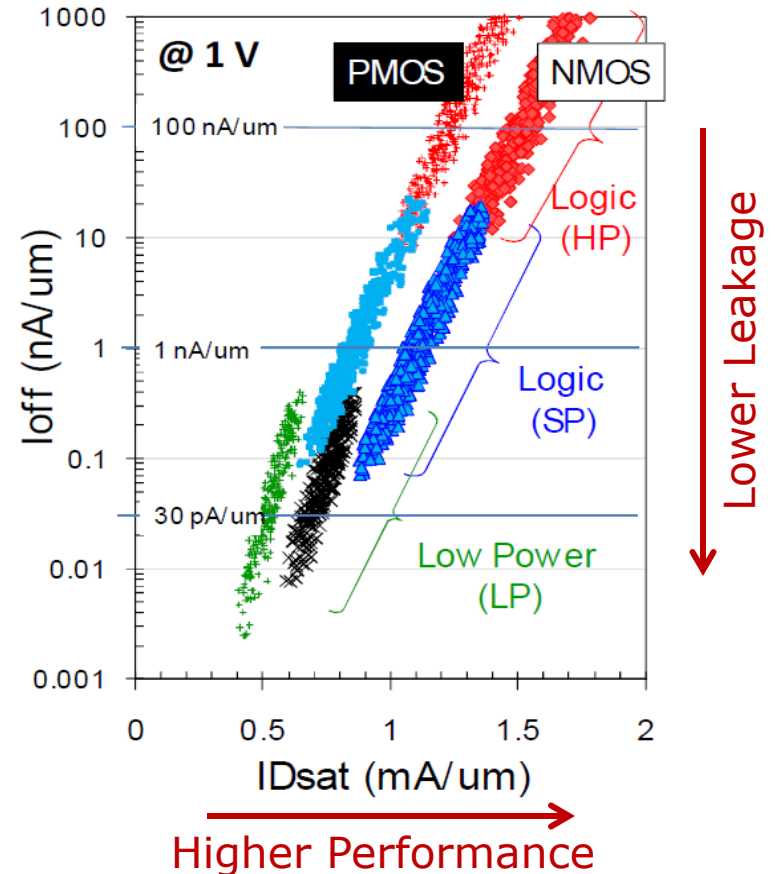
Low Power Smartphone Products

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32 nm SoC process offers a rich mix-and-match feature set

Intel Developer Forum, Sep. 2009



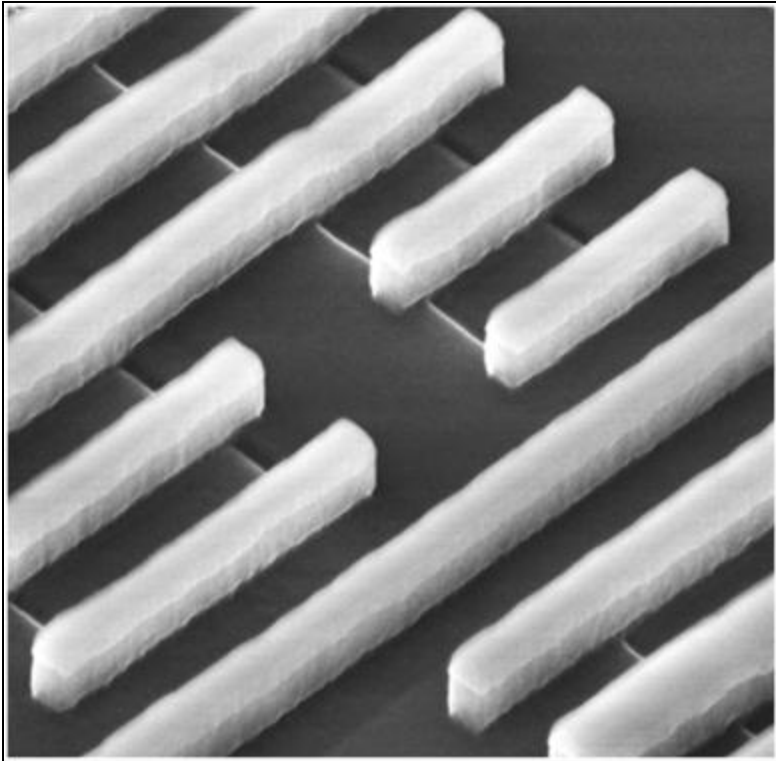
32 nm SoC Technology

32 nm SoC transistors range from high performance to low power

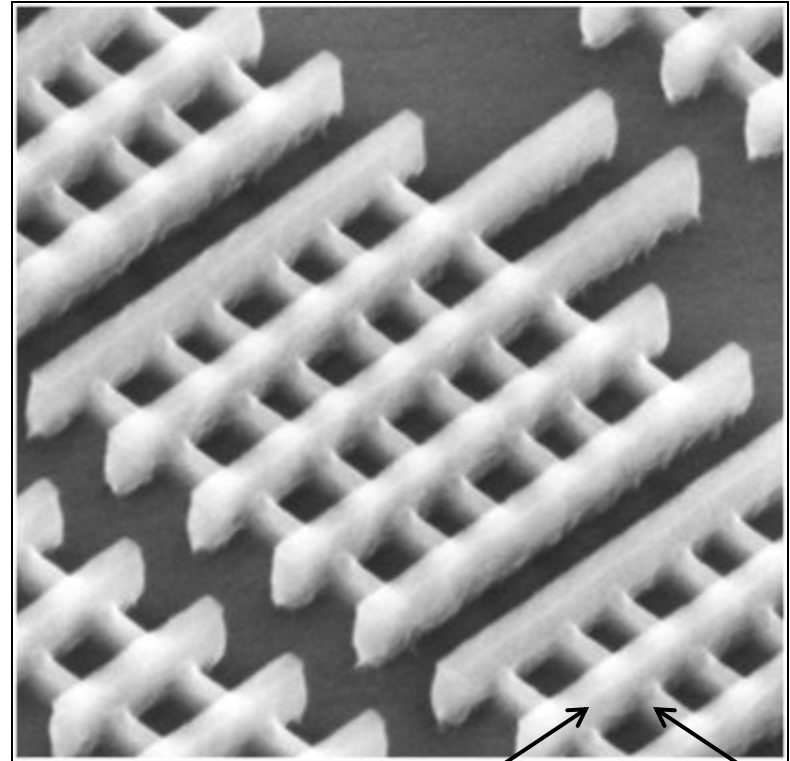
Intel® Technology Roadmap

	32 nm		22 nm		14 nm	
Name:	P1268	P1269	P1270	P1271	P1272	P1273
Products:	CPU	SoC	CPU	SoC	CPU	SoC

32 nm Planar Transistors



22 nm Tri-Gate Transistors

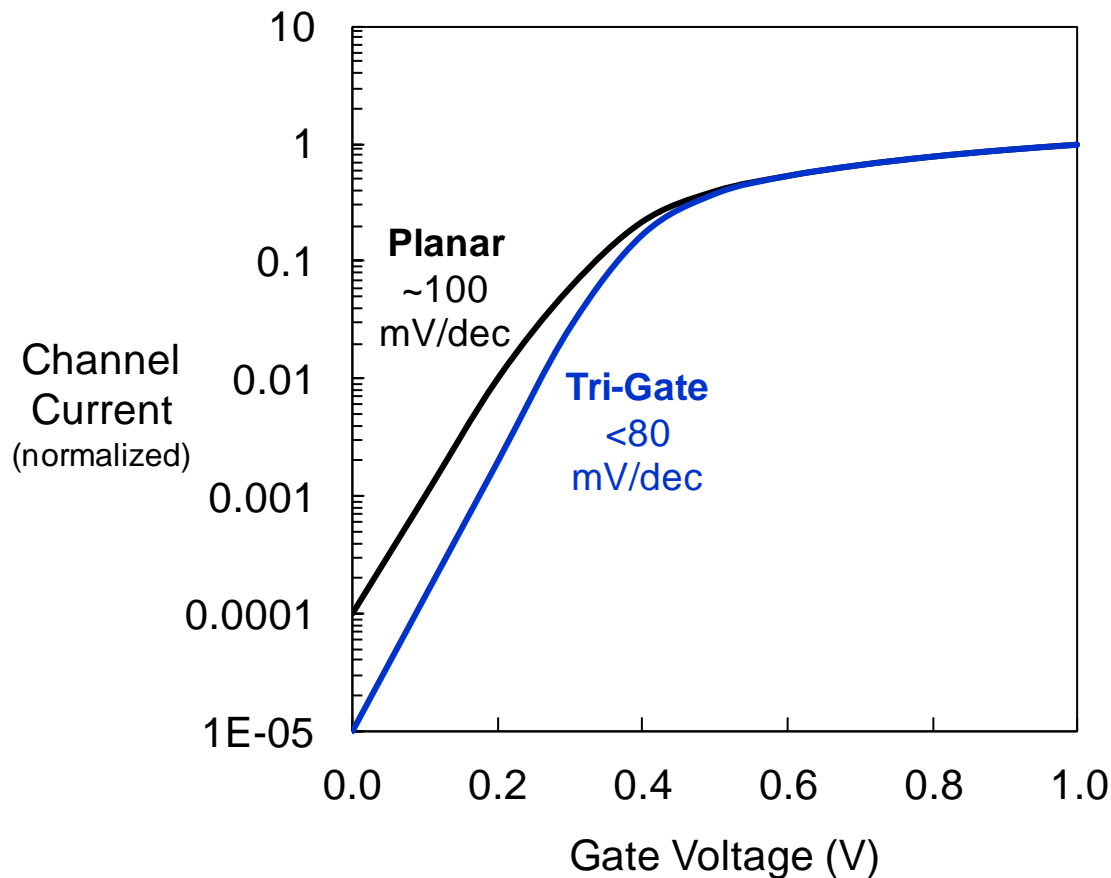


Gates

Fins

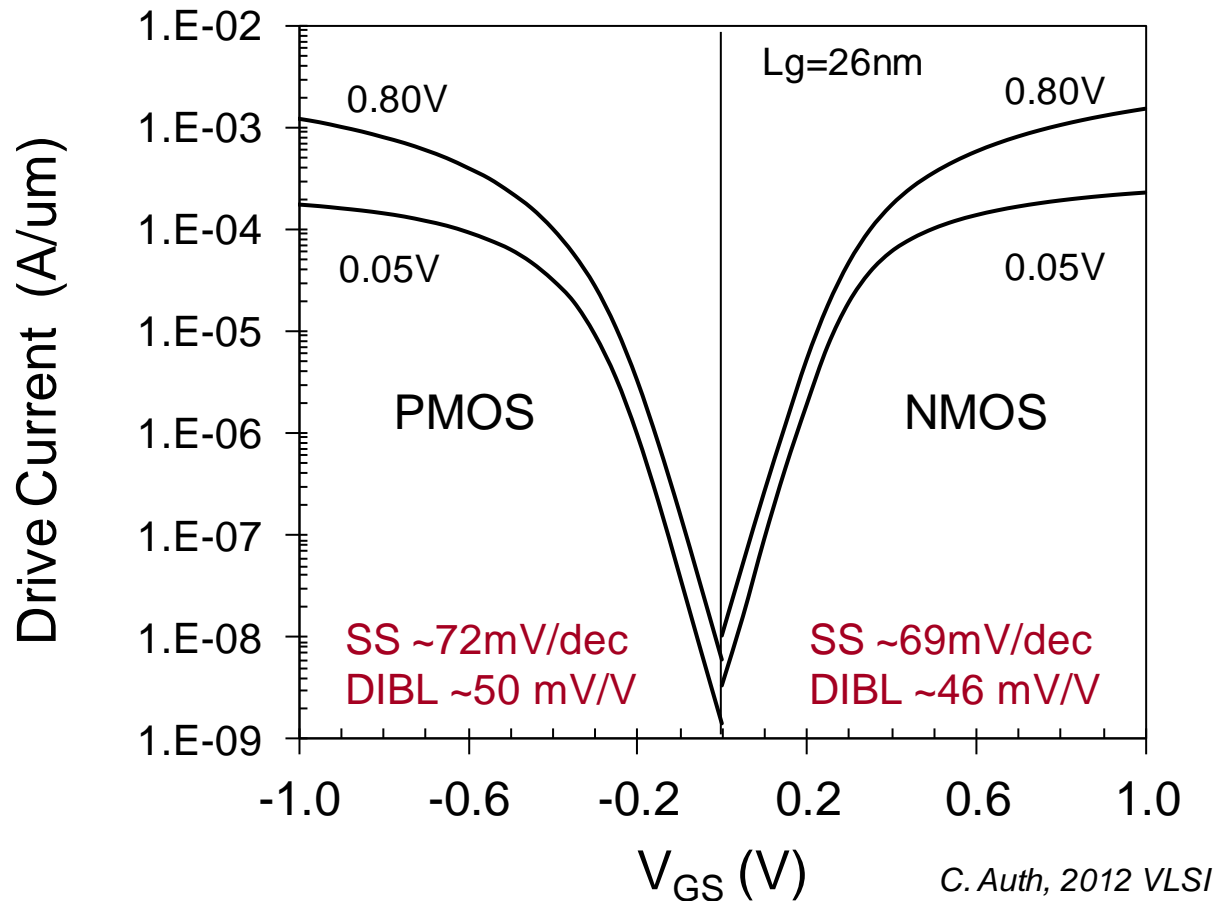
***22 nm generation introduces
revolutionary 3-D Tri-Gate transistors***

Fully Depleted Device



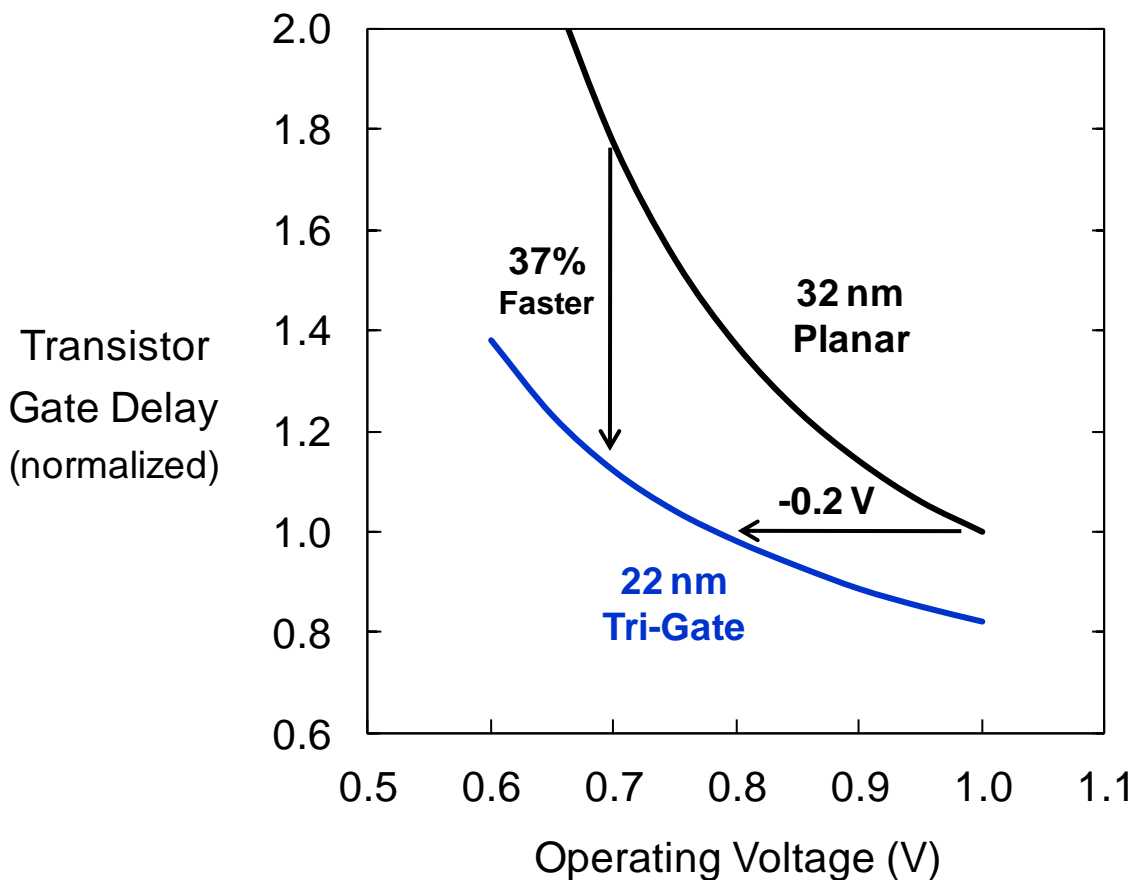
Tri-Gate transistors are fully depleted devices offering a steeper sub-threshold slope

22 nm Tri-Gate I-V Curves



Tri-Gate provides steepest sub-threshold slope and best short channel (DIBL) values of any technology in manufacturing

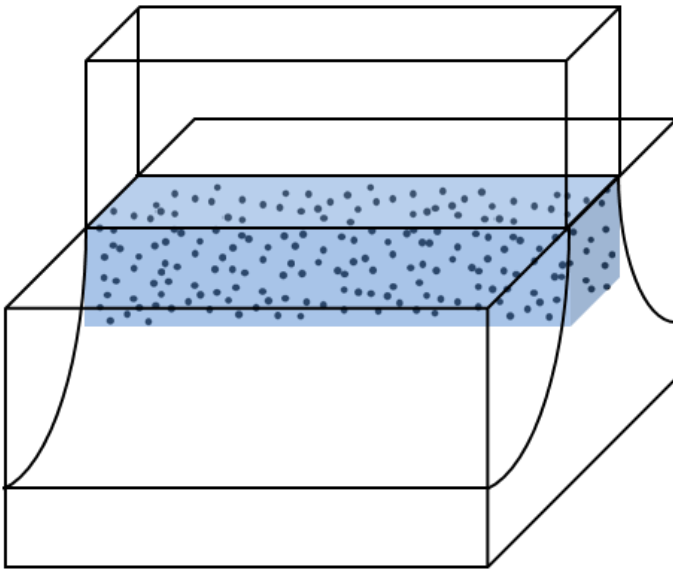
Performance/Power Benefits



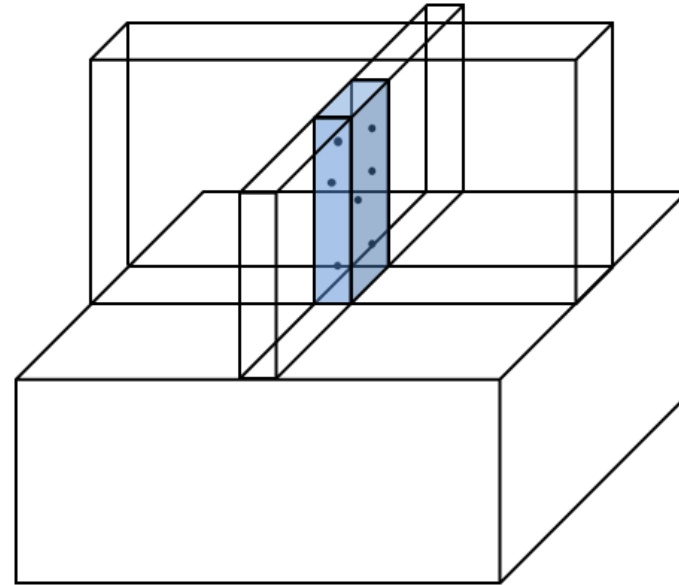
***Tri-Gate provides 37% speed up at low voltage
or 50% active power reduction at same performance***

Reduced Channel Doping

Planar

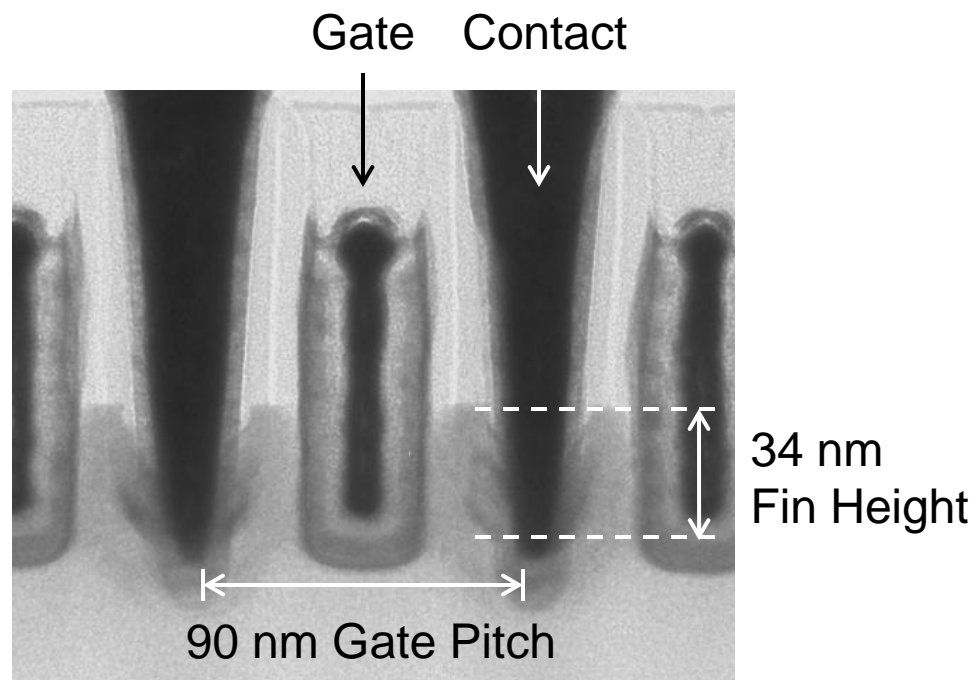
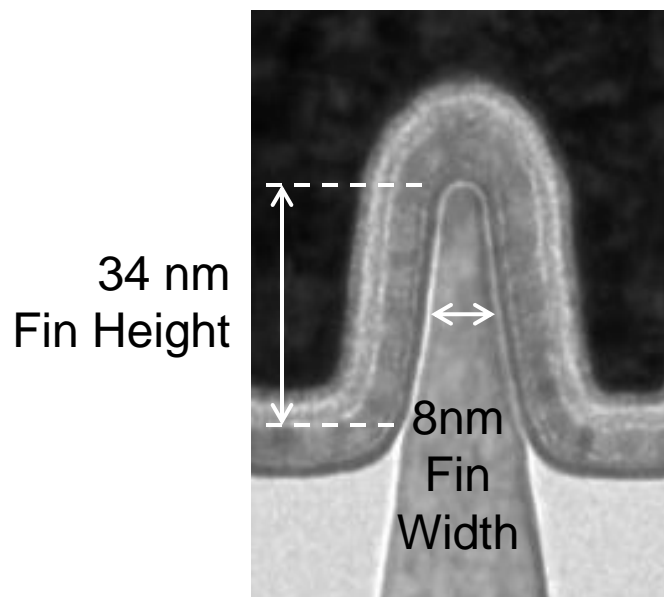


Tri-Gate



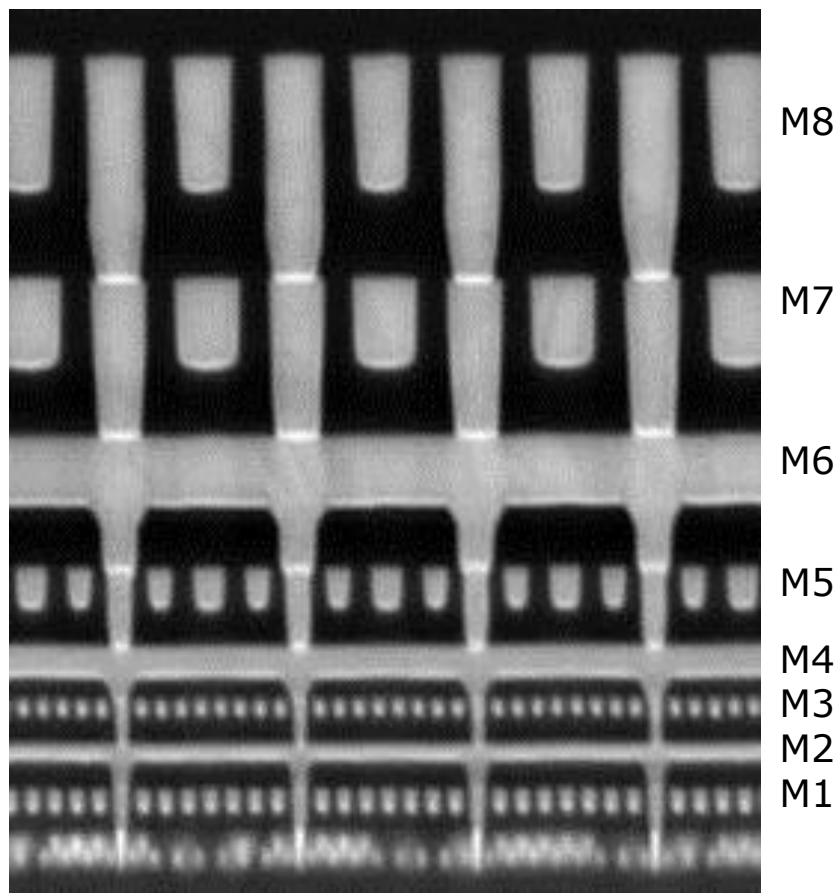
Fully depleted Tri-Gate structure has reduced channel doping, providing improved performance and reduced variability

22 nm Tri-Gate Transistors



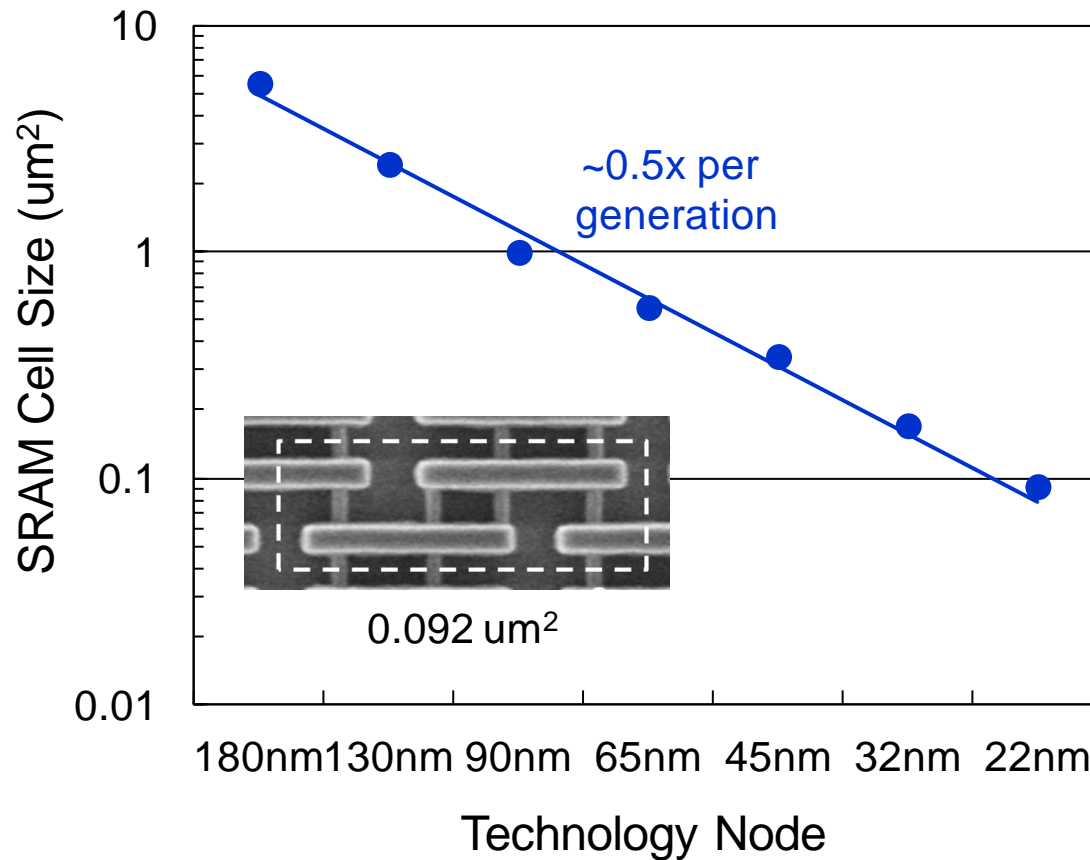
22 nm Interconnects

<u>Layer</u>	<u>Pitch</u>
TM	14 μm
M8	360 nm
M7	320 nm
M6	240 nm
M5	160 nm
M4	112 nm
M3	80 nm
M2	80 nm
M1	90 nm



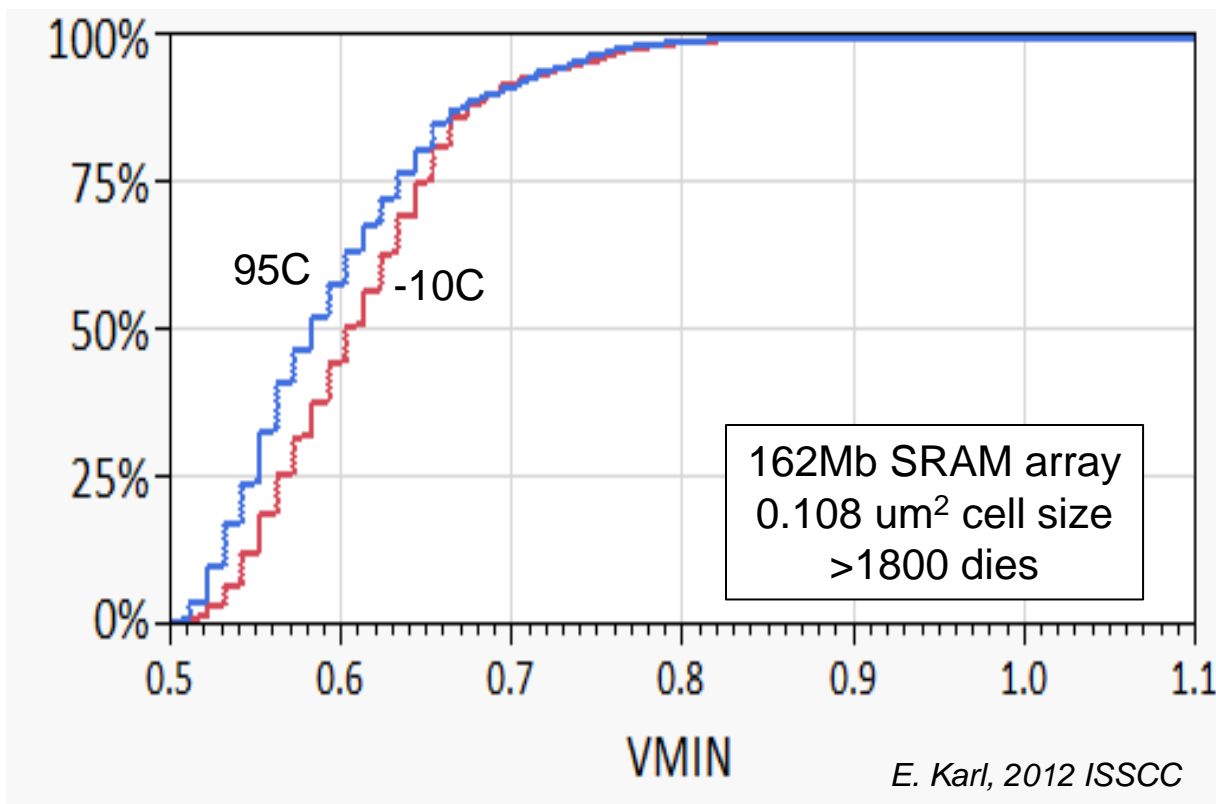
***Minimum pitch scaled $\sim 0.7\times$ from 32 nm
for $\sim 2\times$ transistor density improvement***

SRAM Cells



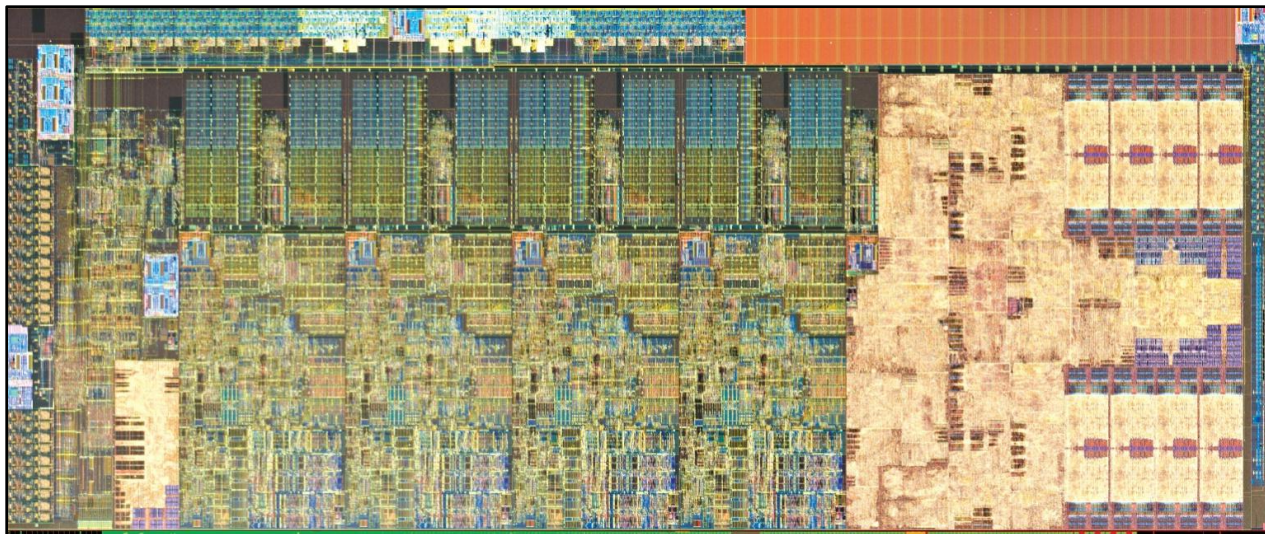
***0.092 μm^2 and 0.108 μm^2 SRAM cells
optimized for density and performance/power***

SRAM Array V_{MIN}



0.60V medium active V_{MIN} for low power applications

3RD Generation Intel® Core™ Processor

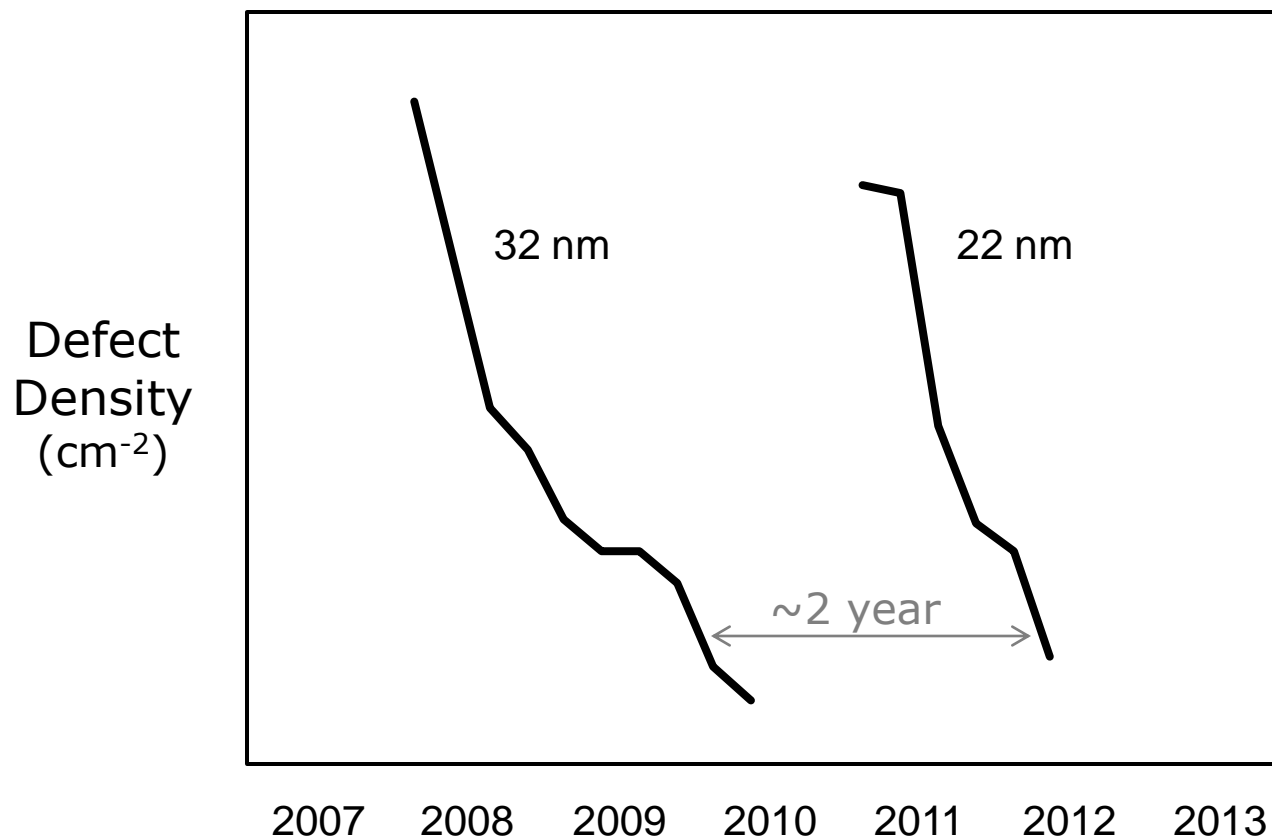


22 nm Tri-Gate Technology

4 Cores + Integrated Graphics

1.4 Billion Transistors, 160 mm²

22 nm Defect Density Trend



***22 nm defect density now at low levels
needed for volume manufacturing***

22 nm Manufacturing Fabs



D1D Oregon ✓



D1C Oregon



Fab 32 Arizona ✓



Fab 28 Israel ✓



Fab 12 Arizona

✓ In production 2Q '12

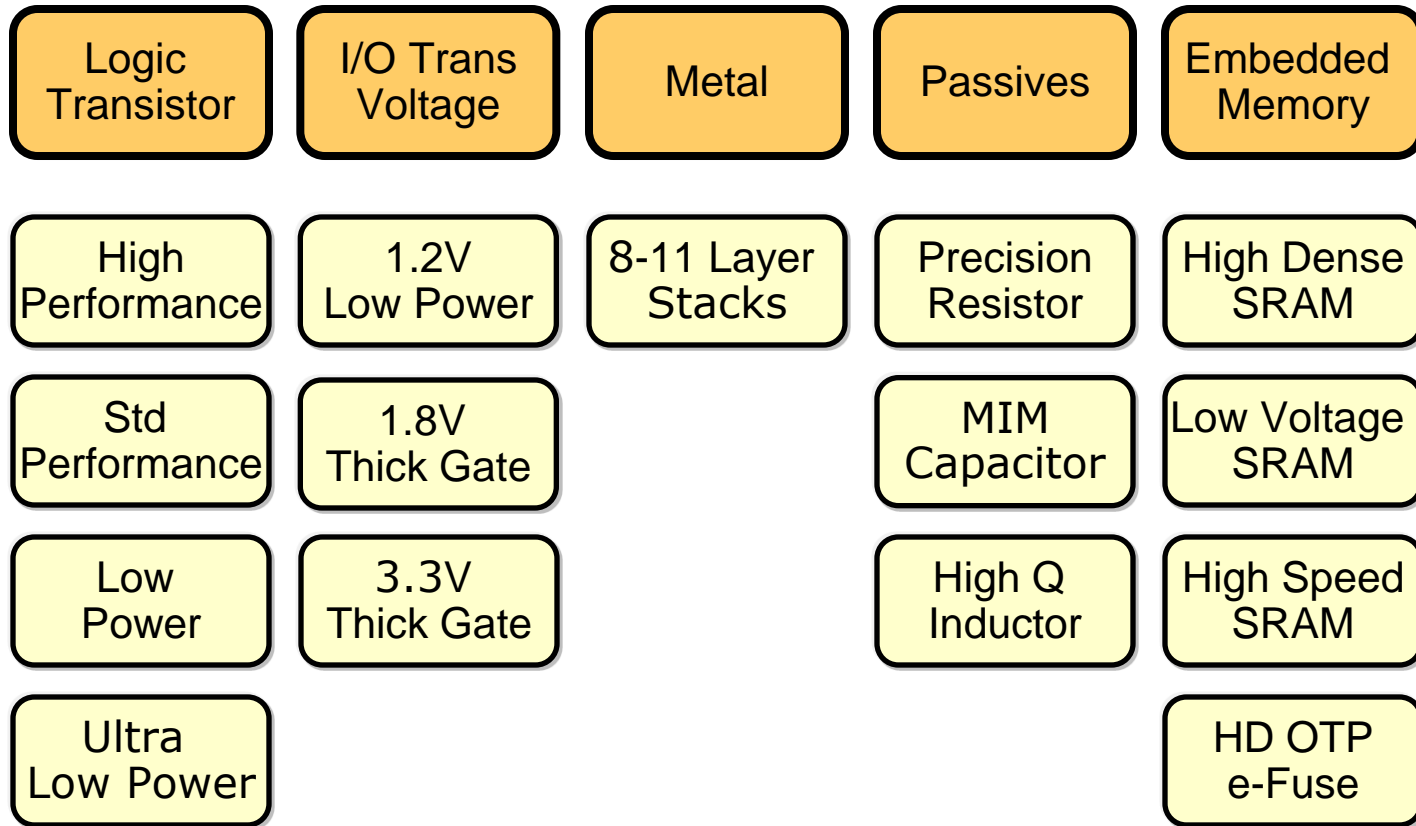
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	32 nm		22 nm		14 nm	
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Products:	CPU	SoC	CPU	SoC	CPU	SoC

CPU vs. SoC Technology Comparison

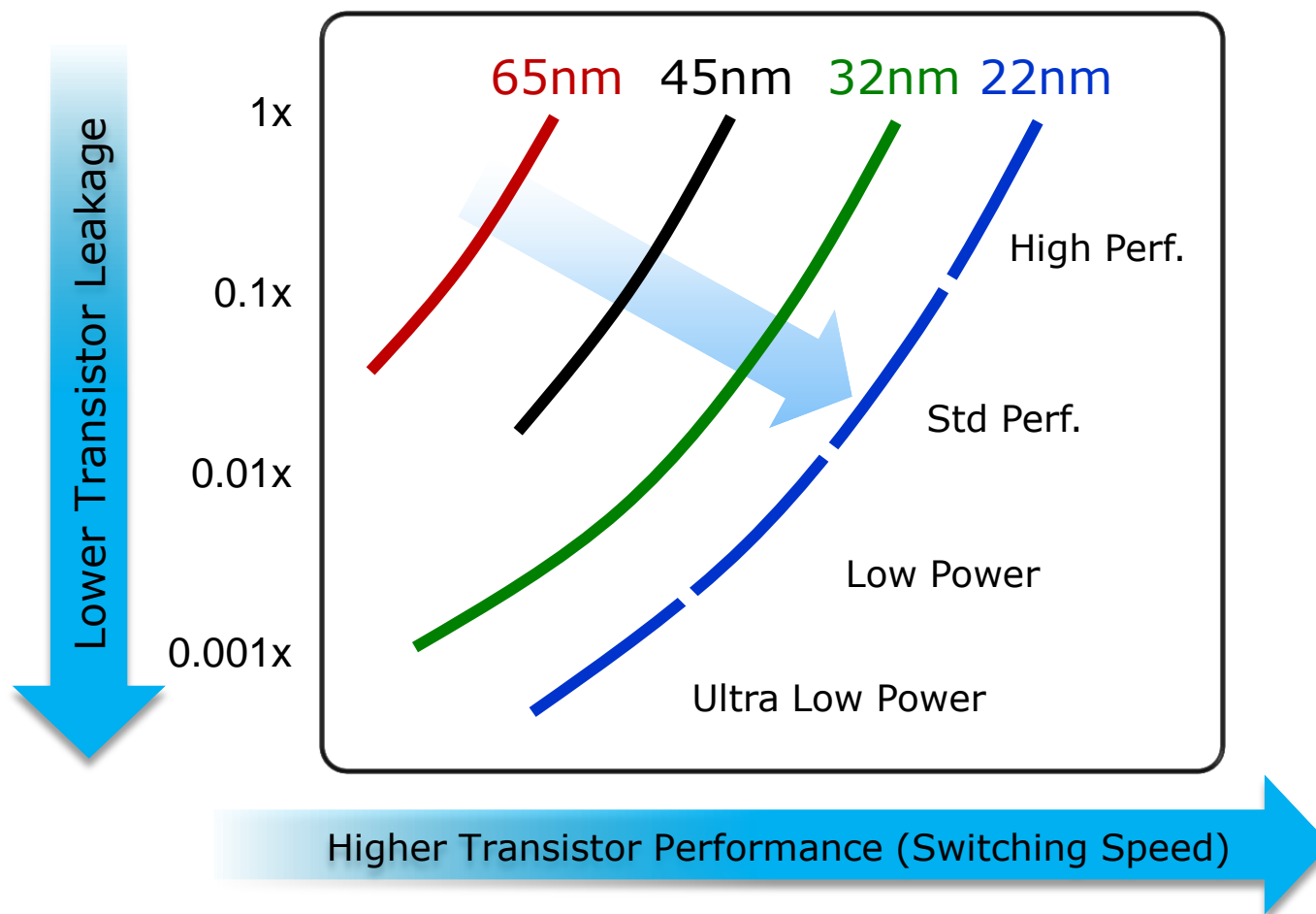
	CPU (P1270)	SoC (P1271)
<u>Similarities</u>		
Tri-Gate Structure	Same	Same
Tight Transistor Pitch	Same	Same
Dense SRAM Cell	Same	Same
Lower Level Interconnects	Same	Same
Fab Process Equipment	Same	Same
<u>Differences</u>		
Logic Transistors	High Speed	Low Leakage
I/O Transistors	Std Voltage	Std and High Volt
Upper Level Interconnects	High Speed	Dense
Precision Passives	None	R, C and L

22 nm SoC Technology Features



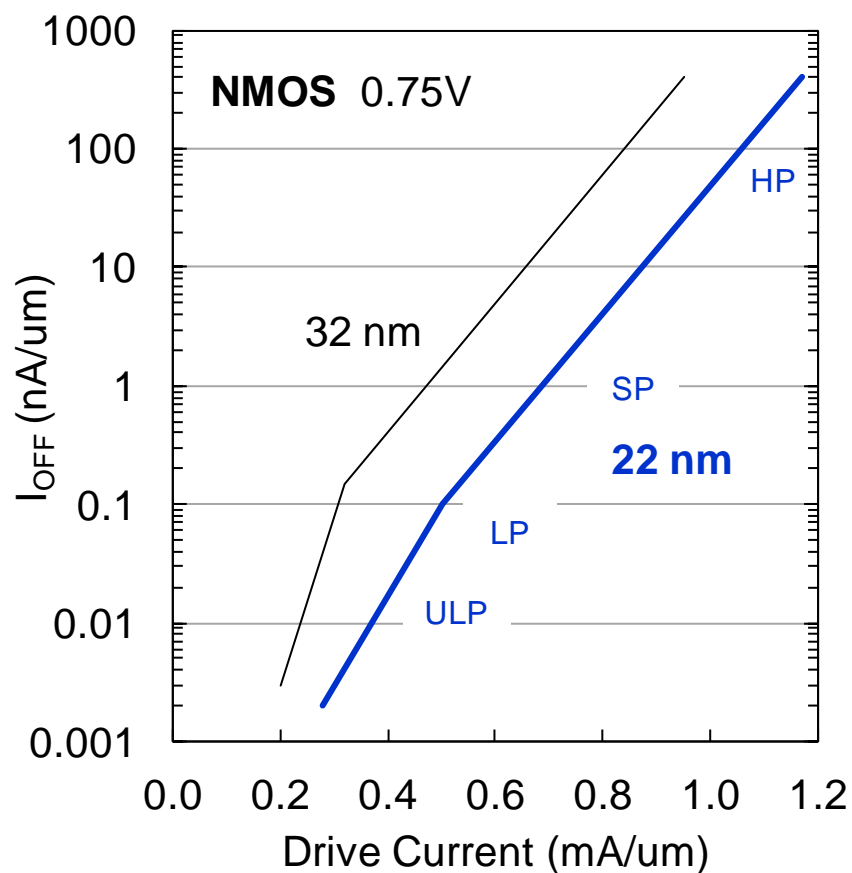
22 nm SoC technology offers a rich menu of feature options

Transistor Performance vs. Leakage

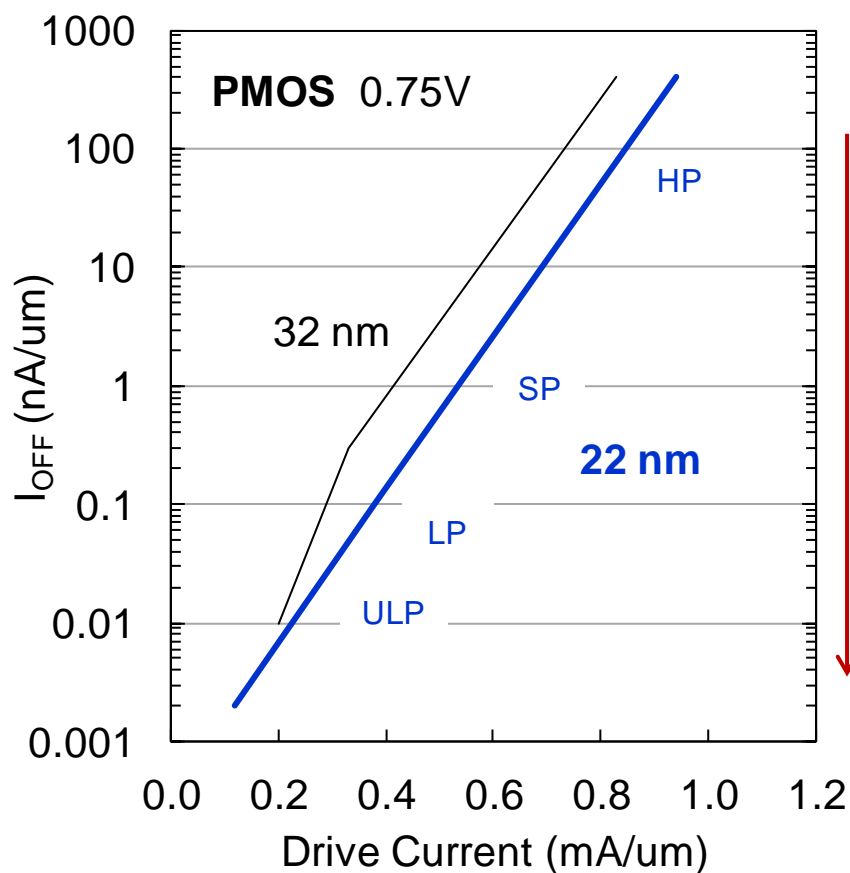


22 nm SoC technology offers a wide range of transistors

Transistor Performance vs. Leakage



Higher Performance →

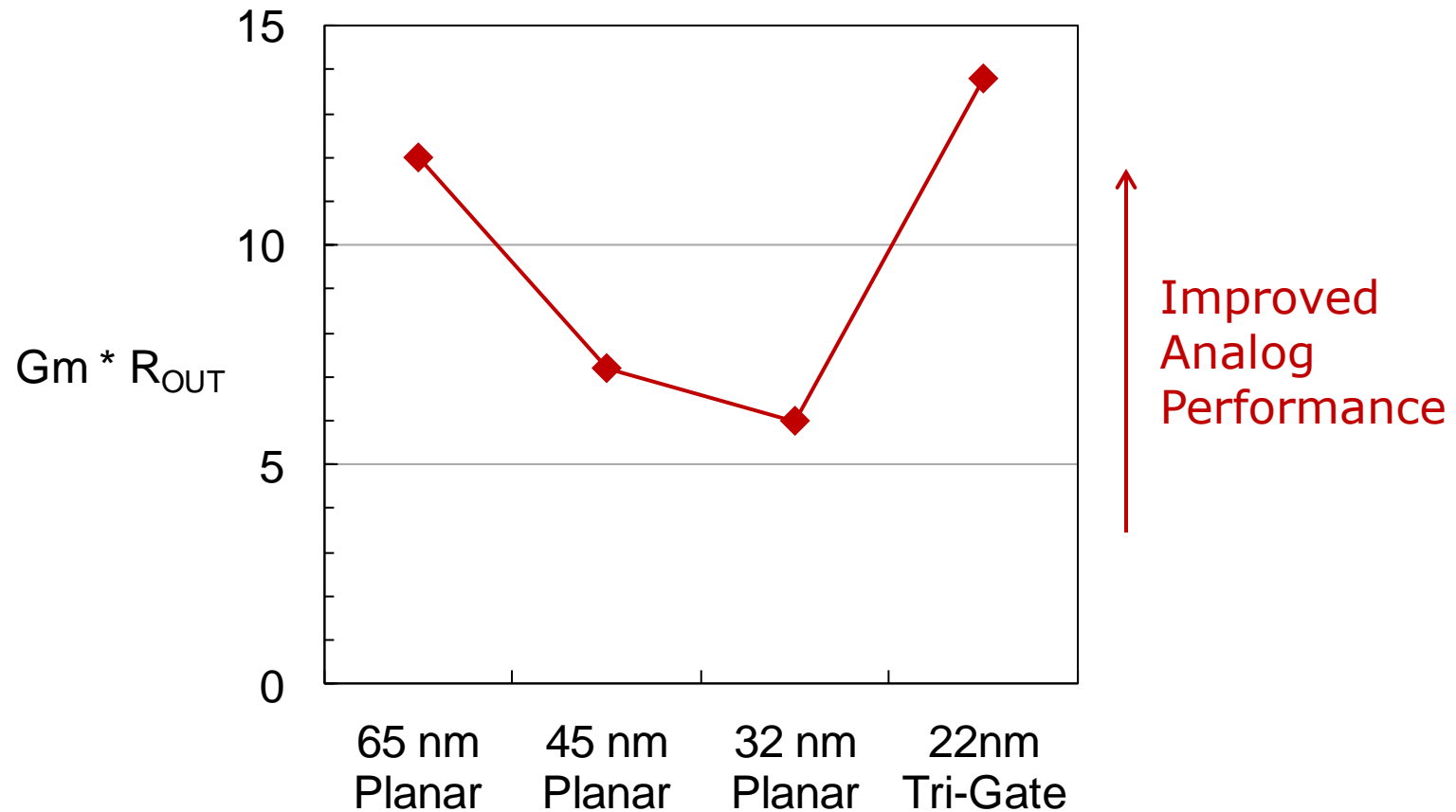


Higher Performance →

Lower Leakage ↓

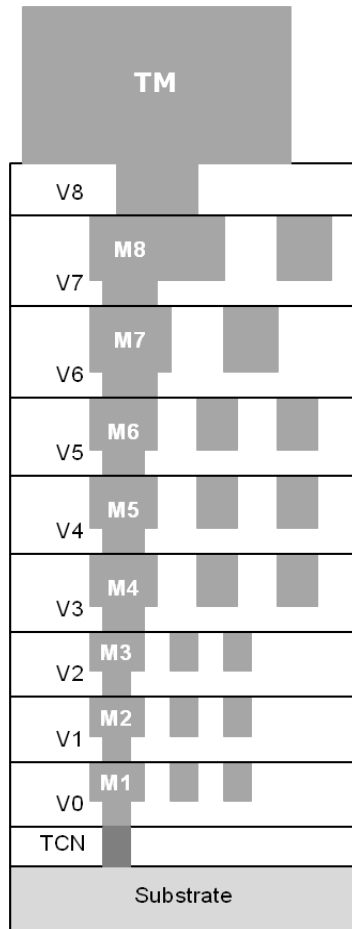
22 nm SoC technology offers a wide range of transistors

Analog Device Characteristics



22 nm Tri-Gate transistors provide improved $G_m * R_{OUT}$ for improved analog circuit performance

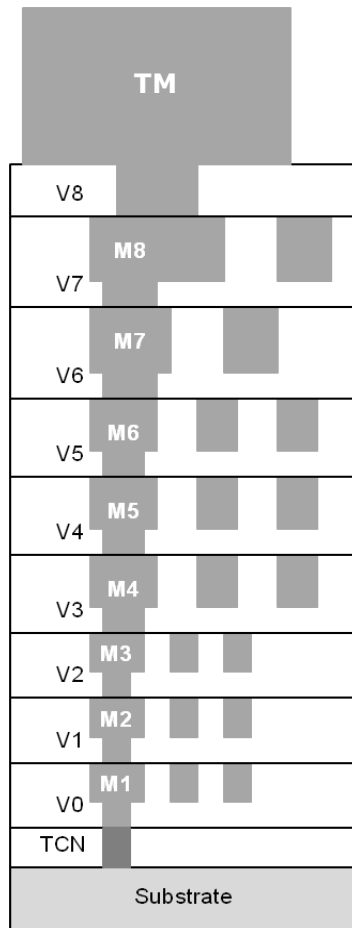
22 nm SoC Interconnect Options



<u>Layer</u>	<u>A</u>	<u>B</u>	<u>C</u>	
TM	14	14	14	um
M10	-	-	360	nm
M9	-	360	360	nm
M8	360	240	160	nm
M7	240	160	108	nm
M6	160	108	80	nm
M5	108	80	80	nm
M4	80	80	80	nm
M3	80	80	80	nm
M2	80	80	80	nm
M1	90	90	90	nm

Range of SoC interconnect options for low cost or high density

22 nm SoC Interconnect Options

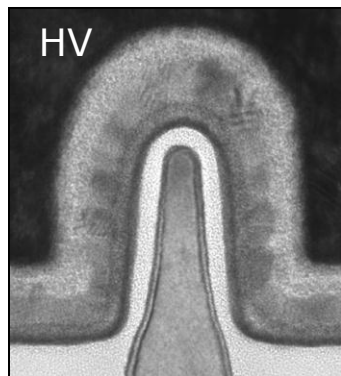
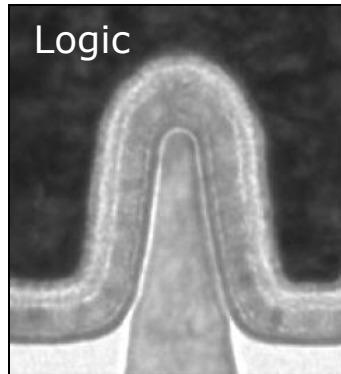


Layer	<u>A</u>	<u>B</u>	<u>C</u>	
TM	14	14	14	um
M10	-	-	360	nm
M9	-	360	360	nm
M8	360	240	160	nm
M7	240	160	108	nm
M6	160	108	80	nm
M5	108	80	80	nm
M4	80	80	80	nm
M3	80	80	80	nm
M2	80	80	80	nm
M1	90	90	90	nm

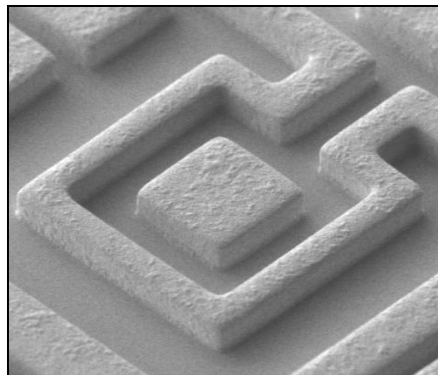
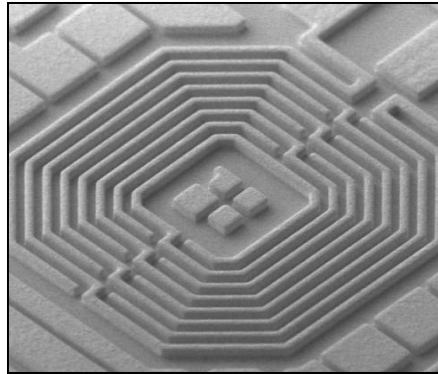
80 nm pitch is done with single patterning, thus an optimal pitch to use for this generation

22 nm SoC Device Features

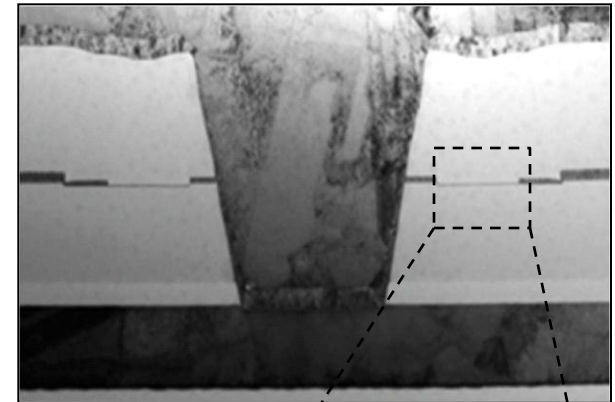
High Voltage
I/O Transistors



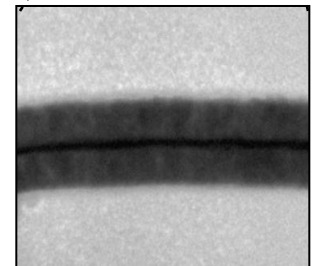
Inductors



MIM Capacitor



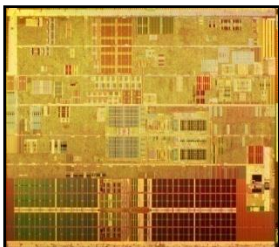
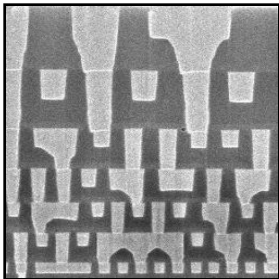
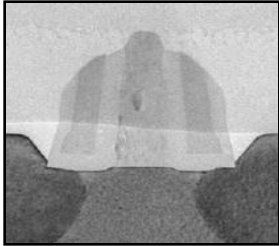
Metal
Insulator
Metal



2 Year Technology Cycles

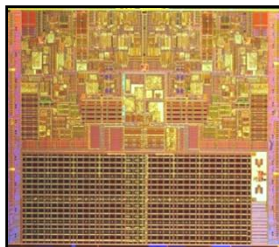
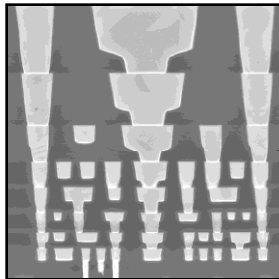
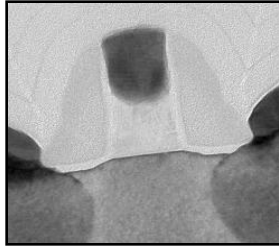
90 nm

2003



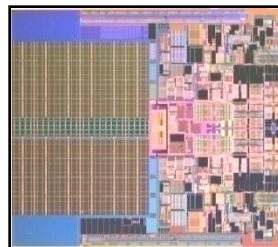
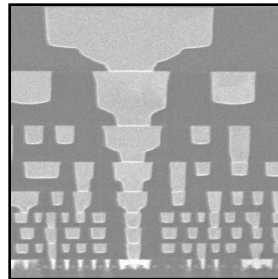
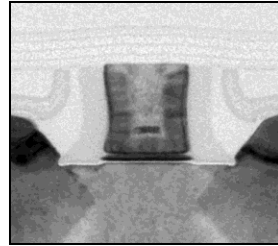
65 nm

2005



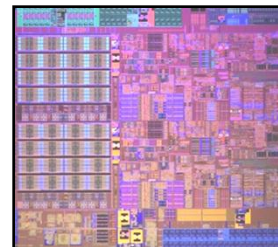
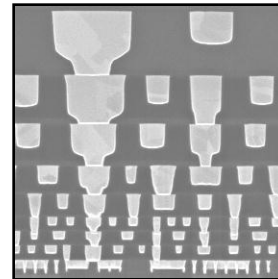
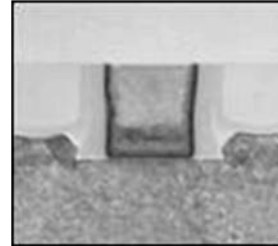
45 nm

2007



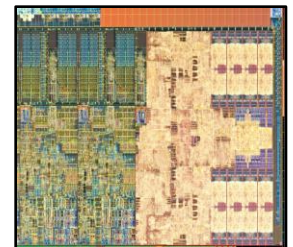
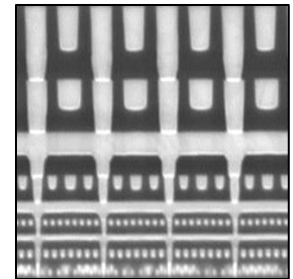
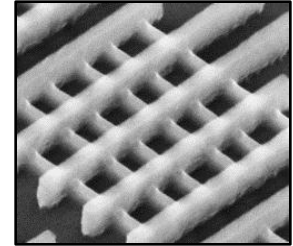
32 nm

2009

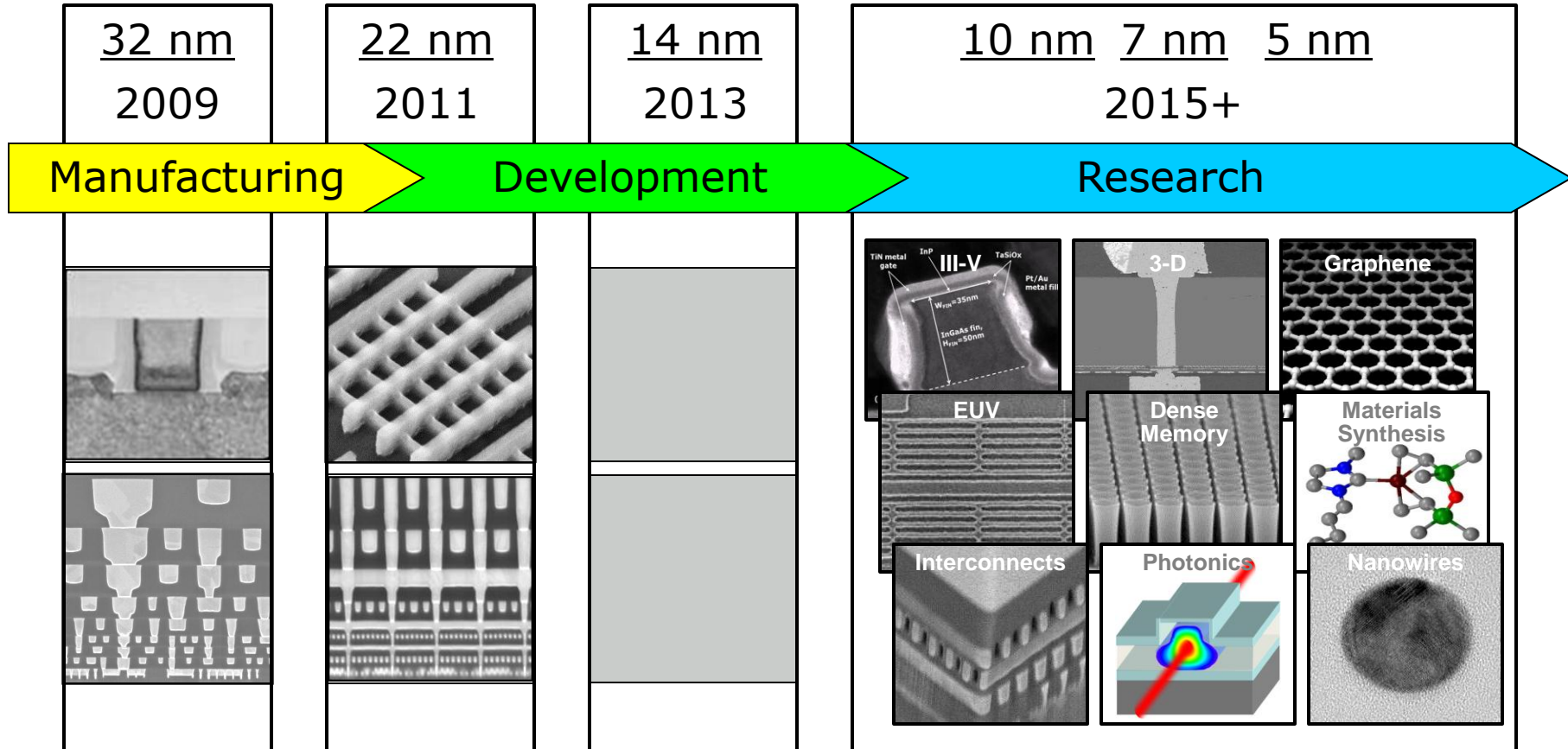


22 nm

2011



Innovation Enabled Technology Pipeline



Future options subject to change

Advantage of an Integrated Device Manufacturer

Research



Components Research

Equipment Vendors
Industry Consortia
Universities
Government Labs

- **Identify innovative technologies**

Advantage of an Integrated Device Manufacturer

Research

Components Research

Equipment Vendors
Industry Consortia
Universities
Government Labs

- **Identify innovative technologies**

Development

Product Design Logic Technology Development

Design Tools
Photo Masks
Packaging

- **Co-optimize process+product**
- **Design for manufacturing**

Advantage of an Integrated Device Manufacturer

Research

Components Research

Equipment Vendors
Industry Consortia
Universities
Government Labs

- **Identify innovative technologies**

Development

Product Design Logic Technology Development

Design Tools
Photo Masks
Packaging

- **Co-optimize process+product**
- **Design for manufacturing**

Manufacturing

Wafer Manufacturing Fabs

Oregon
Arizona
New Mexico
Israel
Ireland
China

- **Early product ramp**
- **Rapid yield learning**

Summary

- Transistor scaling continues to provide improvements in performance, power and cost, but now with greater focus on power reduction
- Scaling no longer follows a “classical” path and requires continued innovations in materials and structures
- A highly integrated approach is needed to successfully bring innovative technologies from the research phase to high volume manufacturing
- Low power System-on-Chip technologies are increasingly important to support the wide range of features needed on mobile computing devices

Additional Sources of Information on This Topic:

More web based info:

www.intel.com/technology/architecture-silicon

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Risk Factors

The above statements and any others in this document that refer to plans and expectations for the second quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel’s actual results, and variances from Intel’s current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company’s expectations. Demand could be different from Intel’s expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel’s and competitors’ products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel’s products; actions taken by Intel’s competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel’s response to such actions; and Intel’s ability to respond quickly to technological developments and to incorporate new features into its products. Intel is in the process of transitioning to its next generation of products on 22nm process technology, and there could be execution and timing issues associated with these changes, including products defects and errata and lower than anticipated manufacturing yields. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The majority of Intel’s non-marketable equity investment portfolio balance is concentrated in companies in the flash memory market segment, and declines in this market segment or changes in management’s plans with respect to Intel’s investments in this market segment could result in significant impairment charges, impacting restructuring charges as well as gains/losses on equity investments and interest and other. Intel’s results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel’s products and the level of revenue and profits. Intel’s results could be affected by the timing of closing of acquisitions and divestitures. Intel’s results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues, such as the litigation and regulatory matters described in Intel’s SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel’s ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel’s results is included in Intel’s SEC filings, including the company’s most recent Form 10-Q, Form 10-K and earnings release.

Rev. 5/4/12