Which is correct about the ALU and the register file in MIPS?

A. The ALU *always* performs an operation before accessing the register file

B. The ALU *sometimes* performs an operation before accessing the register file

C. The register file is *always* accessed before performing an ALU operation

D. The register file is *sometimes* accessed before performing an ALU operation

E. None of the above.

- Answer C

Which is correct about the ALU and memory in MIPS?

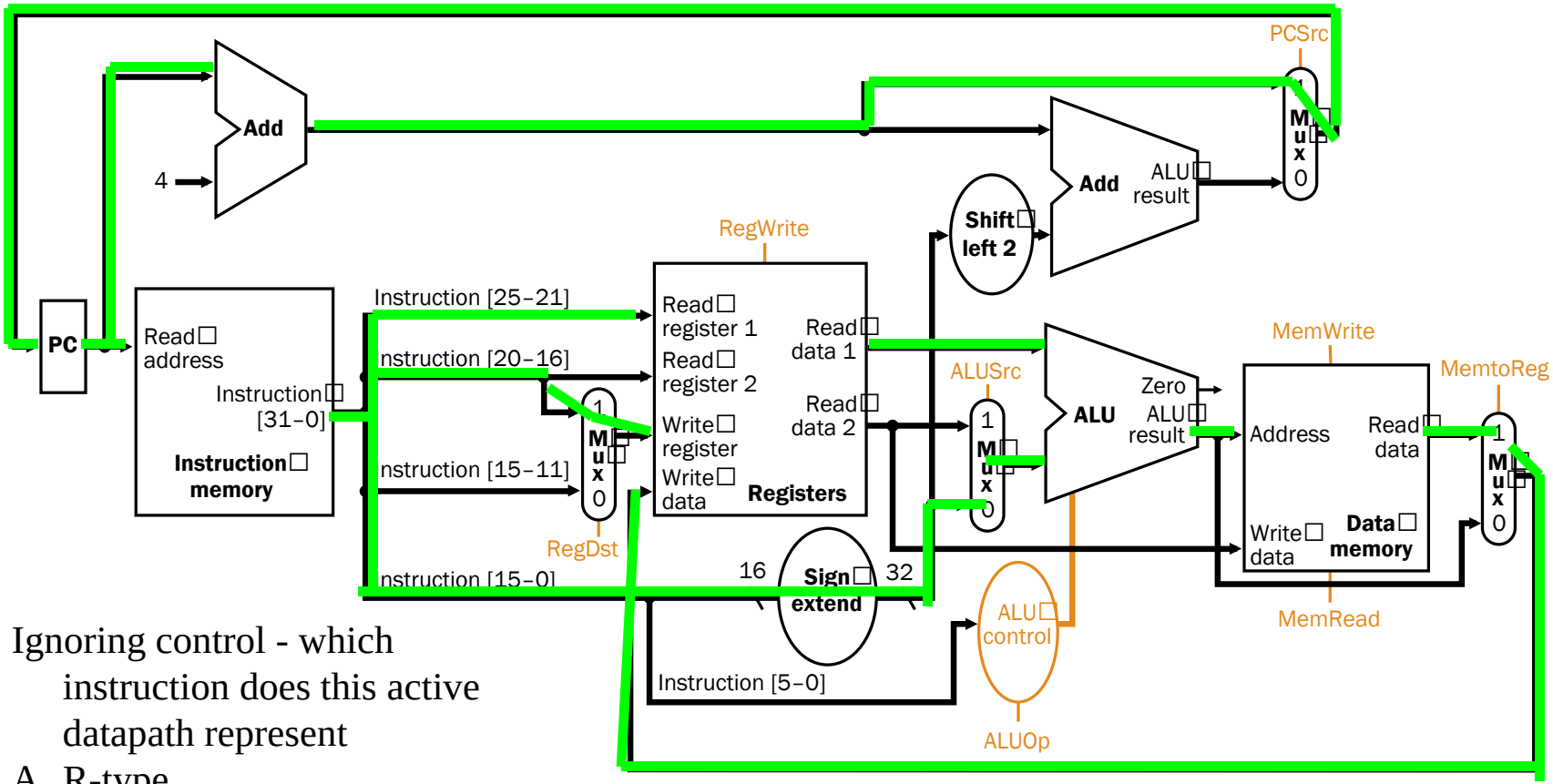
A. The ALU *always* performs an operation before accessing data memory
B. The ALU *sometimes* performs an operation before accessing data memory
C. Data memory is *always* accessed before performing an ALU operation
D. Data memory is *sometimes* accessed before performing an ALU operation
E. None of the above.

- Answer A

A branch instruction changes the flow of information by changing the PC

TRUE or FALSE?

Active Single-Cycle Datapath -1

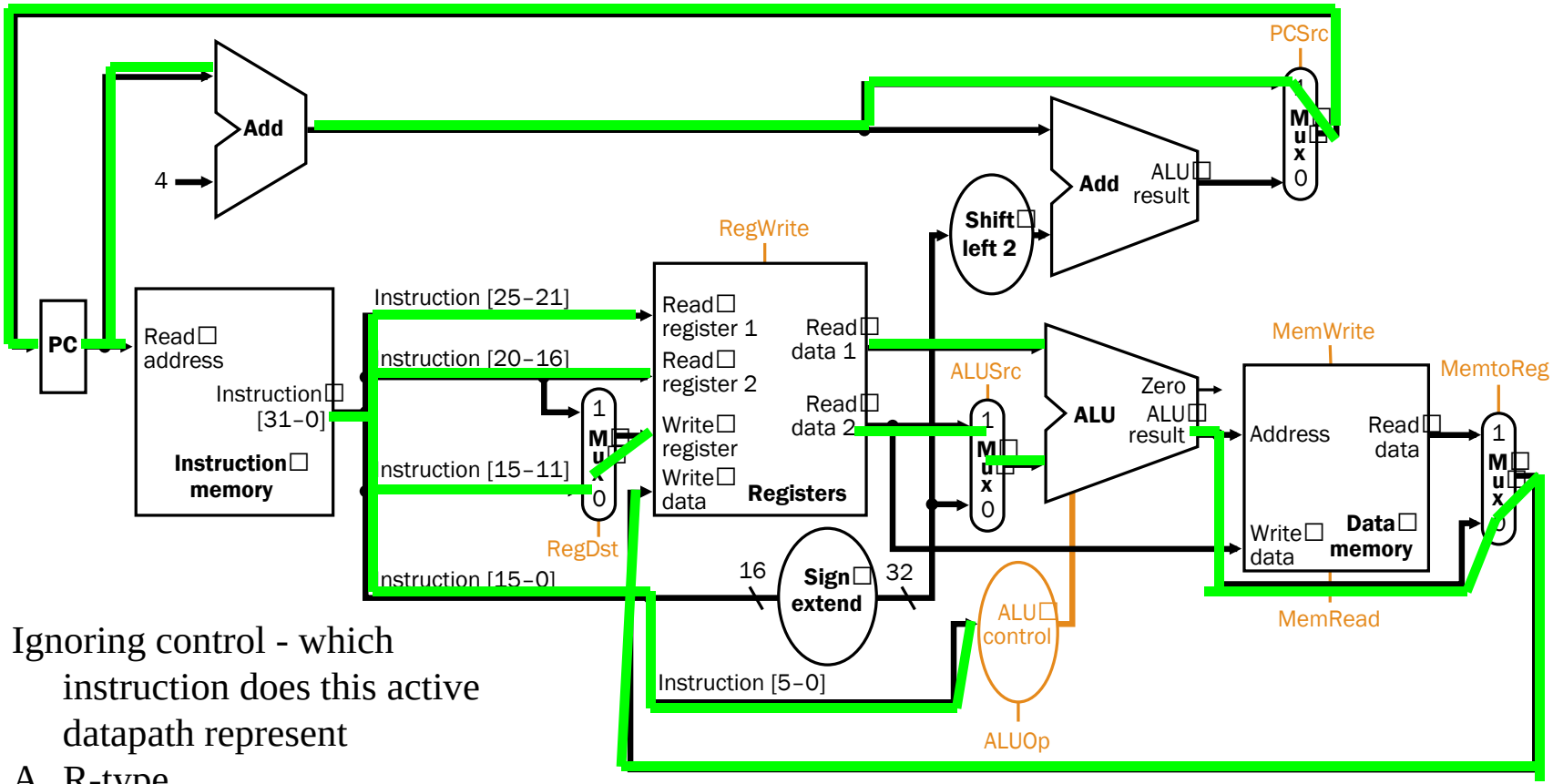


Ignoring control - which instruction does this active datapath represent

A. R-type
B. lw
C. sw
D. Beq
E. None of the above

- Answer lw

Active Single-Cycle Datapath - 2

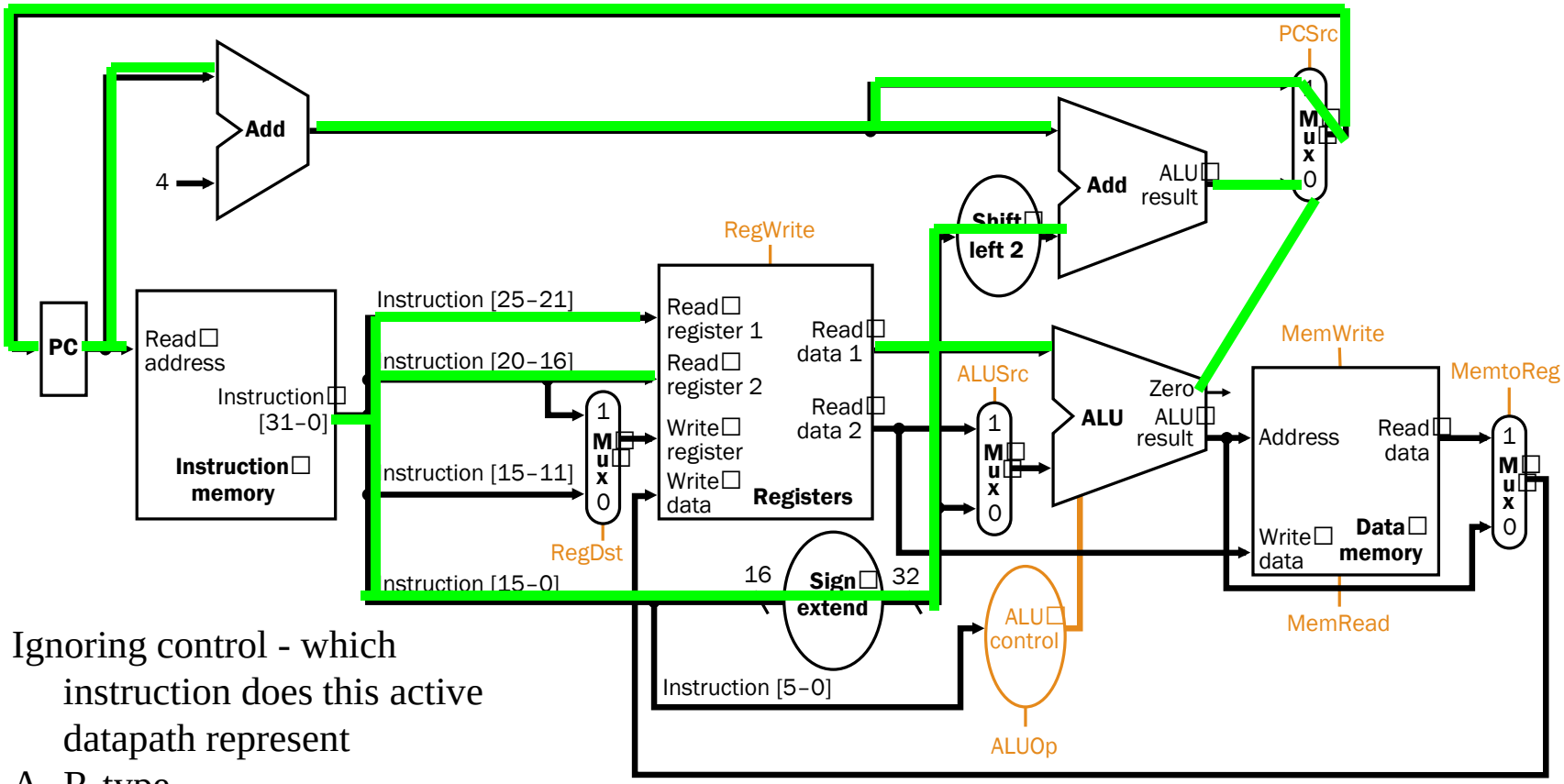


Ignoring control - which instruction does this active datapath represent

A. R-type
B. lw
C. sw
D. Beq
E. None of the above

- Answer R type

Active Single-Cycle Datapath - 3

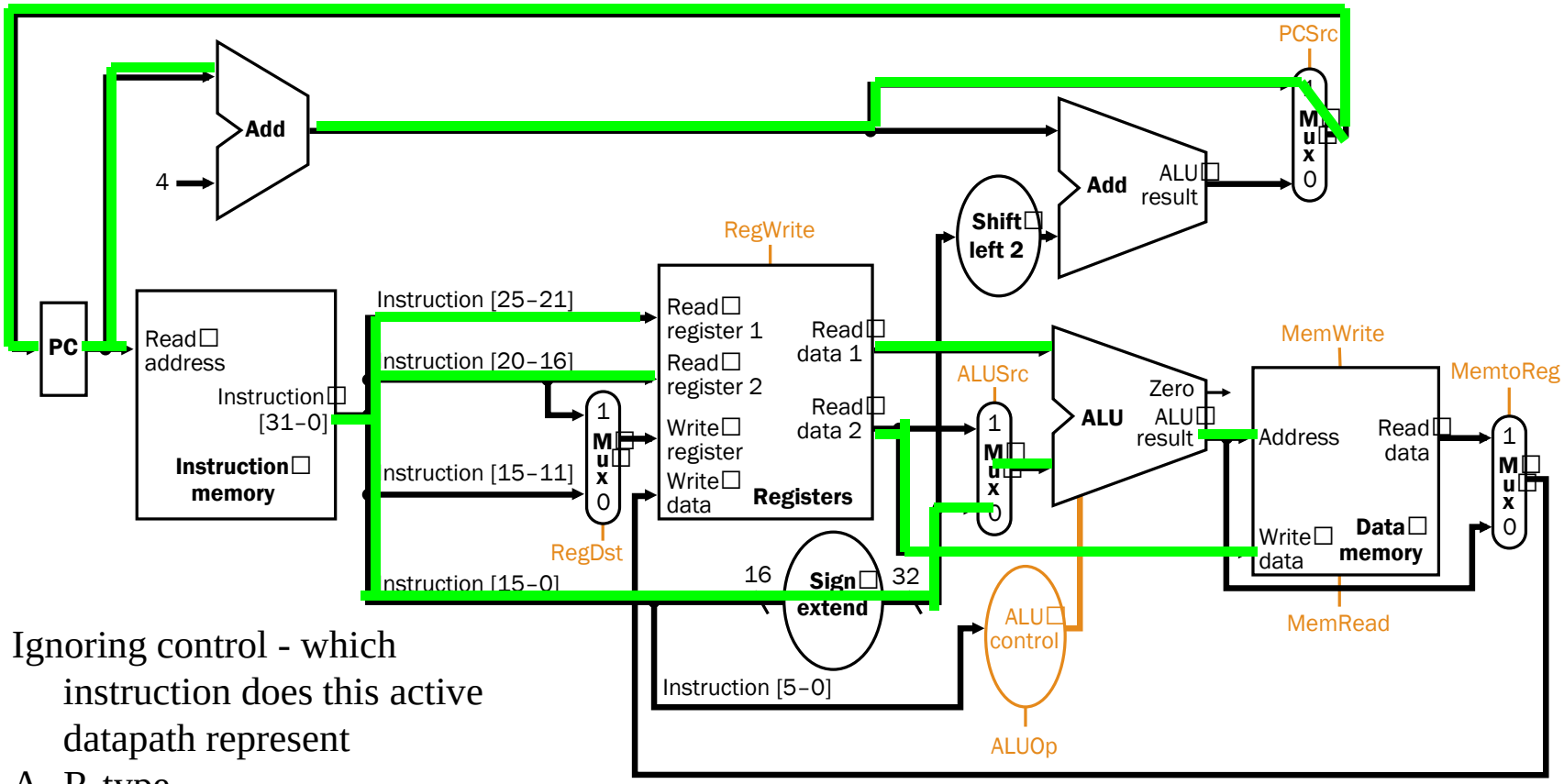


Ignoring control - which instruction does this active datapath represent

A. R-type
B. lw
C. sw
D. Beq
E. None of the above

- Answer branch

Active Single-Cycle Datapath - 4



Ignoring control - which instruction does this active datapath represent

A. R-type
B. lw
C. sw
D. Beq
E. None of the above

- Answer sw

Which of these describes our register file?

A. Two 32-bit outputs, 3 5-bit inputs, 1-bit control input, 1 32-bit input

B. Two 32-bit outputs, 3 32-bit inputs, 1-bit control input

C. Two 32-bit outputs, 2 5-bit inputs, 1 32-bit input, 1-bit control input

D. Two 32-bit outputs, 2 32-bit inputs, 1 32-bit input, 1-bit control input

E. None of the above

- Answer A

Which of these describes our memory ?

A. One 32-bit output, 1 5-bit input, 1 32-bit input, 1 bit control input

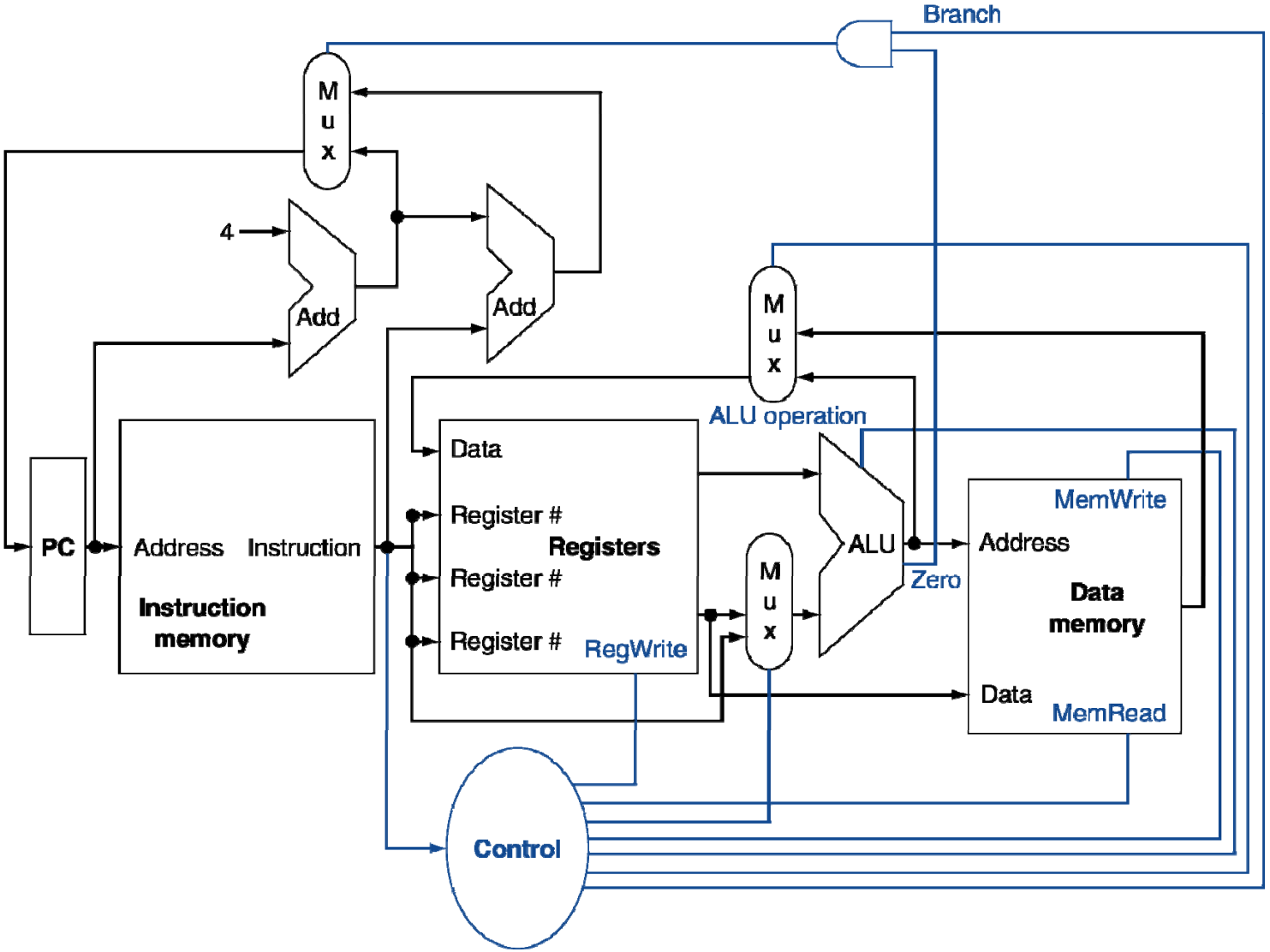
B. One 32-bit output, 2 5-bit inputs,1-bit control input, 1 bit control input

C. One 32-bit output, 2 32-bit inputs, 2 1-bit control inputs

D. One 32-bit output, 1 32-bit input, 2 1-bit control inputs

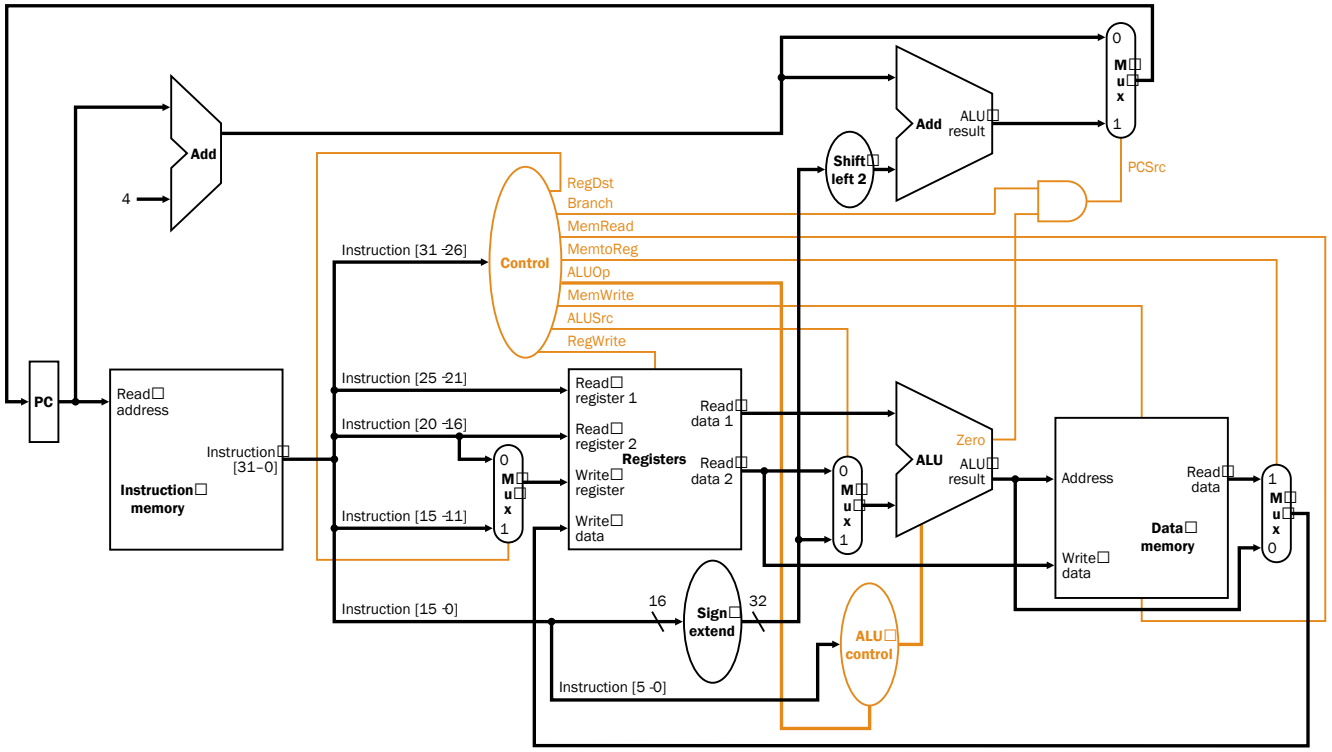
E. None of the above

- Answer C



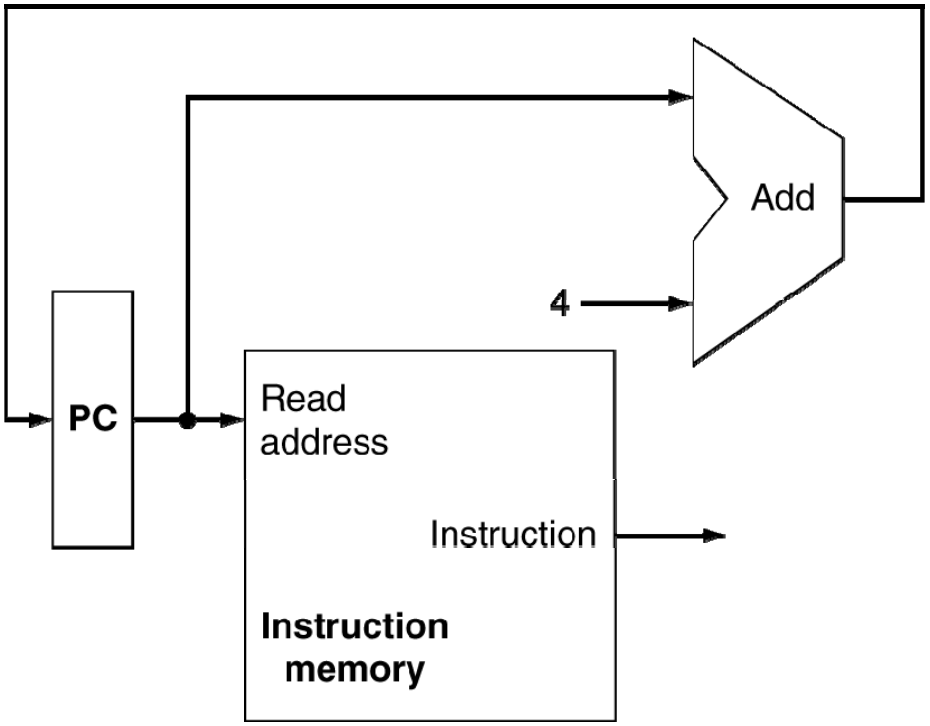
Problem: **Consider the instruction: AND Rd, Rt, Rs. What are the control signals generated by the control unit in this figure ?**

- ANSWER :
  - Regwrite asserted to write
  - Mux (before ALUs) signaled to read from registers and not immediate
  - Mux (before registers) signaled to use ALU and not data memory
  - ALU is signaled to perform AND
  - Branch not asserted
  - Memwrite not asserted
  - Memread not asserted



Selection	Select the true statement for MIPS
A	Registers can be read in parallel with control signal generation
B	Instruction Read can be done in parallel with control signal generation
C	Registers can be written in parallel with control signal generation
D	The main ALU can execute in parallel with control signal generation
E	None of the above

- Answer : A



Problem: **If the only thing we need to do in a processor is fetch consecutive instructions (see figure), what would the cycle time be ? Consider that the logic blocks have the following latencies. Other units have negligible latencies.**

I -Mem	ADD	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2
200 ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

- ANSWER:
- 200ps because
  - I-Mem has larger latency than the Add unit
  - I-Mem and Add are in parallel paths

Suppose EX is the longest (in time) pipeline stage. To reduce CT, we split it in half. Given the following pipeline:

IF ID EX1 EX2 M WB

Assume the input data must be available at the start of EX1 and the output is available after EX2.How many hardware stalls would be required in the following code (assuming hardware forwarding wherever possible)?

```
lw r1, 0(r3)
add r2, r1, r3
```

Selection	Number of stalls
A	0
B	1
C	2
D	3
E	4

- Answer C

Suppose EX is the longest (in time) pipeline stage. To reduce CT, we split it in half. Given the following pipeline:

IF ID EX1 EX2 M WB

Assume the input data must be available at the start of EX1 and the output is available after EX2. How How many hardware stalls would be required in the following code (assuming hardware forwarding wherever possible)?

add r1, r2, r3
add r4, r1, r3

Selection	Number of stalls
A	0
B	1
C	2
D	3
E	4

- Answer B