ECE425: Introduction to VLSI System Design

MP2 Overview

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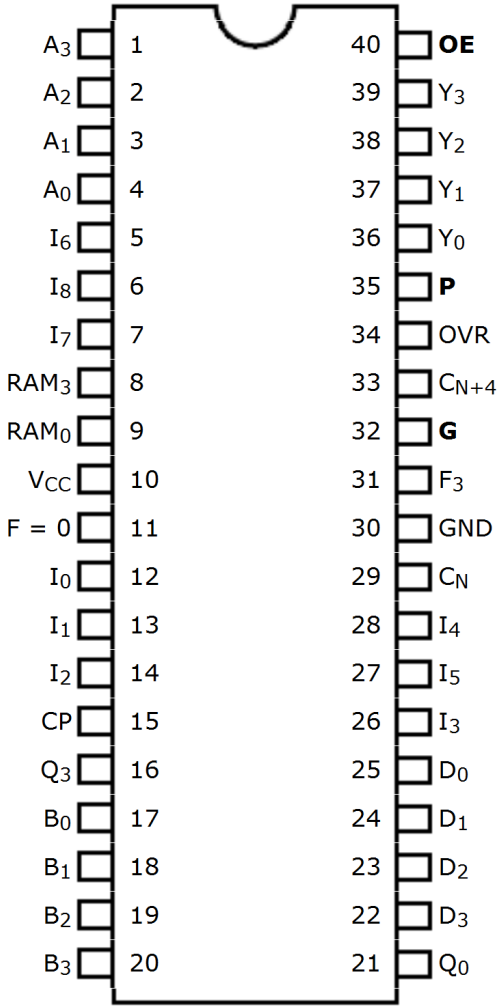
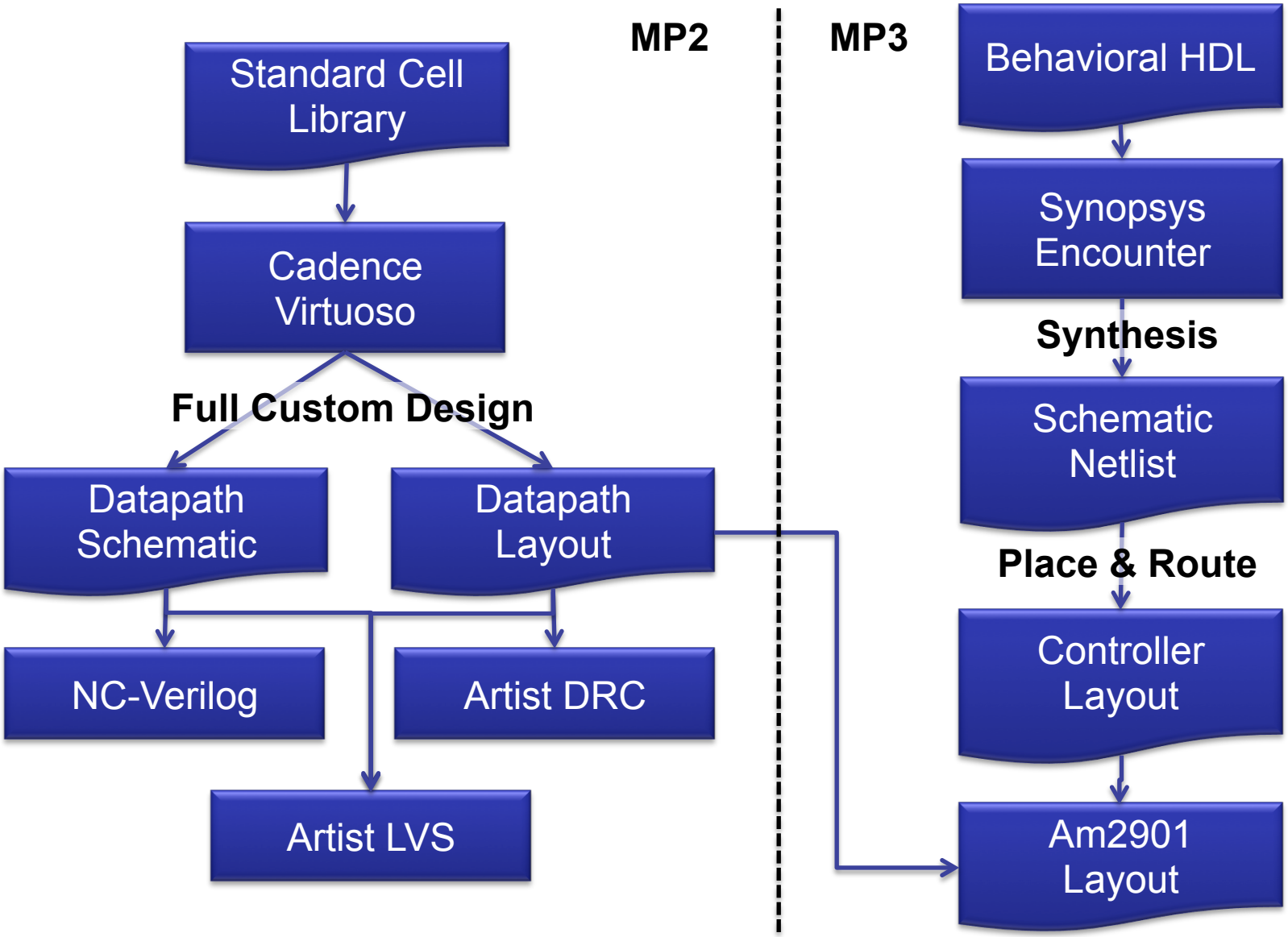
AMD Am2901

- 4-bit *bitslice* datapath unit
- ~500 transistors
- Popular in ~70s
- ~$5 today

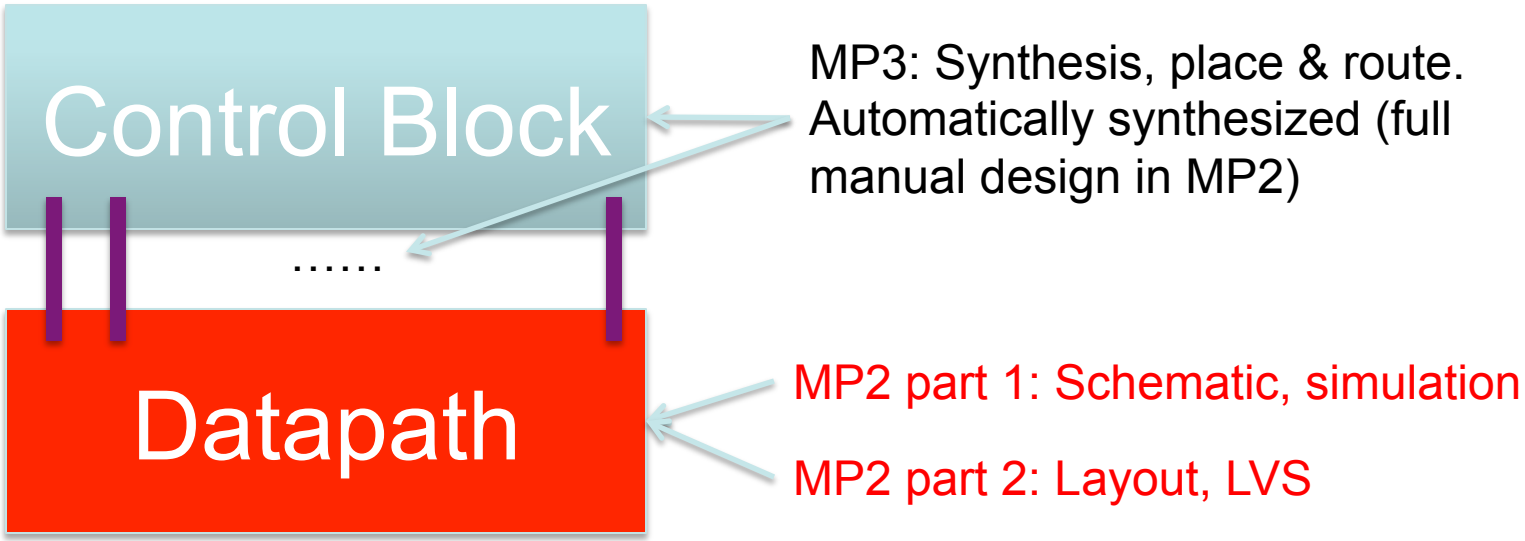


Our ASIC Design Flow

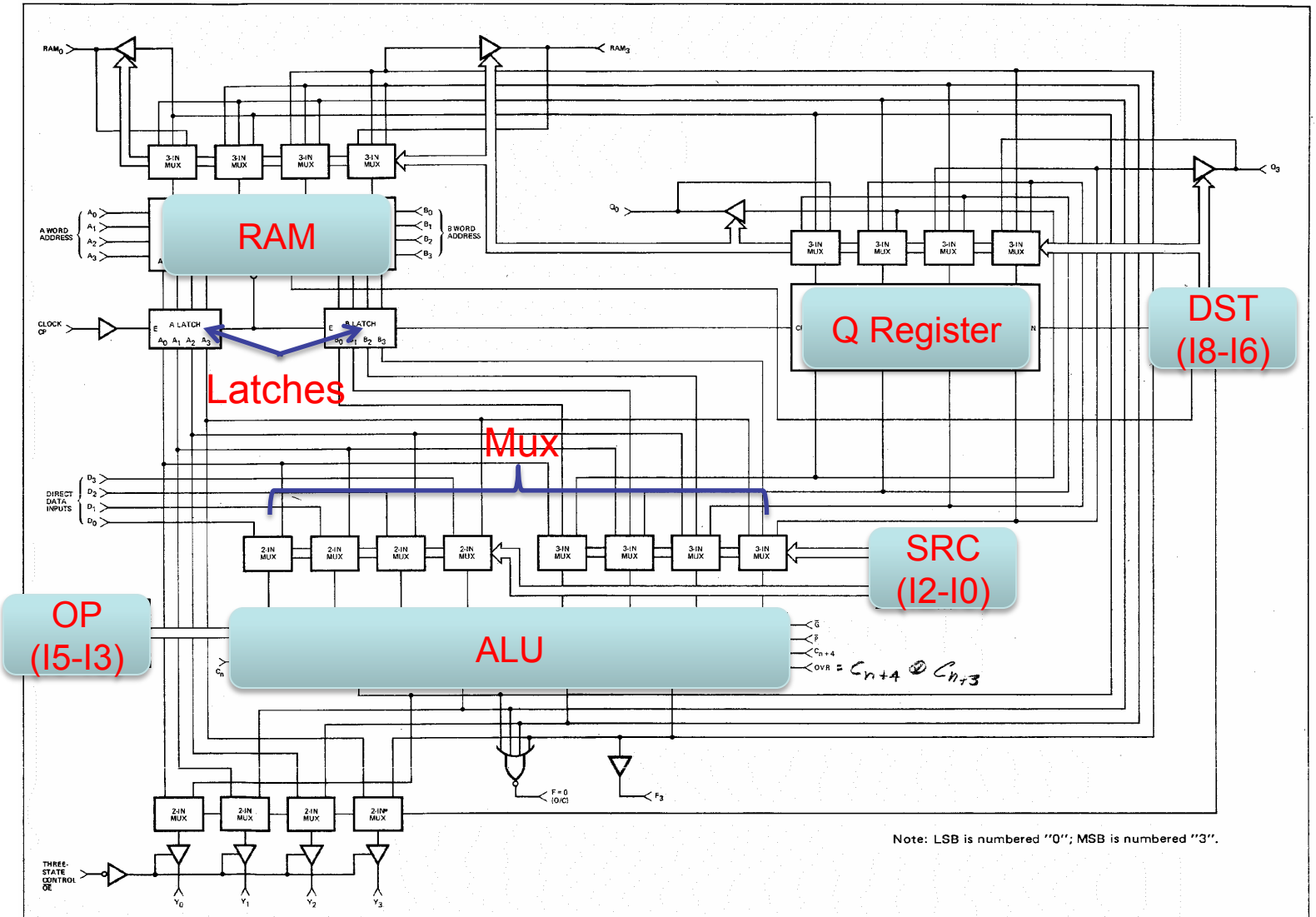


MP2 Overview

- One bitslice does calculation for one bit.
- Datapath: 4-bit
  - 4 bitslices
- Schematic design: MP2 checkpoint 1
- Layout design: MP2 checkpoint 2
- Control logic: MP3



Block Diagram

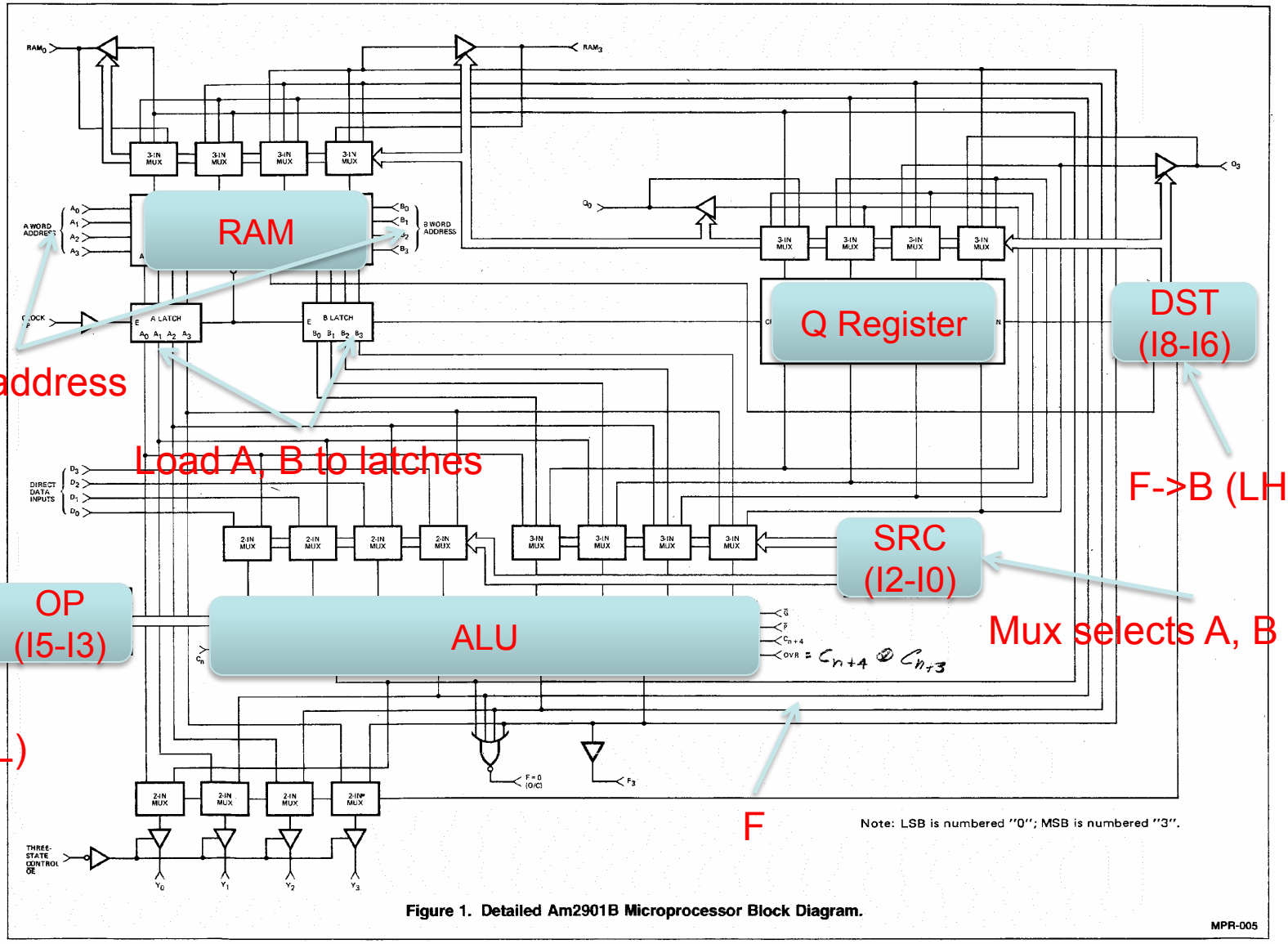


How it works

- 4-bit ALU with 8 operations supported:
  - Plus, Minus, XOR, XNOR, AND, OR
- RAM
  - 16x4-bit (how many bits for the address?)
  - 2-port (R/W)
- Q register
  - Bit shift
  - multiplication/division (via extension module)
- Micro Code: 9 bits (I[0..8])

- Example:
- Code = 011 000 001
  - (I2-I0) SRC: R=A, S=B (address specified by A[3..0], B[3..0])
  - (I5-I3) OP code: R+S
  - (I8-I6) DST: B
- Operation: A+B -> F -> B (write back to B)

Block Diagram



CP1: Schematic Design

- Some templates are already given
- Re-use or redesign your MP1 basic gates
  - NAND, NOR etc.
  - Make sure to create symbol views
- Design the rest part
  - Mux
  - ALU
  - Etc
- You have to carefully design how to implement the ALU functionality, as it will affect your design and layout area later.

Rules

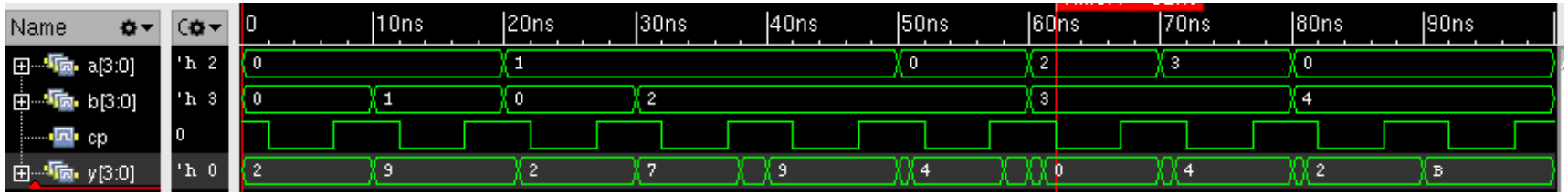
1. Use Complementary static CMOS
   - PMOS + NMOS networks
2. Fan-in: path from gate output to power/ ground <= 3 transistors
3. Combinational logic only: no feed back loops
4. Drive ratio: not required to size the transistors in this MP, just keep pmos 0.72um, nmos 0.36um.

RTL

- We need to provide the control signals to data path:
  - decode the microcode
  - select the register, etc.
- This is done in Control Unit
- In MP2, we do not design the control unit manually, instead, we write RTL codes to specify the functionality
  - Schematic & layout will be synthesized in MP3
- Read the given template file and write your own verilog to complete your design.

Simulation

- Ensure your design works properly
- Run the *test program* provided and compare the output with golden
- The output sequence should be 2, 9, 2, 7, 9, 4, 0, 4, 2, B
- The wave form looks like this…



CP2: Layout

- Once you have a working schematic design, you can create the layout
- MUST follow the rules
  - Control wires on metal 3, data on metal 2, transistor routing on metal 1
  - Metal 2 is HORIZONTAL, metal 3 is VERTICAL
  - More on the MP document
- We will look at your final area

- Your cells should have same height (standard cell)
  - Smaller height: smaller area, but harder to route
  - Have a rough estimation first, you may have to re-design the cells later if this went wrong
  - Safe strategy: allow a larger height first and get it working, then optimize

Design Competition

- Goal: minimize the final area (datapath + controller). Hints:
  1. Minimize #transistors leads to smaller layout
  2. Design cell height carefully to have compact but routable layout
  3. Optimize ALU implementation
  4. Share vdd/gnd between bitslices
  5. Other tricks you learned from MP1

- Bonus (tentative): points towards your final grade
  - 1st place: 2 pts
  - 2nd place: 1.5 pts
  - 3rd place: 1 pts

- Large area is fine. Insanely large is not okay.
  - E.g., you cannot just use a very large cell height to create lots of empty space, which gives you a very easy routing

Final words

- Be organized
  - Build your basic gates first, then use them to build higher level gates
  - Hierarchical design
- One step at a time
  - Make sure each step is correct
  - E.g., don't do simulation/LVS unless you are sure your logic is correct
  - Check and save to synchronize your change
- The document may be long, but it contains every bit of information you need. So read it through carefully.