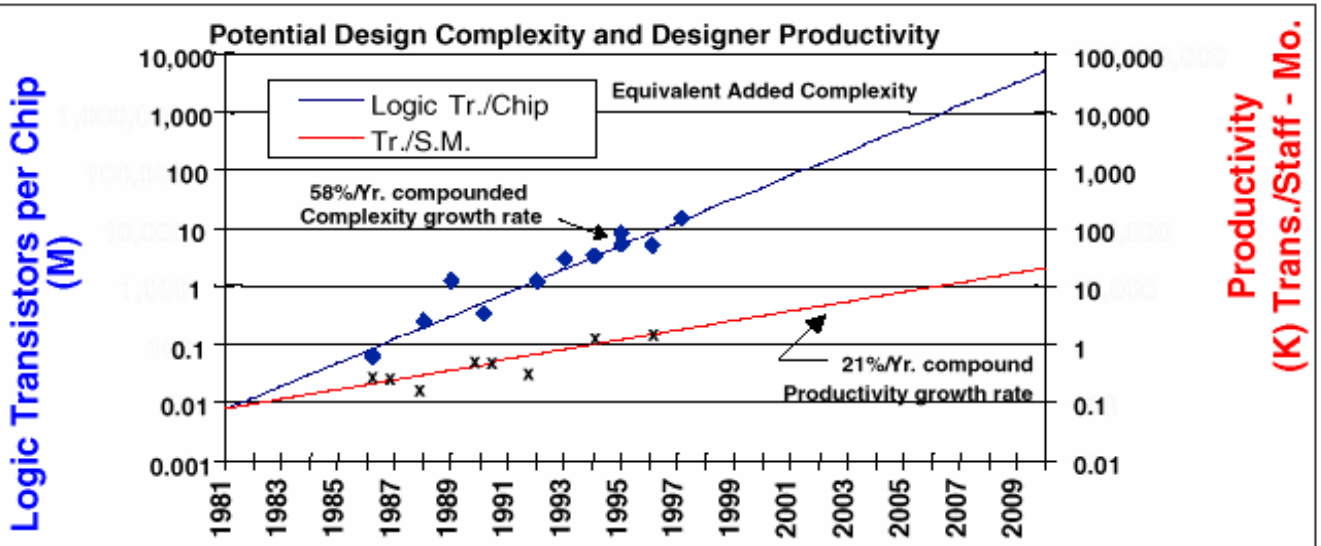
ECE 715
System on Chip Design and Test

Lecture 3

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Design Trend: Productivity Gap



Year	Technology	Chip Complexity	ASIC Frequency
1997	250 nm	50M Tr.	100MHz
1999	180 nm	150M Tr.	200MHz
2002	130 nm	250M Tr.	400MHz
2004	90 nm	500M Tr.	600MHz

Designing a 50M Transistor IC

• Gates Required	~12.5M	
• Gates/Day (Verified)		1K (including memory)
• Total Eng. Days	12,500	
• Total Eng. Years	35	
• Cost/Eng./Year	$200K	
• Total People Cost	$7M	
• Other costs (masks, tools, etc.)		$8M

Actual Cost is $10-15M to get actual prototypes after fabrication.

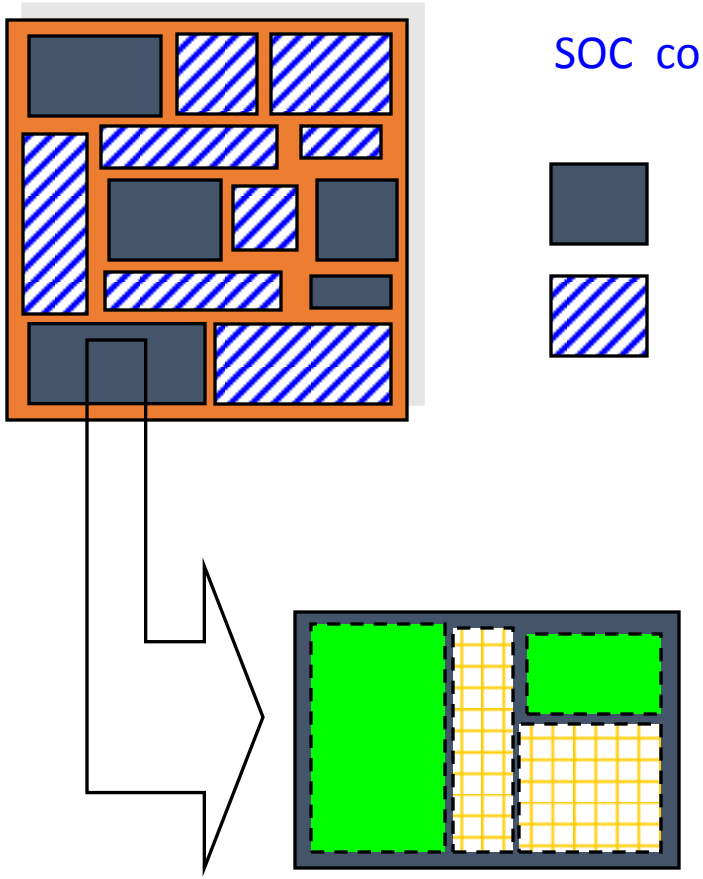
Productivity Gap

- Deep submicron (DSM) technology allows hundreds of millions of transistors to be integrated on a single chip
- Number of transistors that a designer can design per day (~1000 gates/day) is not going up significantly
- New design methodologies are needed to address the integration/productivity issues

$\Rightarrow$ "System on a chip" Design with reusable IP (Intellectual Property)

- new design methodology, IP development
- new HW/SW design and verification issues
- new test issues

SoC Design Hierarchy



SOC consists of new logic blocks and existing IP

New Logic blocks

Existing IP including memory

Each logic block can be implemented by newly designed portion and a re-use portion based on IPs

Newly designed portion

Re-use portion including memory

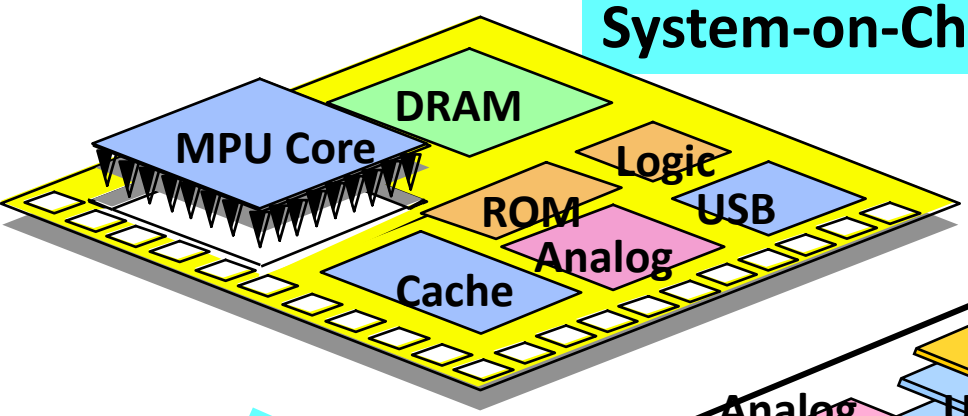
Motivation for SoC Design

What is driving the industry to develop the SoC design methodology?

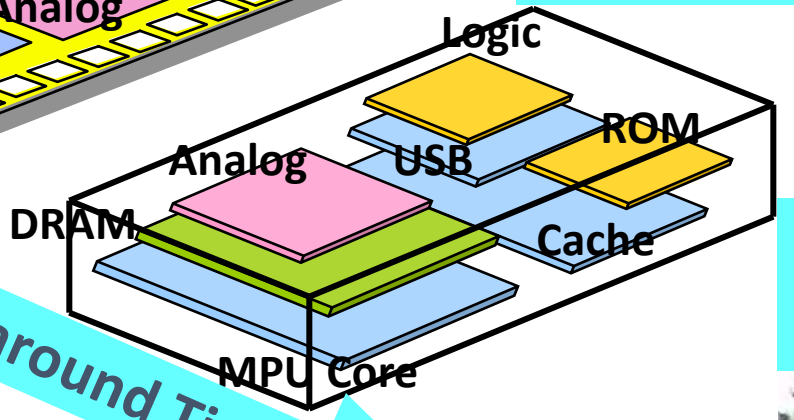
- Higher productivity levels
- Lower overall cost
- Lower overall power
- Smaller form factor
- Higher integration levels
- Rapid development of derivative designs

SoC vs. SiP vs. SoB

System-on-Chip (SoC)



System-in-Package (SiP)

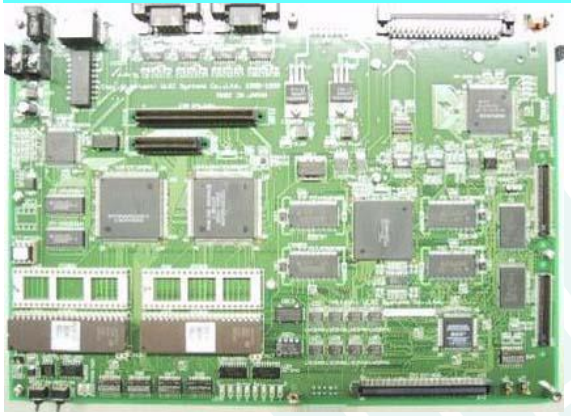


Quick Turn-around Time

Smaller form factor

Lower power, cost

System-on-Board (SoB)



Design Reuse Options

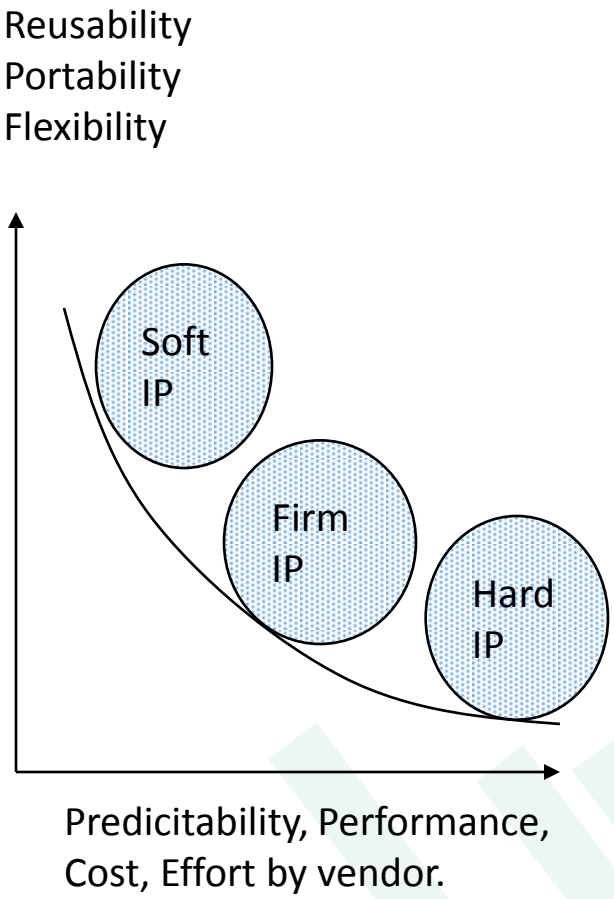
- Option 1: chip-level reuse
  - Fewer chips designed, HW programmable
  - Undifferentiated silicon
- Option 2: processor-level reuse or software reuse
  - Chip = processors + memory
  - Big SW, little hardware model
  - Undifferentiated silicon
- Option 3: widespread reuse
  - High-value, domain specific reusable blocks
  - Differentiated silicon

Defining System-on-Chip

- Definitions:
  - Virtual Socket Interface (VSI) Alliance: *"Highly integrated device. Also known as system on silicon, system- on-a-chip, system-LSI, system-ASIC"*
- Our view of an SoC design is defined by extensive use of reusable IP blocks, and mixed HW/SW design issues:
  - Programmable processor
  - Embedded memory
  - Digital signal processors
  - System bus + interfaces
  - Embedded programmable logic
  - Embedded software
  - Analog components.....

Classification of IP Blocks

- Soft IP (RTL):
  - High flexibility/low predictability
  - Synthesize from hardware description language (HDL)
- Firm IP (gate level):
  - Medium flexibility/medium predictability
  - Gate level netlist that is ready for P&R
- Hard IP (layout level):
  - Low flexibility/high predictability
  - Layout and technology dependent information



Examples of IP Blocks in Use today

- RISC: ARM, MIPS, PowerPC, SPARC
- CISC: 680x0 x86
- Interfaces: USB, PCI, UART, Rambus
- Encryptions: DES, AES
- Multimedia” JPEG coder, MPEG decoder
- Networking: ATM switch, Ethernet
- Microcontroller: HC11, etc.
- DSP: Oak, TI, etc.

SoC is forcing companies to develop high-quality IP blocks to stay in business.

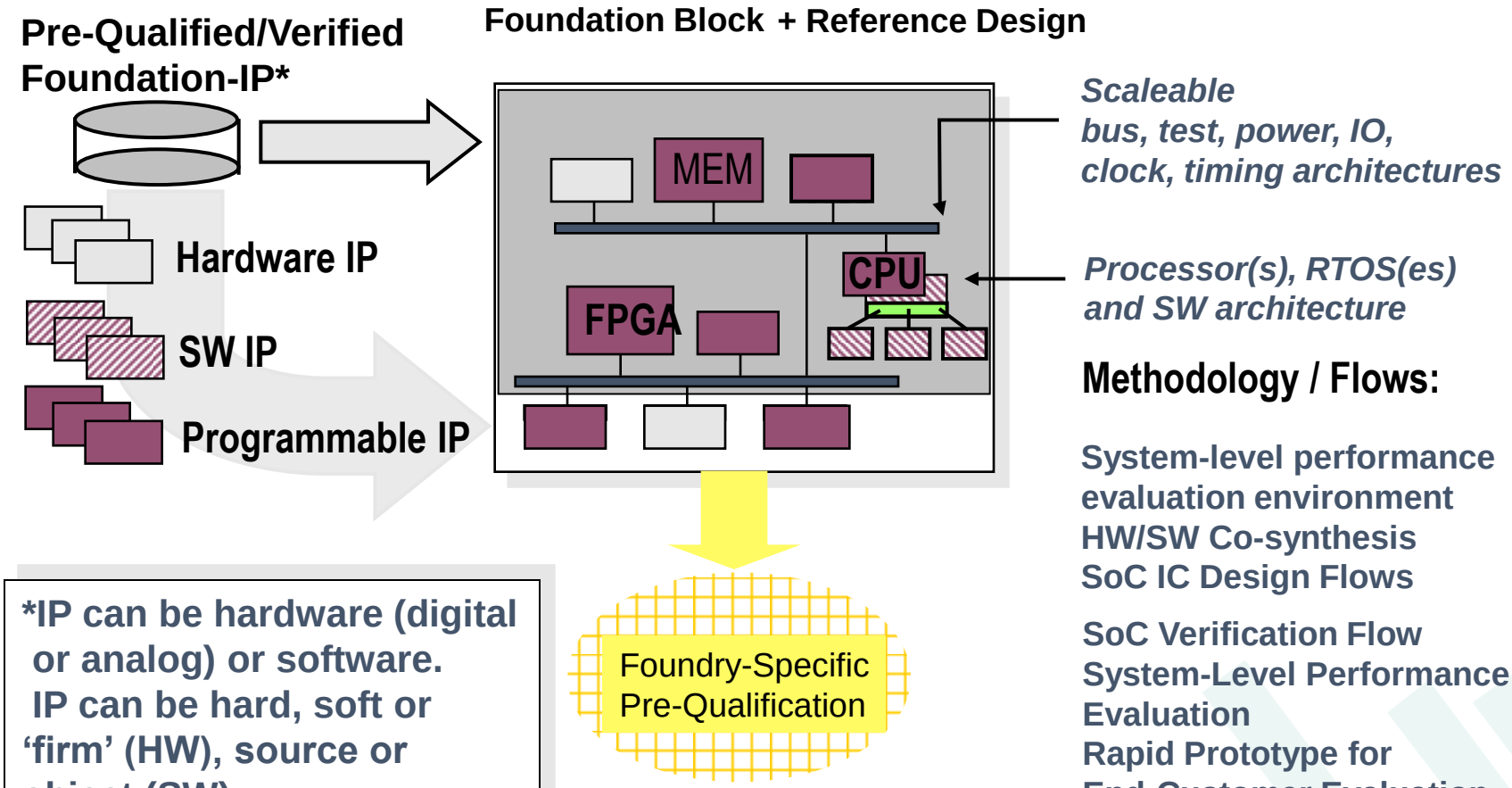
Evolution of Silicon Technology

	1997	1998	1999	2002
Process Technology	0.35 micron	0.25 micron	0.18 micron	0.13 micron
Cost of Fabrication	$1.5 - 2.0 billion	$2.0 - 3.0 billion	$3.0 - 4.0 billion	$4.0 ---- billion
Design Cycle	18-12 months	12-10 months	10-8 months	10-8 months
Derivative Cycle	8-6 months	6-4 months	4-2 months	4-2 months
Silicon Complexity	200-500k gates	1-2M gates	4-6M gates	10-25M gates
Applications	Cellular, PDA, DVD	Set-top boxes wireless PDA	Internet appliances	Ubiquitous computing
Primary IP Sources	Intragroup	Intergroup	Intercompany	Intercompany Interindustry

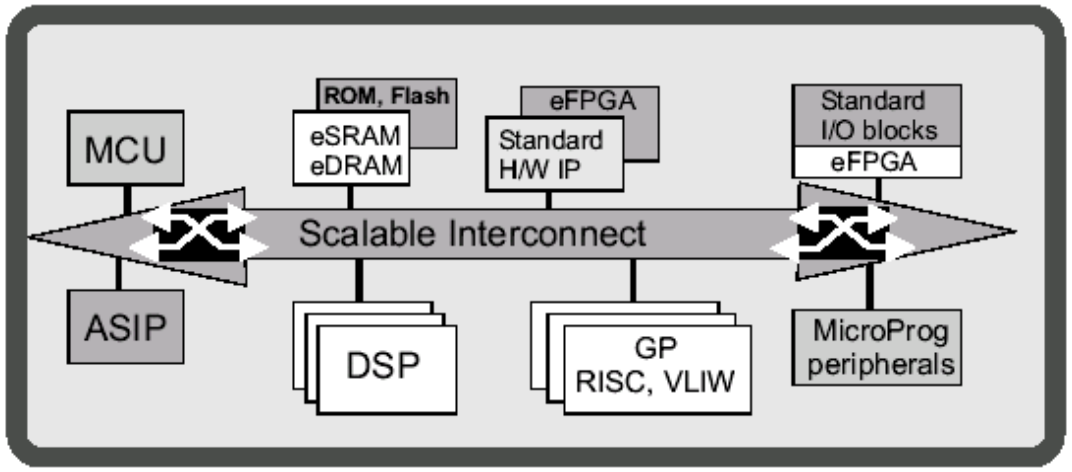
What is a Platform?

- **What is platform?**
  - A stable core-based architecture for a target application
  - Can be rapidly extended and customized
- **What are the benefits of a platform?**
  - Major benefit
    - Increased productivity
  - Derivative designs can be easily created
    - Using software or hardware modifications
    - Reduces the design time and increasing success rate
  - Diverse applications each require a different platform
    - Example of WPAN application
      - Bluetooth platform
      - AMBA bus and ARM TDMI CPU based

SoC Platform Design Concept

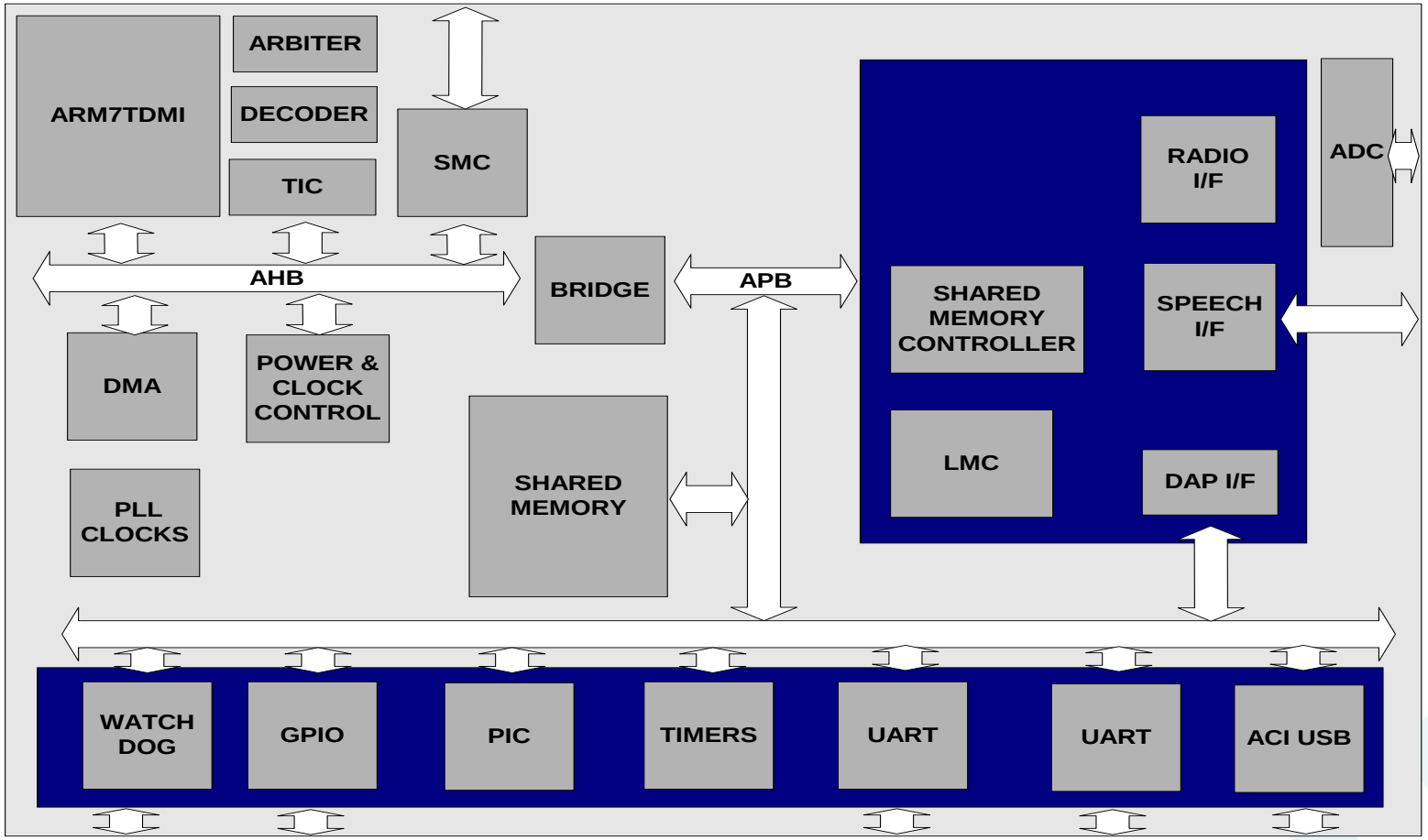


MP-SoC Platforms



- Both general purpose processors and Application-specific processors will be important
- Embedded FPGA (eFPGA) will complement the processors, however power is a concern

Tality Bluetooth Platform



Design Issues

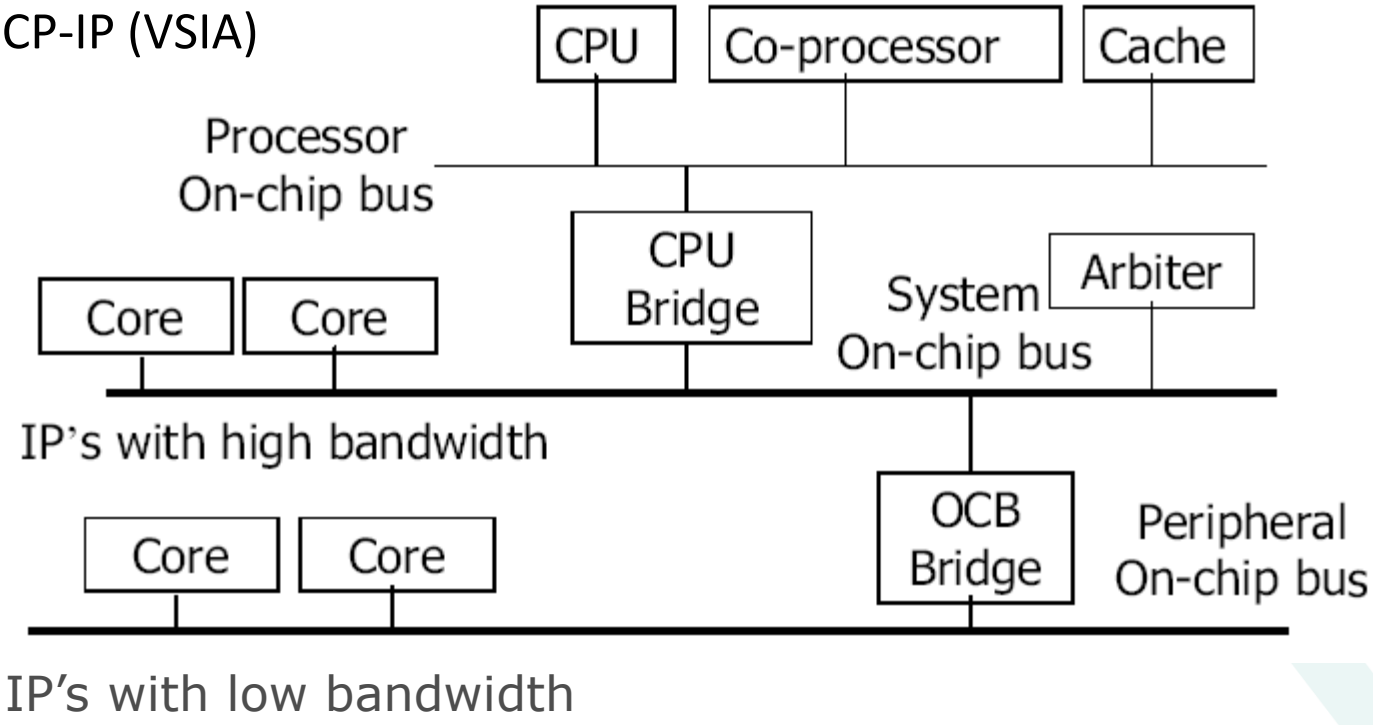
- Non-net listed cores
- Layout dependency
- Aspect ratio misfits
- Hand-crafted layouts
- Clock redistribution
- Timing re-verification
- ……

Efforts in Standardization

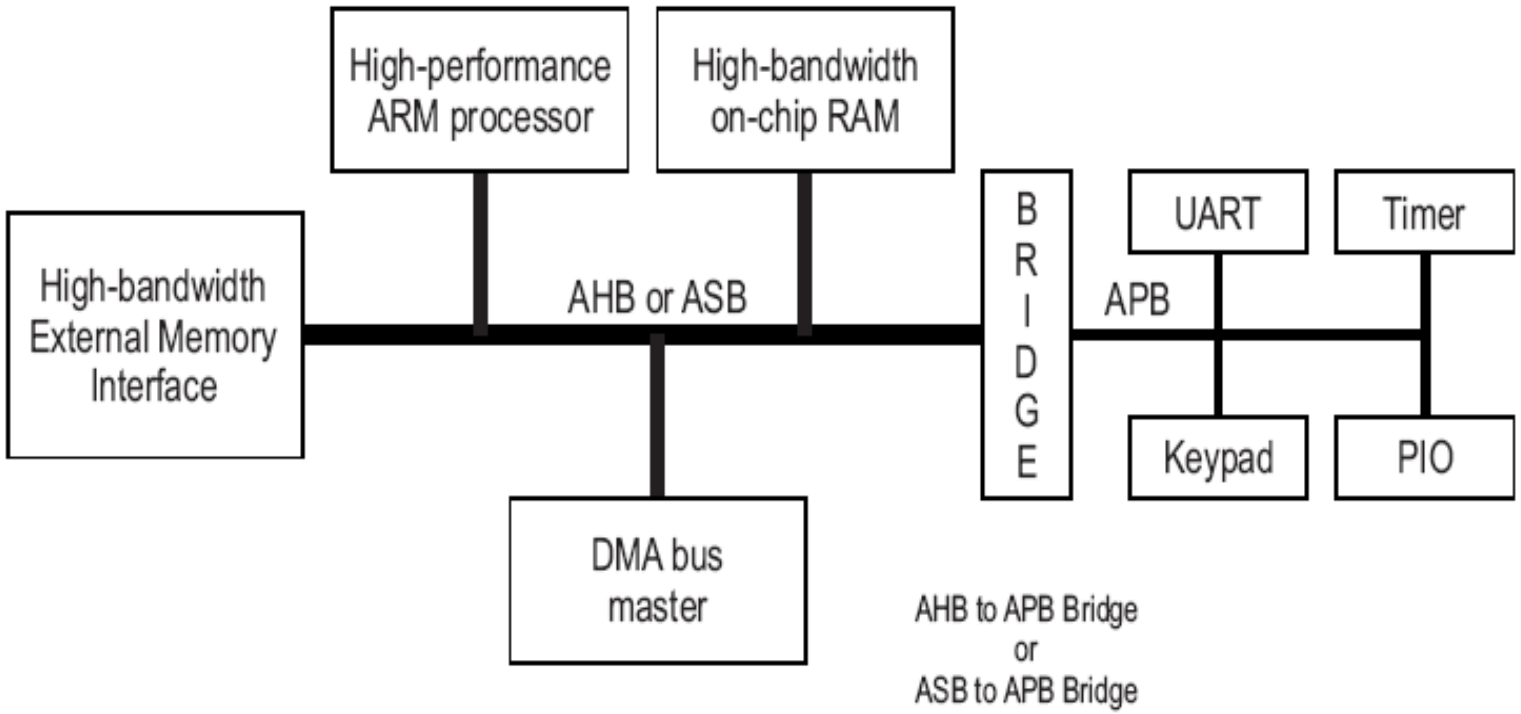
- Defacto bus standards – AMBA, CoreConnect, etc.
- VSIA is involved in developing standards in SoC design to promote widespread use
  - on-chip bus attributes
  - IP design exchange format
  - specifications for signal integrity, soft/hard IP modeling, functional verification, test data formats
  - documentation standards
  - test access architecture standard
  - VCID for tracking IP
  - IP protection, IP quality
- IEEE testing standard (P1500)

On-chip Standardized Bus Structures

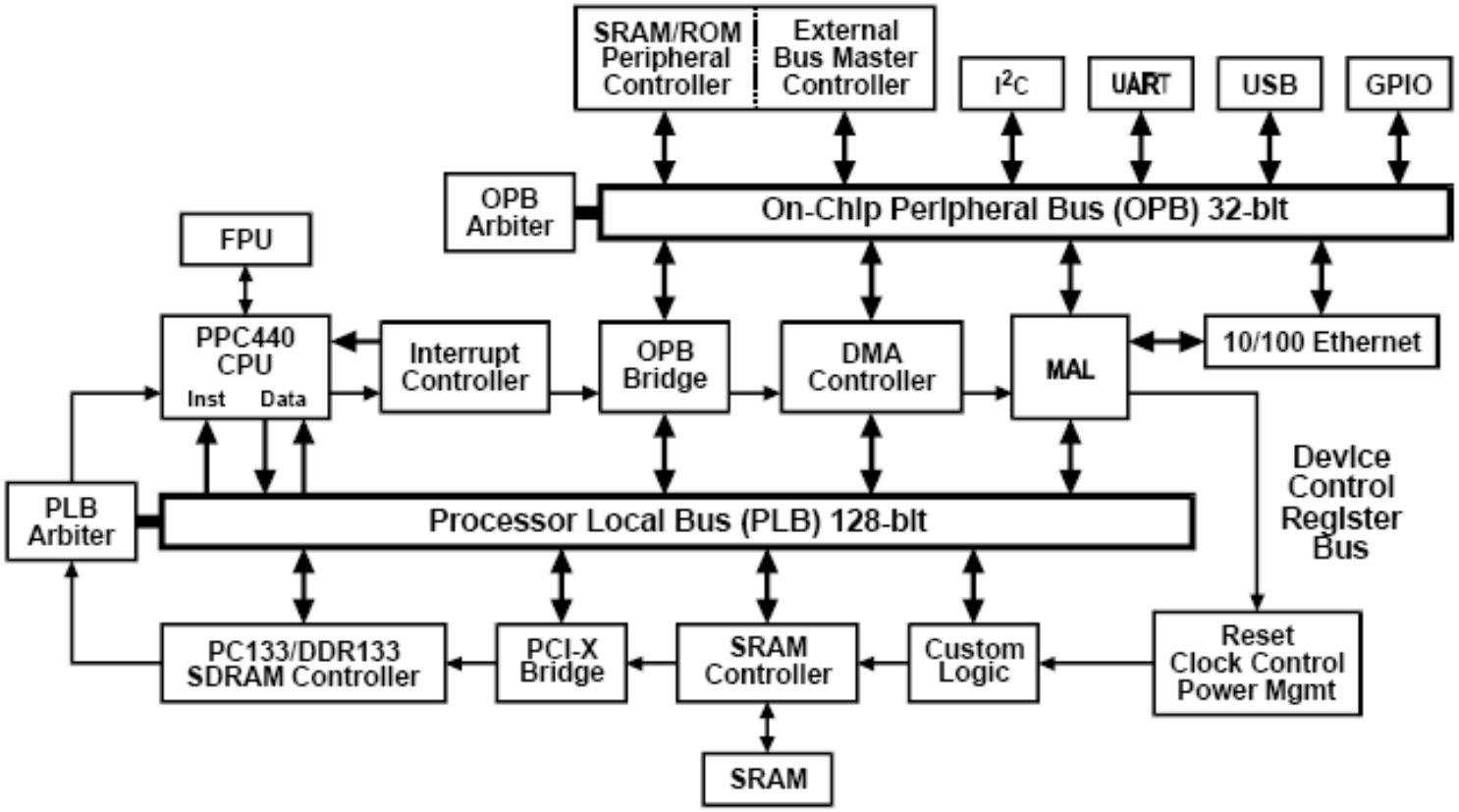
- AMBA (ARM)
- Core Connect (IBM)
- OCP-IP (VSIA)



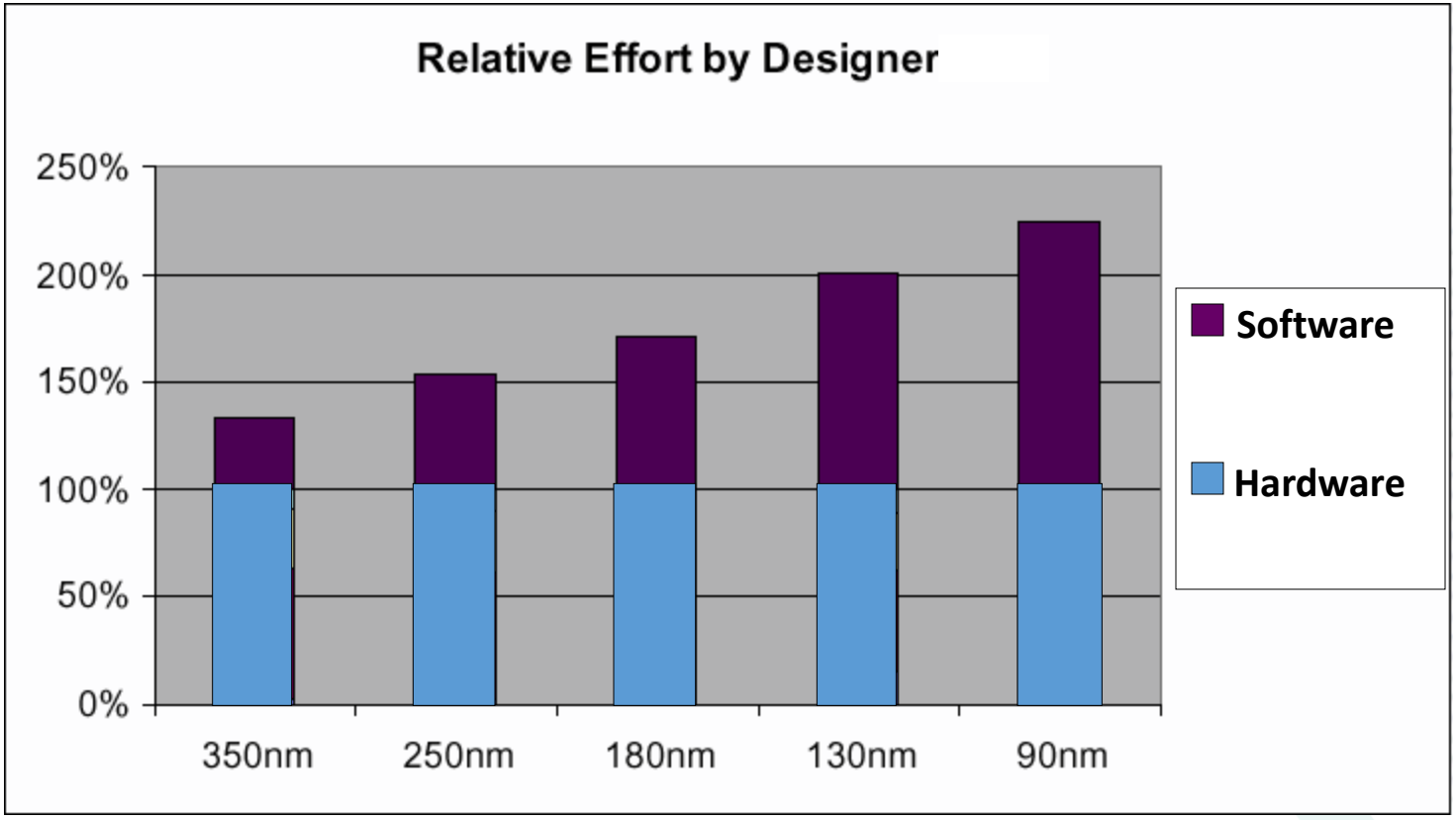
ARM AMBA


High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth External Memory Interface
AHB or ASB
B R I D G E
APB
UART
Timer
Keypad
PIO
DMA bus master
AHB to APB Bridge
or
ASB to APB Bridge

IBM Coreconnect



Design Cycle Trends



*** Software costs overtake total hardware costs at 130nm**

80% of System in Embedded SW

- Hardware is not sufficient to build an SoC platform
- 70-80% of the system will be implemented in software
  - Product differentiation will move to software from silicon
  - Many IC companies hire more software designers than IC designers
- Standard platforms with software differentiation will be the trend
  - Example: in Set-top box market, manufacturers are converting from 7 different chips to 1 chip with 7 different application SW

Levels of Abstraction

- System application design
- Multi-processor SoC (MP-SoC) platform design
- High level IP block design
- Semiconductor technology & basic IP

Interconnect

- Ease of Communication
- a regular, plug-and-play methodology for interconnecting various hardwired, reconfigurable or **S/W** programmable IP's.
- Buses won’t be sufficient
- Network on chip is a promising solution

Summary of SoC

Driven by:

- Need for New Methodology to Handle Design Complexity
- Need for Increased Productivity
- Need for Lower System Power
- Need for Reduced System Size and Costs

Driver for:

- Development and Use of Industry-wide Standards
- Improved Quality of IP blocks
- Focus on Higher Level HW/SW Issues

Outstanding Issues:

- Deep Submicron Physical Design Issues
- Development of SoC flows (HW/SW co-design)
- Verification and Test Complexity