ECE 715
System on Chip Design and Test

Lecture 9: Power and Clock Distribution

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Purpose of Power Distribution

- Goal of power distribution system is to deliver the required current across the chip while maintaining the voltage levels necessary for proper operation of logic circuits
- Must route both power and ground to all gates
- Design Challenges:
  - How many power and ground pins should we allocate?
  - Which layers of metal should be used to route power/ground?
  - How wide should be make the wire to minimize voltage drops and reliability problems
  - How do we maintain V_{DD} and Gnd within noise budget?
  - How do we verify overall power distribution system?

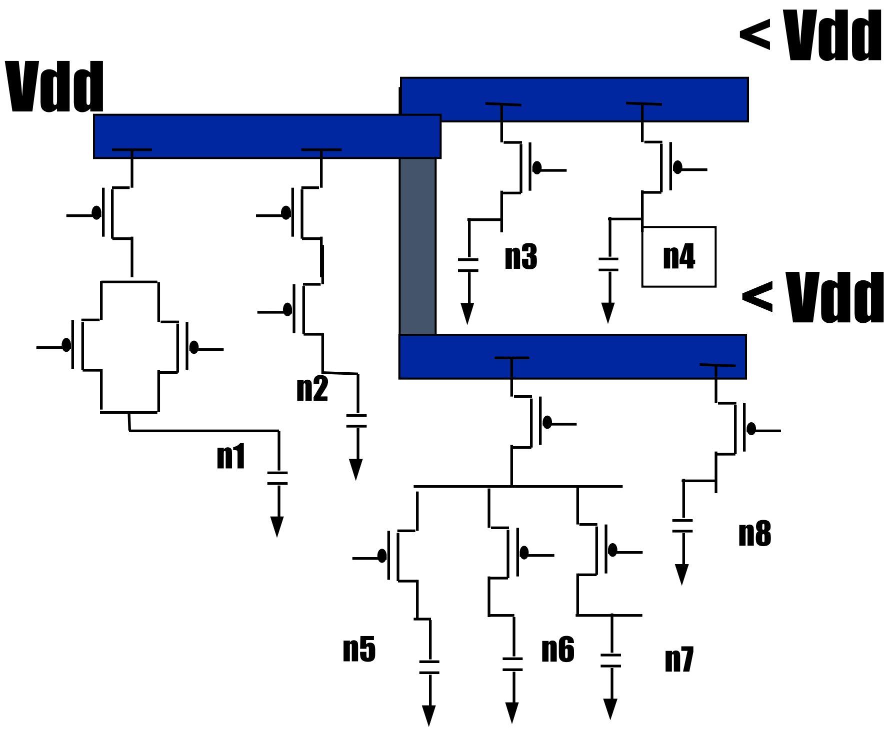
Design Example

- Target Impedance of the power grid

$$Z = \frac{V_{DD} \times (Fractional\,NoiseBudget)}{I_{DD}}$$

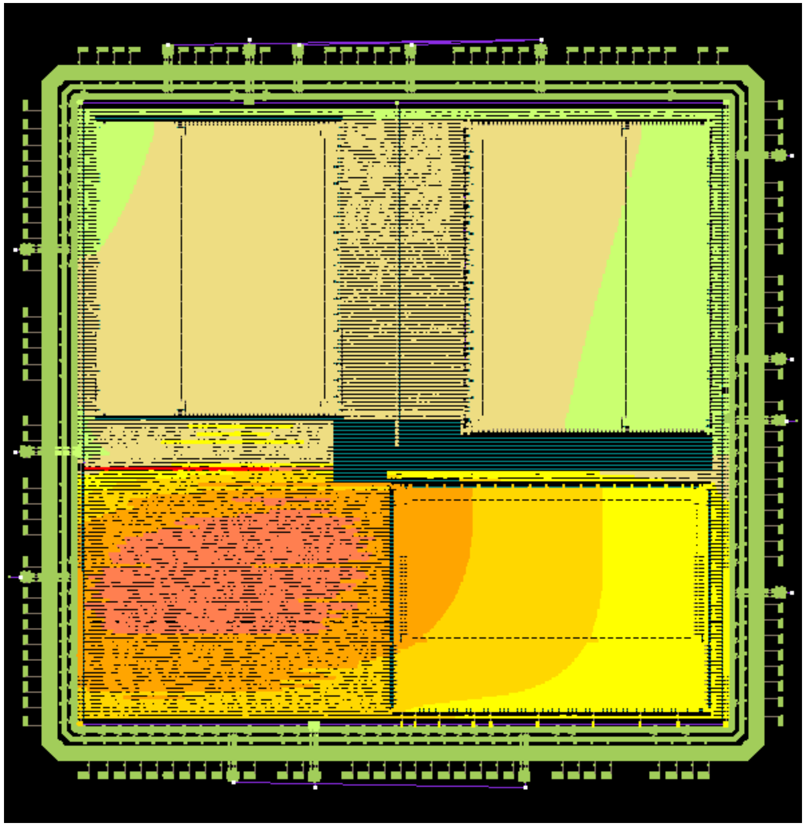
- For a supply voltage of 1.2 V and a supply current of 100 A, with a 10 % noise budget the power grid impedance can be 1.2 mΩ

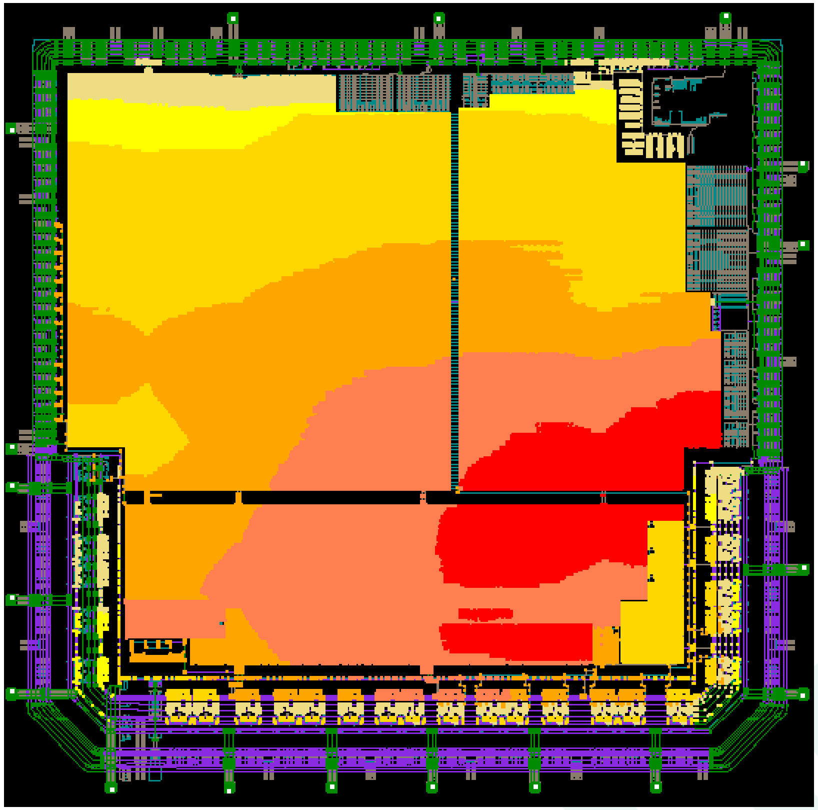
Power Distribution Issues - IR Drop



- Narrow line widths increase metal line resistance
- As current flows through power grid, voltage drops occur
- Actual voltage supplied to transistors is less than Vdd
- Impacts speed and functionality
- Need to choose wire widths to handle current demands of each segment

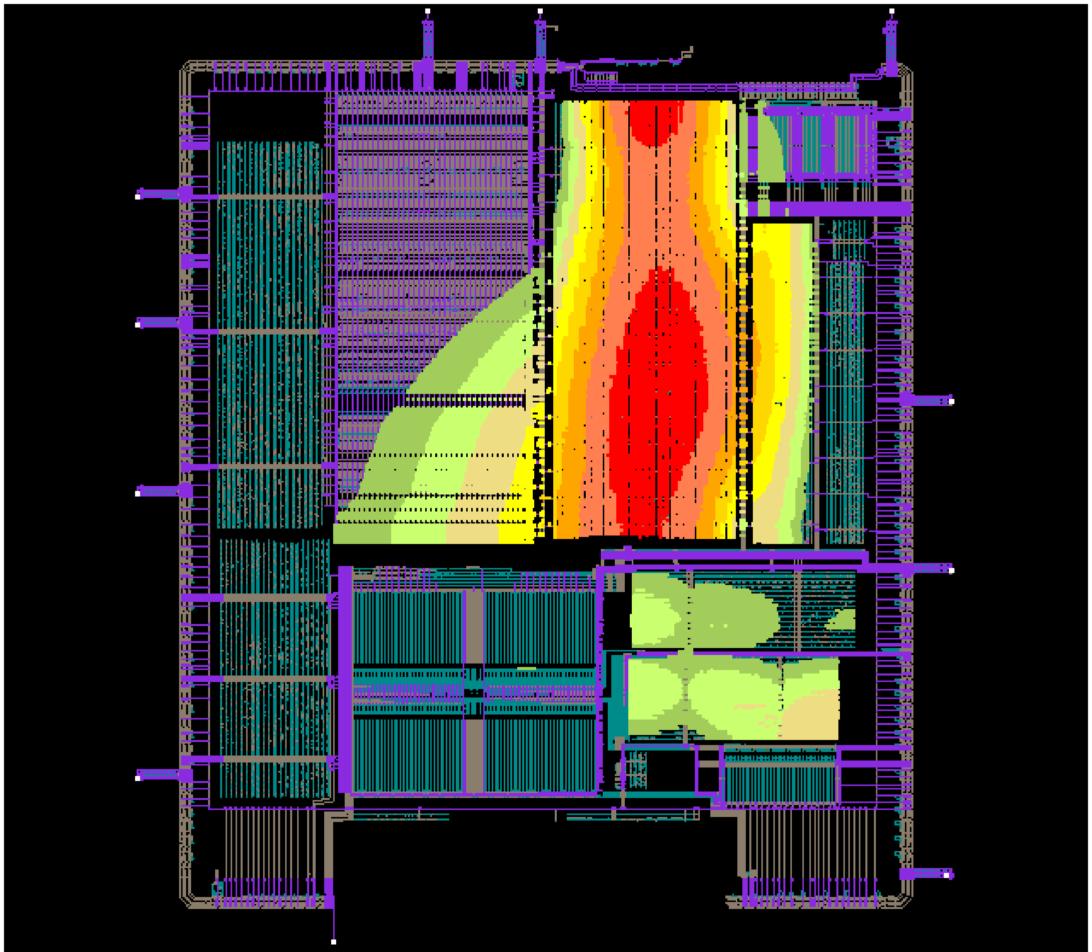
Block Interaction yields IR Drop





Plots courtesy of Simplex Solutions, Inc.

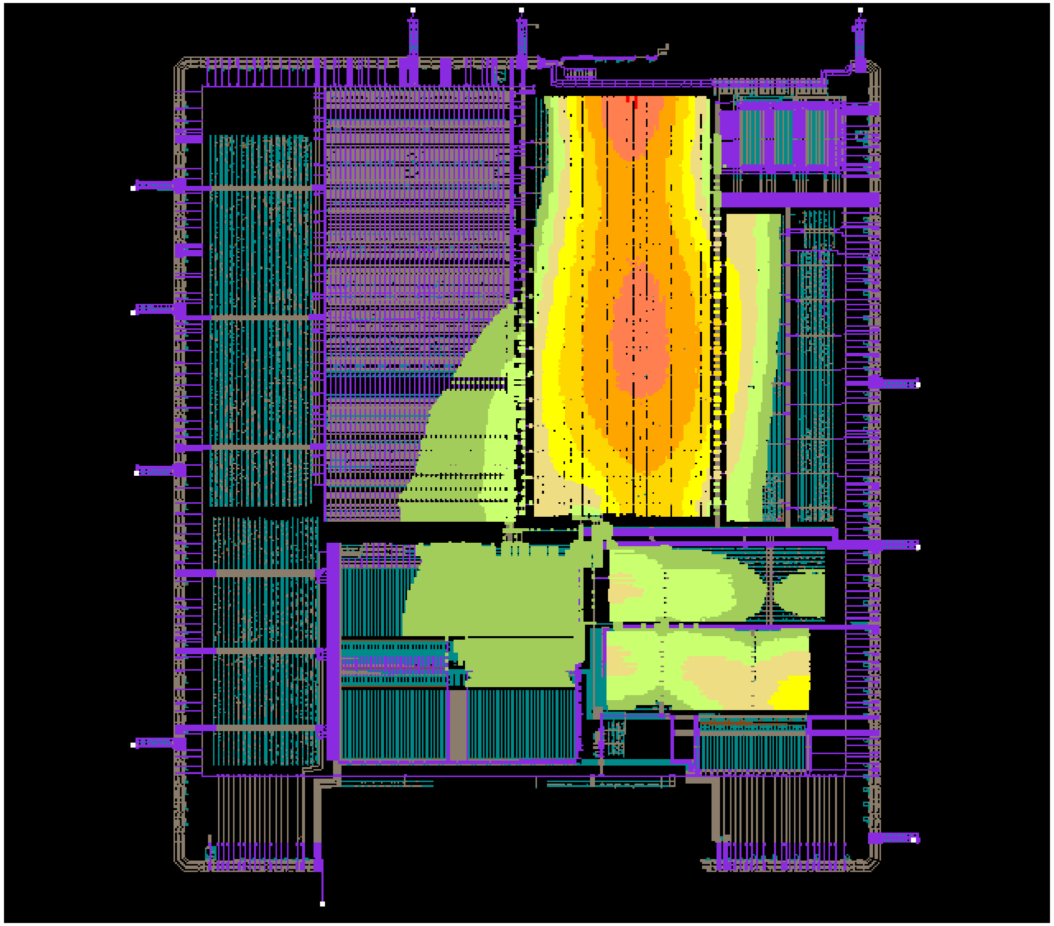
Power Grid Issues – Static IR Drop



- Block placement and global power routing determines IR drop on the chip
- Possible solutions
  - Rearrange blocks
  - More Vdd pins
  - Connect bottom portion of grid to top portion

Plot courtesy of Simplex Solutions, Inc.

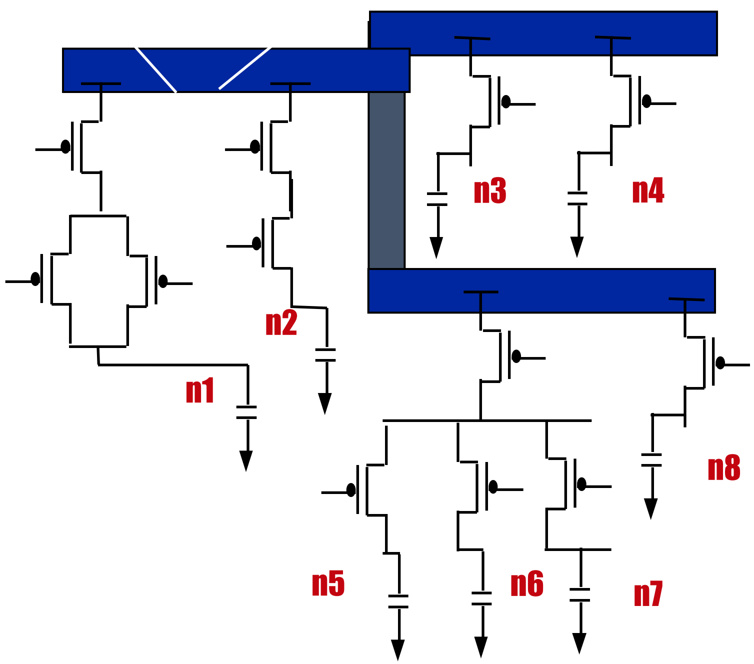
Power Grid Issues – Static IR Drop



- If we connect bottom portion of grid to top portion, the IR drop is reduced significantly
- However, this is only one part of the problem
- We must also examine electromigration

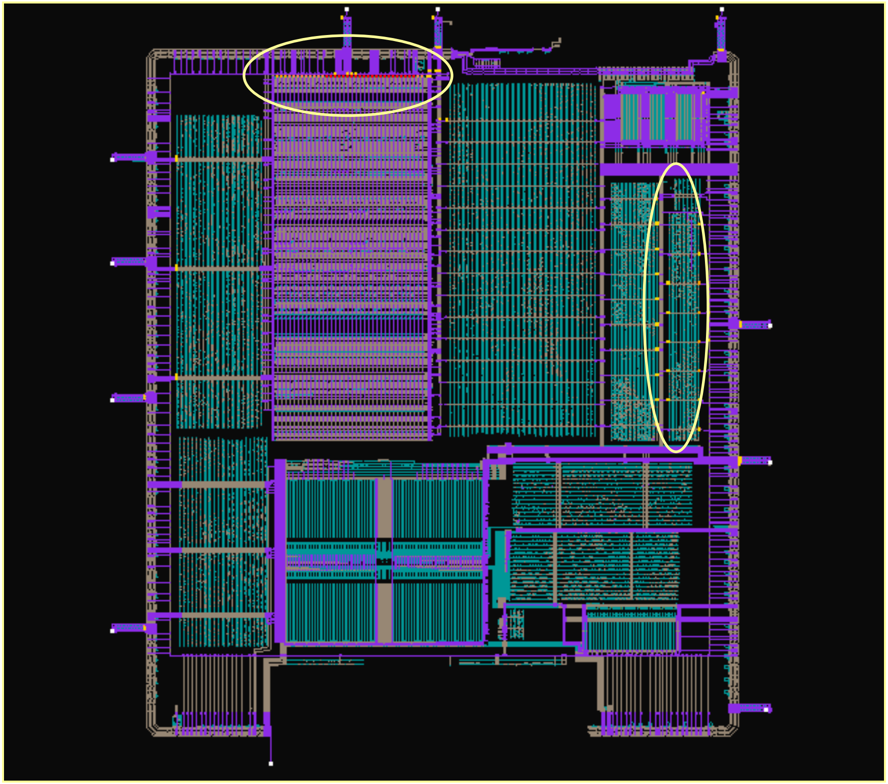
Plot courtesy of Simplex Solutions, Inc.

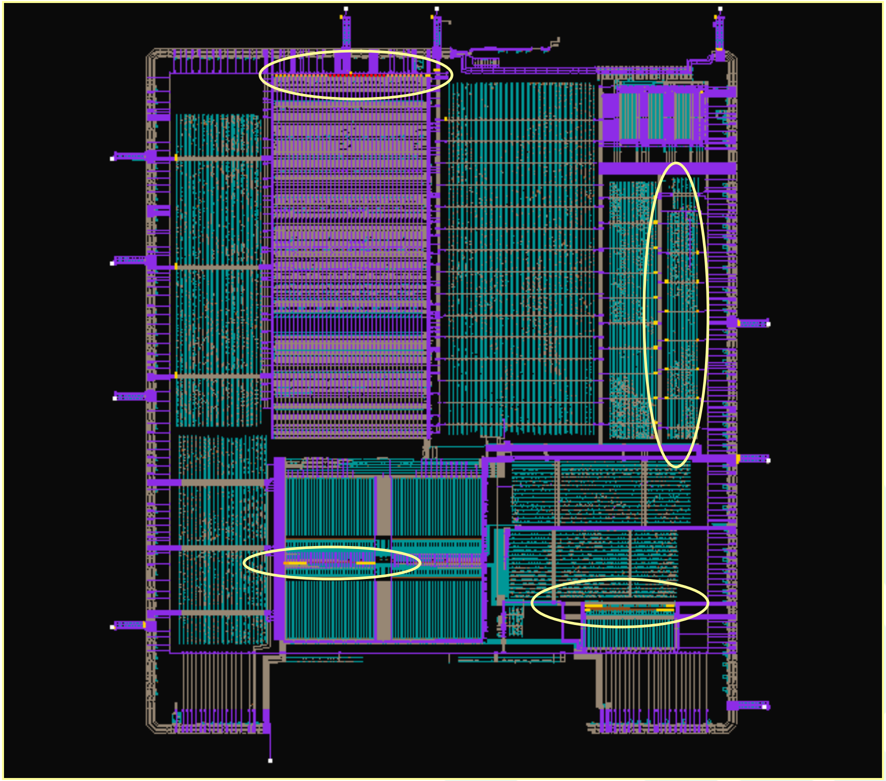
Power Grid Issues - Electromigration



- As current flows down narrow wires, metal begins to migrate
- Metal lines break over time due to metal fatigue
- Based on average/peak current density
- Need to widen wires enough to avoid this phenomenon

Case Study – IR and EM Tradeoff



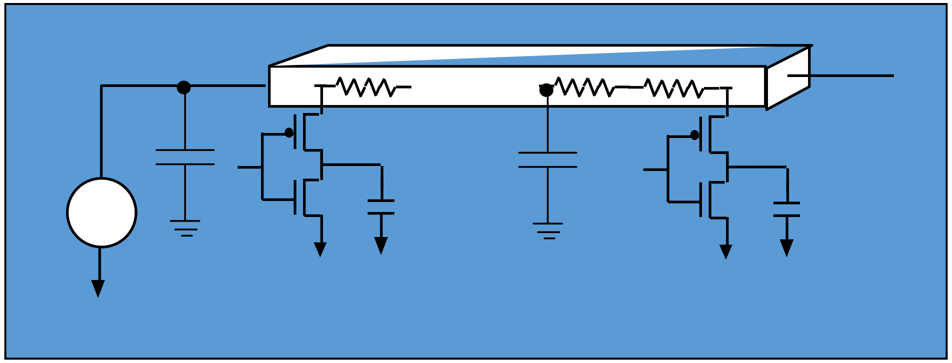


Ldi/dt Effects in the Power Supply

- In addition to IR drop, power system inductance is also an issue
- Inductance may be due to power pin, power bump or power grid
- Overall voltage drop is:

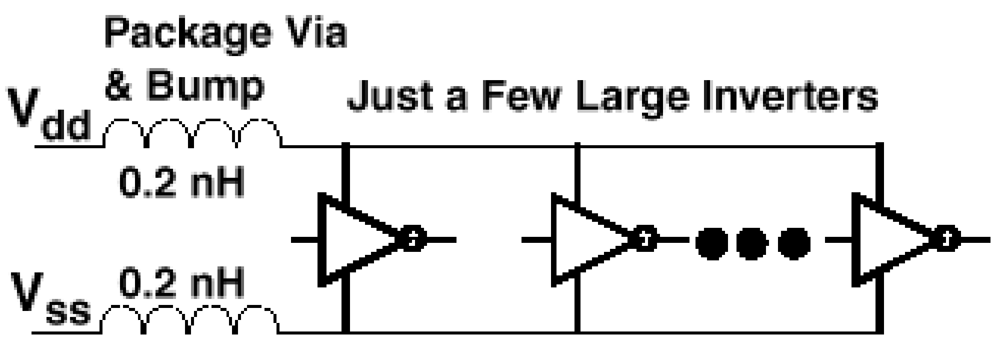
$$V_{drop} = IR + Ldi/dt$$

- Distribute decoupling capacitors (decaps) liberally throughout design
  - Capacitors store up charge
  - Can provide instantaneous source of current for switching



On-chip Decoupling Caps

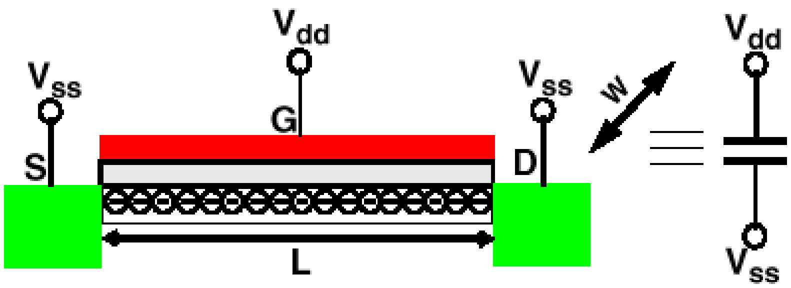
- On-chip decaps help to stabilize the power grid voltage
- First line of defense against noise which can extend beyond 10GHz
- Simple Example:



  - Drop across inductors = 2 x L x di/dt = 2 x 0.2nH x 20mA/100ps = 80mV (problematic if supply is 1.2V)
- Actual power pad or bump may need to support thousands of inverters
- Use capacitors to supply instantaneous charge to inverters

Making a Decoupling Cap

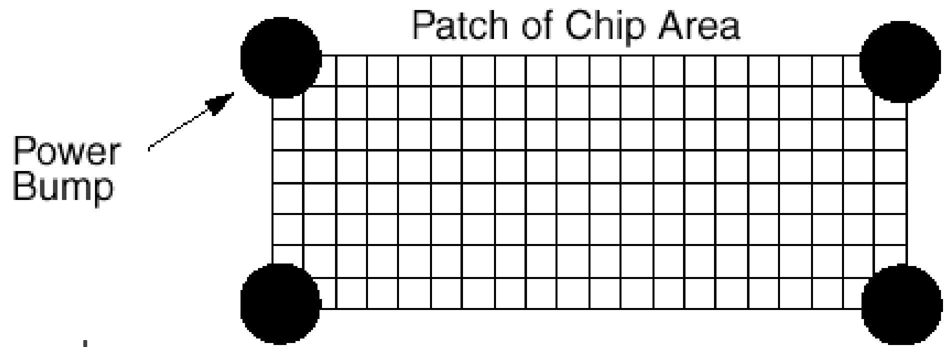
- Decaps are basically NMOS transistors. Top plate is polysilicon, bottom-plate is inverted channel, insulator is gate oxide.
- Connect poly to Vdd and source/drain to Vss



- Low-frequency capacitance is roughly C_{OX} W L.
- Since these are large capacitance to be used at high frequencies, more accurate representation is needed

How much Decoupling Cap?

- To estimate required decap value, run SPICE on patch of chip area with power grid, part of logic block, and sprinkle of decaps



- Amount of decap depends on:
  - Acceptable ripple on Vdd-Vss (typically 10% noise budget)
  - Switching activity of logic circuits (usually need 10X switched cap)
  - Current provided by power grid (di/dt)
  - Required frequency response (high frequency operation)
  - How much decap exists (non-switching diffusion, gate, wire caps)

Simulation with Decoupling Caps

- Plot center region of grid
- Local Vdd-Vss in worst-case location in patch (center)
- First dip can be dealt with by a low-frequency on-chip voltage regulator and low-frequency decaps
- Steady-state ripple is controlled by high-frequency decoupling caps
- Adjust location of decaps until the ripple is within noise budget