ECE 715
System on Chip Design and Test

Lecture 10

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
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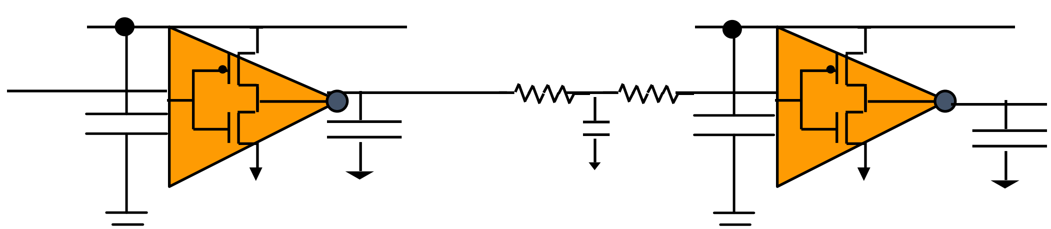
Designing Power Distribution

- Floorplanner should be aware of IR+Ldi/dt drop and EM problems and design accordingly
  - Requires knowledge of current distributions and voltage drop constraints of blocks being placed
- Provide adequate number of V_{DD} and Gnd pins
- Route power distribution system according to current demands of the blocks
- Widen wires based on expected current density in branches
- Distribute decoupling capacitors liberally throughout design
- Verify full chip with IR/EM tools

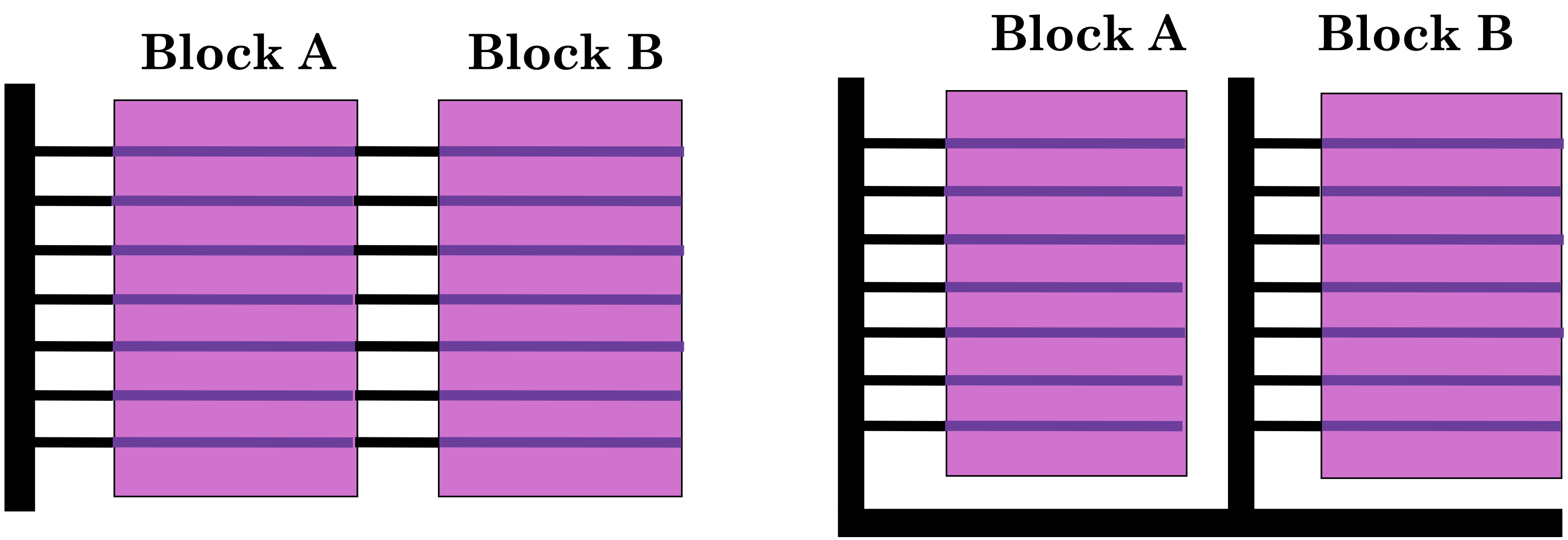
Reducing the Effects of IR drop and Ldi/dt

- Stagger the firing of buffers (bad idea: increases skew)
- Use different power grid tap points for clock buffers (but it makes routing more complicated for automated tools)
- Use smaller buffers (but it degrades edge rates/increases delay)
- Make power busses wider (requires area but should do it)
- Use more Vdd/Vss pins; adjust locations of Vdd/Vss pins
- Put in power straps where needed to deliver current
- Place decoupling capacitors wherever there is free space
- Integrate decoupling capacitors into buffer cells

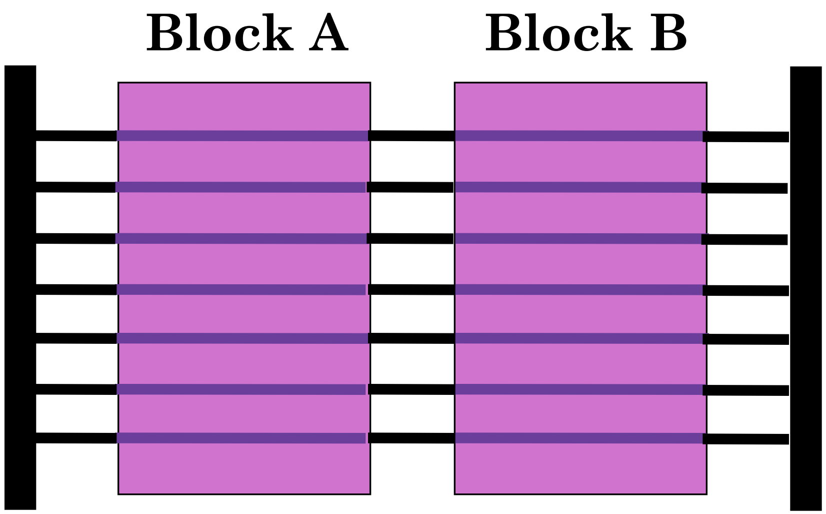


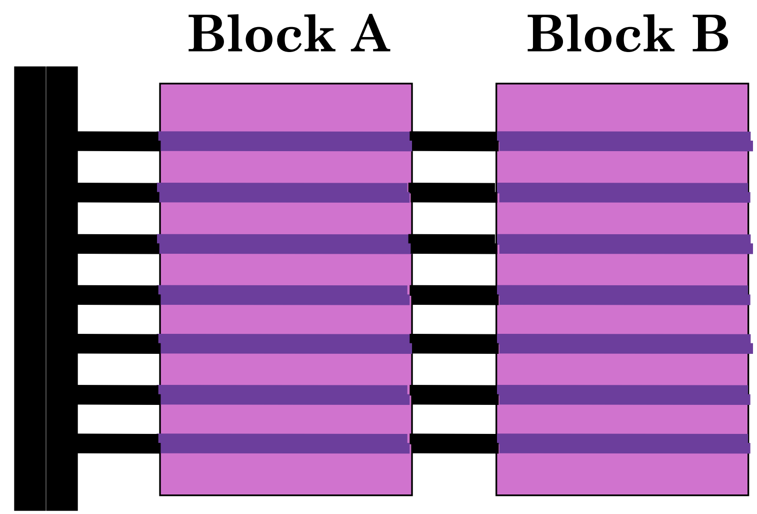
These caps act as decoupling caps when they are not switching

Power Routing Examples

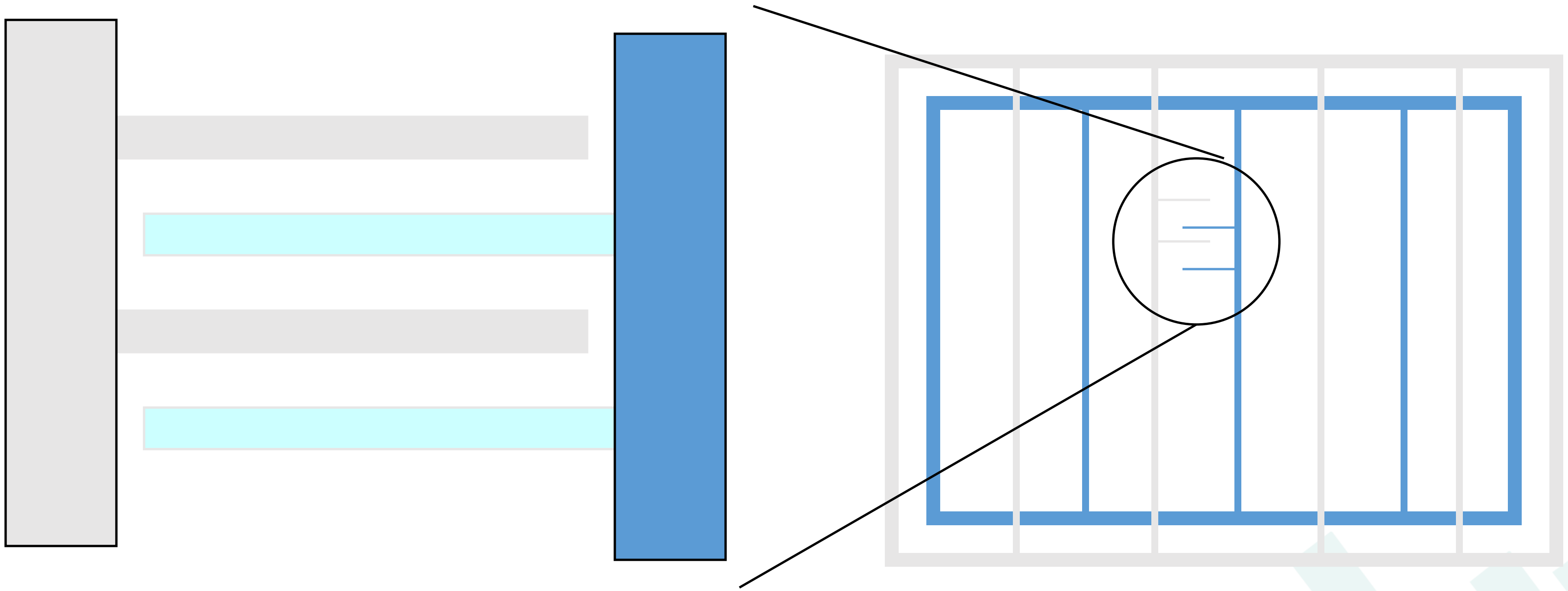


Simple Routing Examples





Interleaved Power/Ground Routing



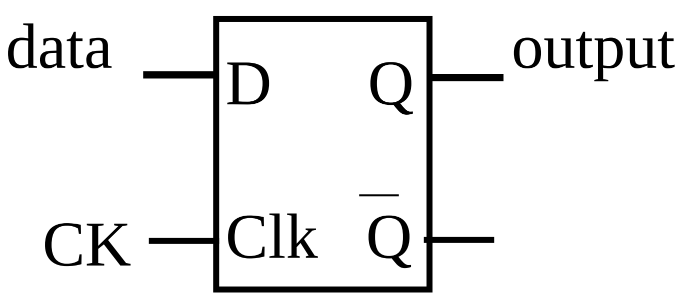
Interleaved Vdd/Vss

Flip-Flop and Clock Design

- Flip-flops and latches are used to gate signals in sequential logic designs.
- The critical parameters of setup and hold times
- Clock design is also a complex issue in DSM due to RC delay components in the interconnect and the power dissipation.
- We will look at clock trees, H-trees and clock grids.
- An overall examination of the issues of clocks skew, IR drop and signal integrity, and how to manage them using circuit techniques.
- Let’s start by revisiting the expected limits of clock speed

Clocked D Flip-flop

- Very useful FF
- Widely used in IC design for temporary storage of data
- May be *edge-triggered* (Flip-flop) or *level-sensitive (transparent* latch*)*



D	Q_{n+1}
0	0
1	1

Latch vs. Flip-flop

Latch (level-sensitive, transparent)

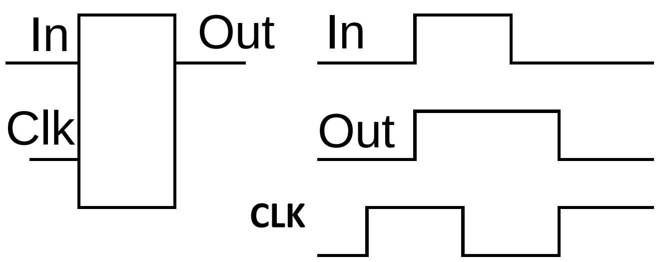
When the clock is high it passes **In** value to **Out**

When the clock is low, it holds value that **In** had when the clock fell

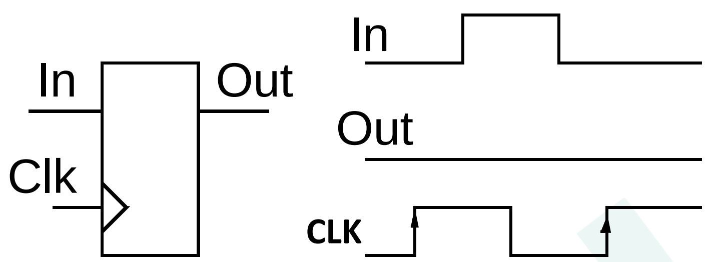
Flip-Flop (edge-triggered, non transparent)

On the *rising* edge of clock (pos-edge trig), it transfers the value of **In** to **Out**

It holds the value at all other times.



Latch

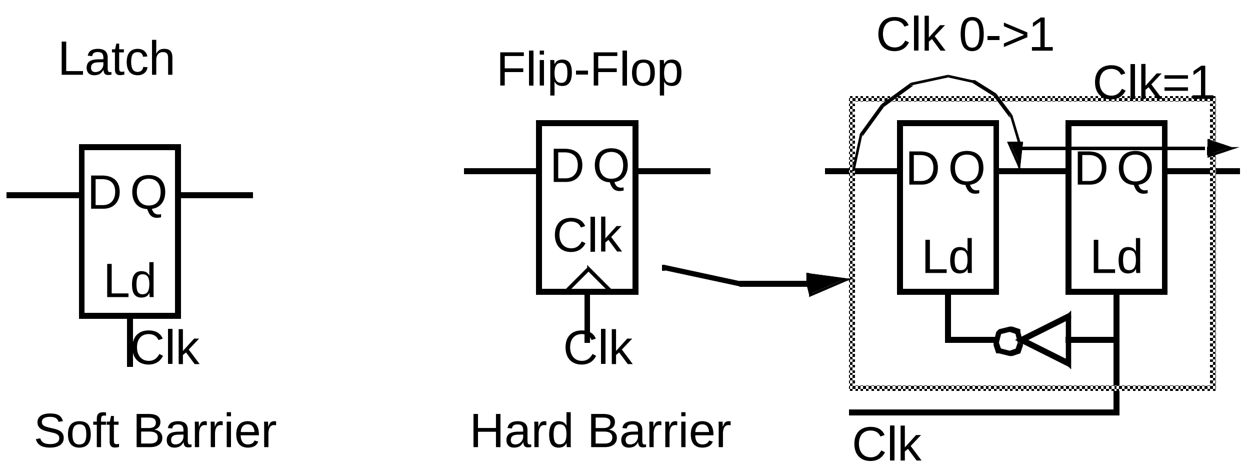


Flip-Flop

Alternative View

Clocks serve to slow down signals that are too fast

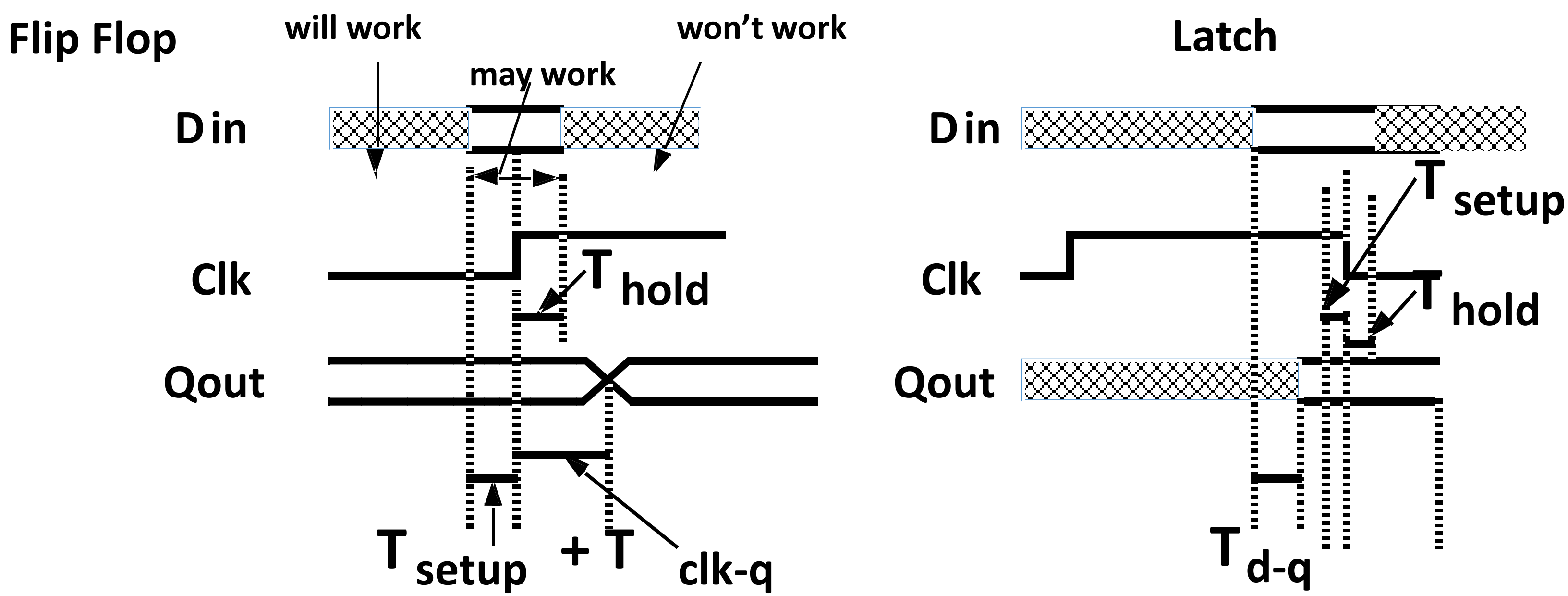
- Flip-flops / latches act as barriers



  - With a latch, a signal can propagate through while the clock is high
  - With a Flip-flop, the signal only propagates through on the rising edge
    Flip-flops consist of two latch like elements (master and slave latch)

Clocking Overhead

FF and Latches have setup and hold times that must be satisfied:



If Din arrives before setup time and is stable after the hold time, FF will work; if Din arrives after hold time, it will fail; in between, it may or may not work; FF delays the slowest signal by the setup + clk-q delay in the worst case

Latch has small setup and hold times; but it delays the late arriving signals by $T_{d\text{-}q}$

Clock Skew

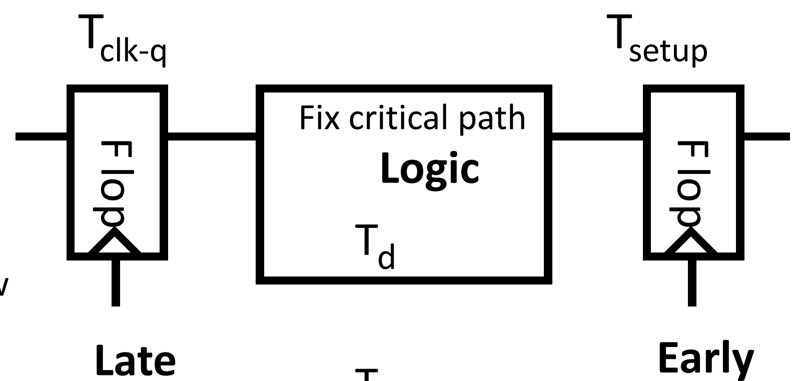
- Not all clocks arrive at the same time, i.e., they may be skewed.
  - SKEW = mismatch in the delays between arrival times of clock edges at FF's

SKEW causes two problems:

- The <u>cycle time gets longer</u> by the skew

  $T_{cycle} = T_d + T_{setup} + T_{clk\text{-}q} + T_{skew}$

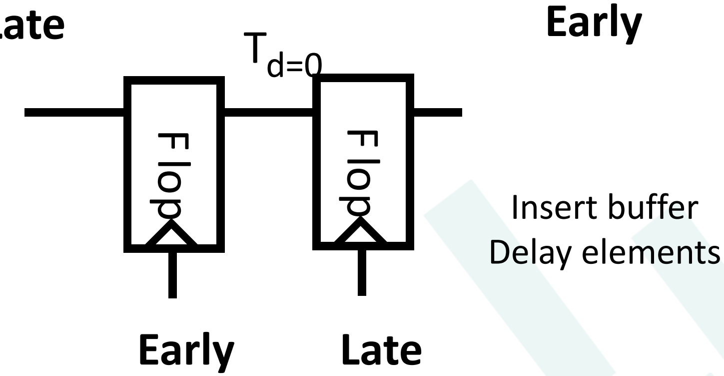
  Shows up as a SETUP time violation



- The part <u>can get the wrong answer</u>

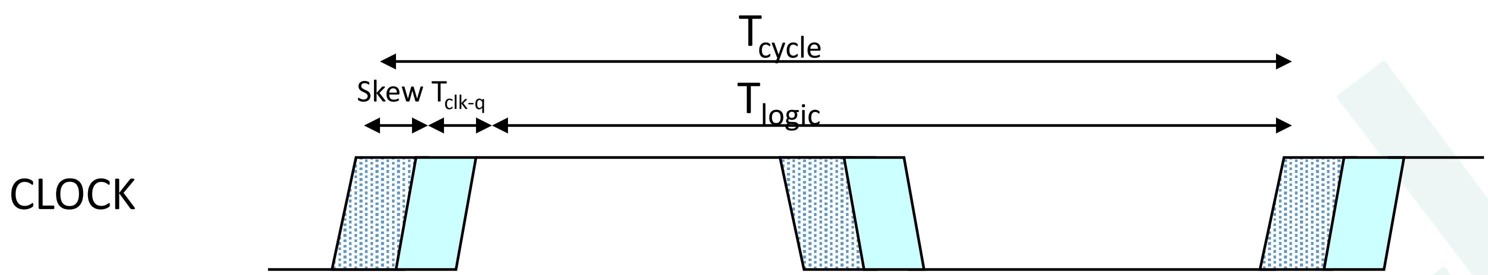
  when $T_{skew} + T_{hold} > T_{clk\text{-}q}$

  Shows up as a HOLD time violation



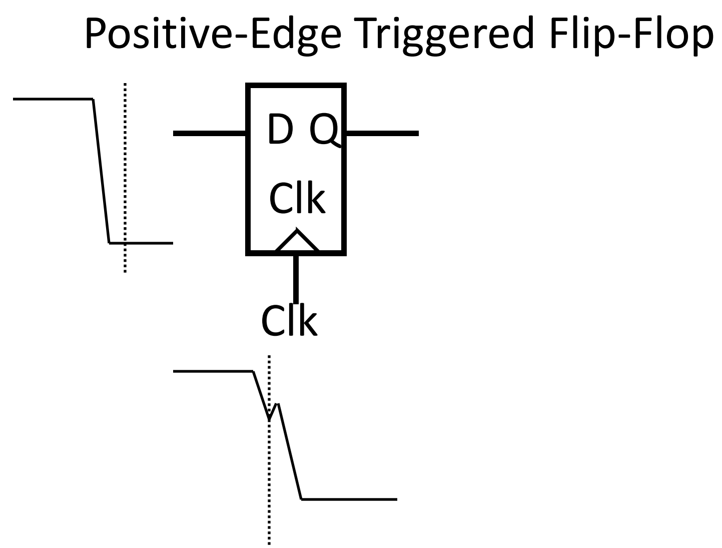
Overhead for a Clock

- CMOS FO4 delay is roughly 425ps/um x L_{eff}
- For 0.13um, FO4 delay $\approx$ 40 - 50ps
  - For a 1GHz clock, this allows < 20 FO4 gate delays/cycle
- Clock overhead (including margins for setup/hold)
  - 2 FF/Latches cost about 2-3 FO4 delays
  - skew costs approximately 2-3 FO4 delays
- Overhead of clock is roughly 4-6 FO4 delays
- 14-16 FO4 delays left to work with for logic
- Need to reduce skew and FF cost



Signal Integrity Issues at FF's

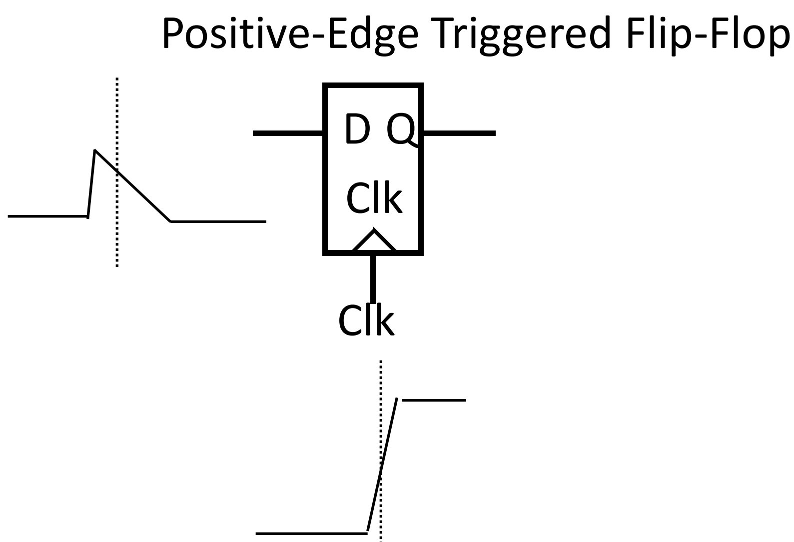
- What happens if a glitch occurs in a clock signal?



- Flip-flop captures and propagates incorrect data
- Could view any signal that, if glitched, could cause a logic upset as a "clock" signal
- Need to space out clocks/signals or shield them

Signal Integrity Issues at FF's

- What happens if a glitch occurs in data signal?



- Flip-flop captures and propagates incorrect data
- Need to insure that data signal is stable during FF setup time
- Shielding with stable signals or spacing is needed

Sources of Clock Skew

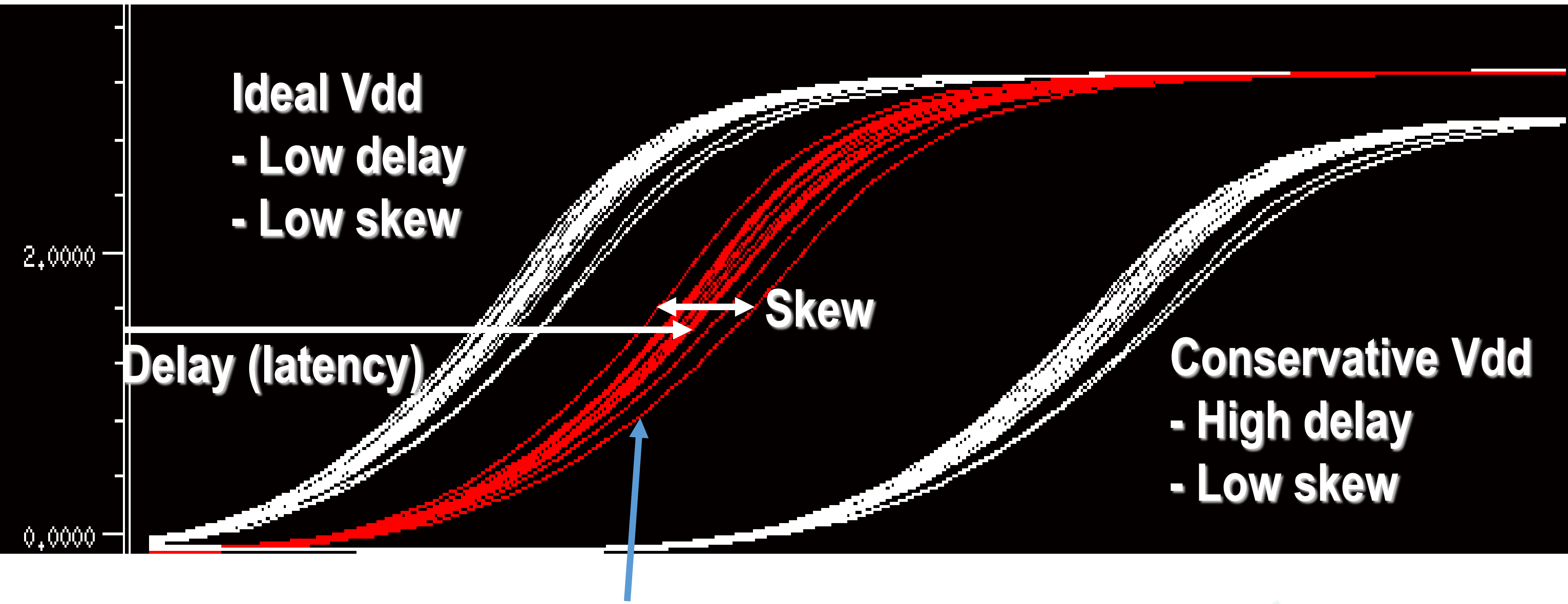
Main sources:

1. Imbalance between different paths from clock source to FF's
   - interconnect length determines RC delays
   - capacitive coupling effects cause delay variations
   - buffer sizing
   - number of loads driven
2. Process variations across die
   - interconnect and devices have different statistical variations

Secondary Sources:

1. IR drop in power supply
2. Ldi/dt drop in supply

IR Drop Impacts on Clock Skew



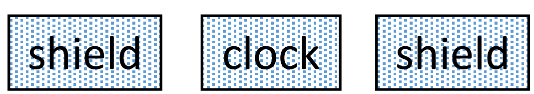
Actual IR drop impact
- delay about 5-15% larger
- skew about 25-30% larger

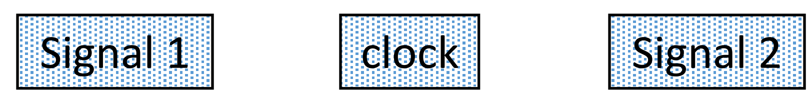
Power dissipation in Clocks

- Significant power dissipation can occur in clocks in high-performance designs:
  - clock switches on every cycle so $P = CV^2f$ (i.e., $\alpha=1$)
  - clock capacitance can be ~nF range, say 1nF = 1000pF
  - assuming a power supply of 1.8V, CV = 1800pC of charge
  - if clock switches every 2ns (500MHz), that's 0.9A
  - for V_{DD} = 1.8V, P=IV=0.9(1.8)=1.6W in the clock circuit alone
- Much of the power (and the skew) occurs in the final drivers due to the sizing up of buffers to drive the flip-flops
- Key to reducing the power is to examine equation CV^2f and reduce the terms wherever possible
  - V_{DD} is usually given to us; would not want to reduce swing due to coupling noise, etc.
  - Look more closely at C and f

Reducing Power in Clocking

- Gated Clocks:
  - can gate clock signals through AND gate before applying to flip-flop; this is more of a total chip power savings
  - all clock trees should have the same type of gating whether they are used or not, and at the same level - total balance
- Reduce overall capacitance (again, shielding vs. spacing)





(a) higher total cap./less area (b) lower cap./ more area

  - Tradeoff between the two approaches due to coupling noise
  - approach (a) is better for inductive noise; (b) is better for capacitive noise

Clock Design Objectives

- Now that we understand the role of the clock and some of the key issues, how do we design it?
  - Minimize the clock skew (in presence of IR drop)
  - Minimize the clock delay (latency)
  - Minimize the clock power (and area)
  - Maximize noise immunity (due to coupling effects)
  - Maximize the clock reliability (signal EM)
- Problems that we will have to deal with
  - Routing the clock to all flip-flops on the chip
  - Driving unbalanced loading, which will not be known until the chip is nearly completed
  - On-chip process/temperature variations

Quiz II

1. Write the expression for the total capacitance for the middle wire when the wires are:
   a) closely spaced and
   b) widely spaced.

2. Find out the target impedance of the power grid for a supply voltage of Vdd=1.2V and supply current of Idd=100 A with 10% fractional noise budget.