ECE 715
System on Chip Design and Test

Lecture 16

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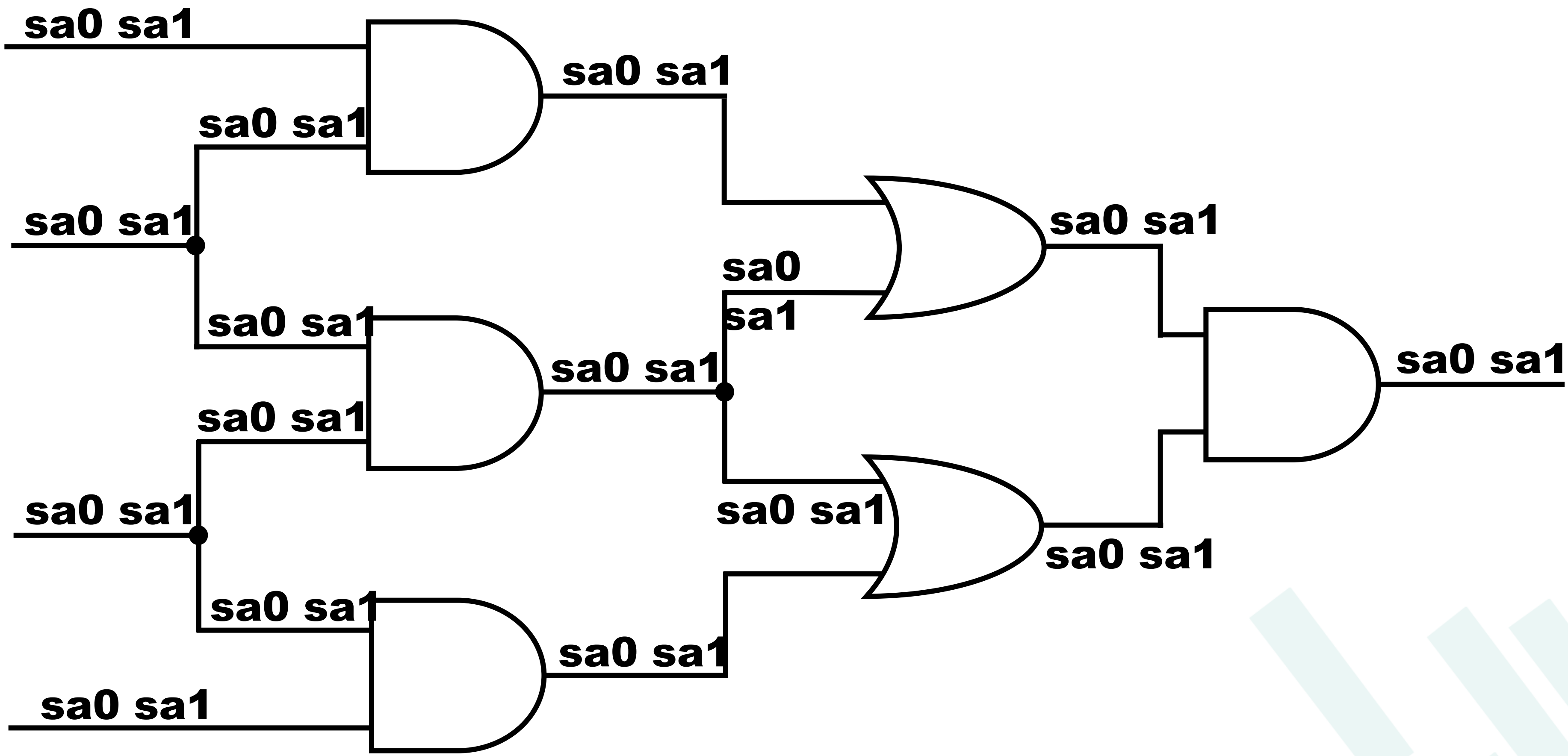
INFORMATION TECHNOLOGY
DELHI

Mid Sem Performance & Discussion

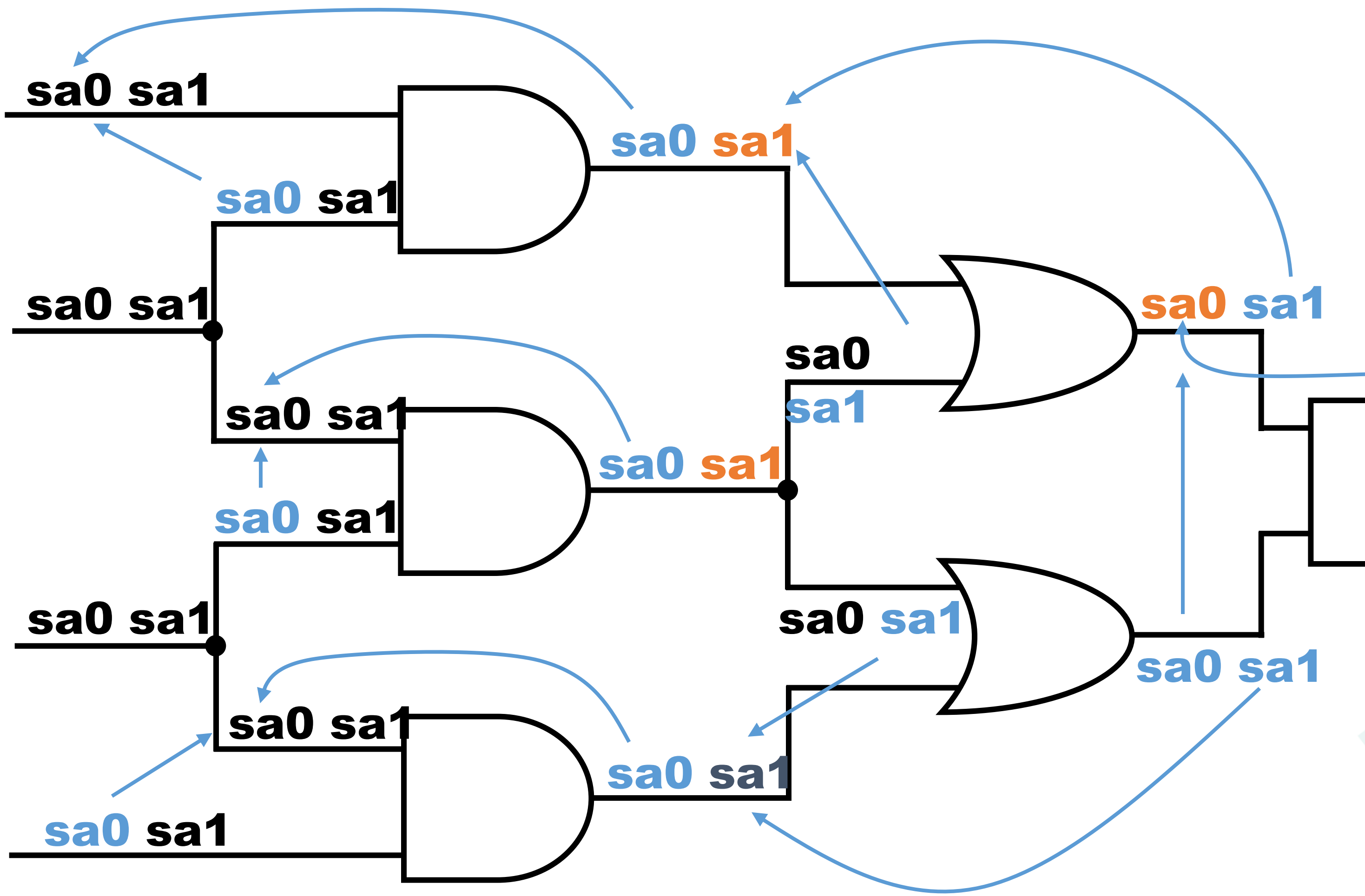
- Highest: 16.5
- Lowest: 6.5
- Average: 12.7

- Discussion

Dominance Example



Dominance Example



Faults in blue removed by equivalence collapsing

Faults in green removed by dominance collapsing

$$\text{Collapse ratio} = \frac{15}{32} = 0.47$$

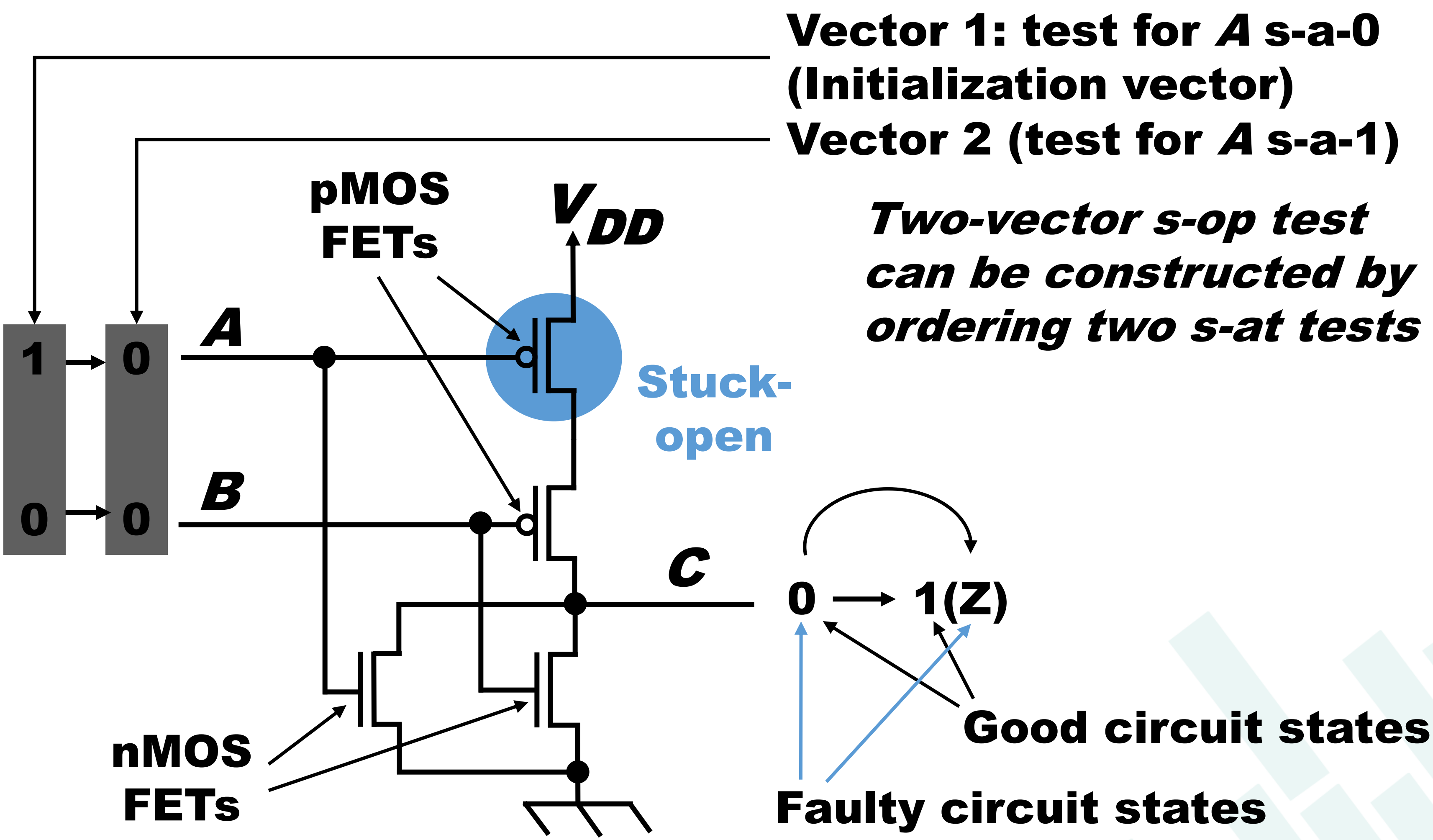
Multiple Stuck-at Faults

- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with k single fault sites is 3^k-1.
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.

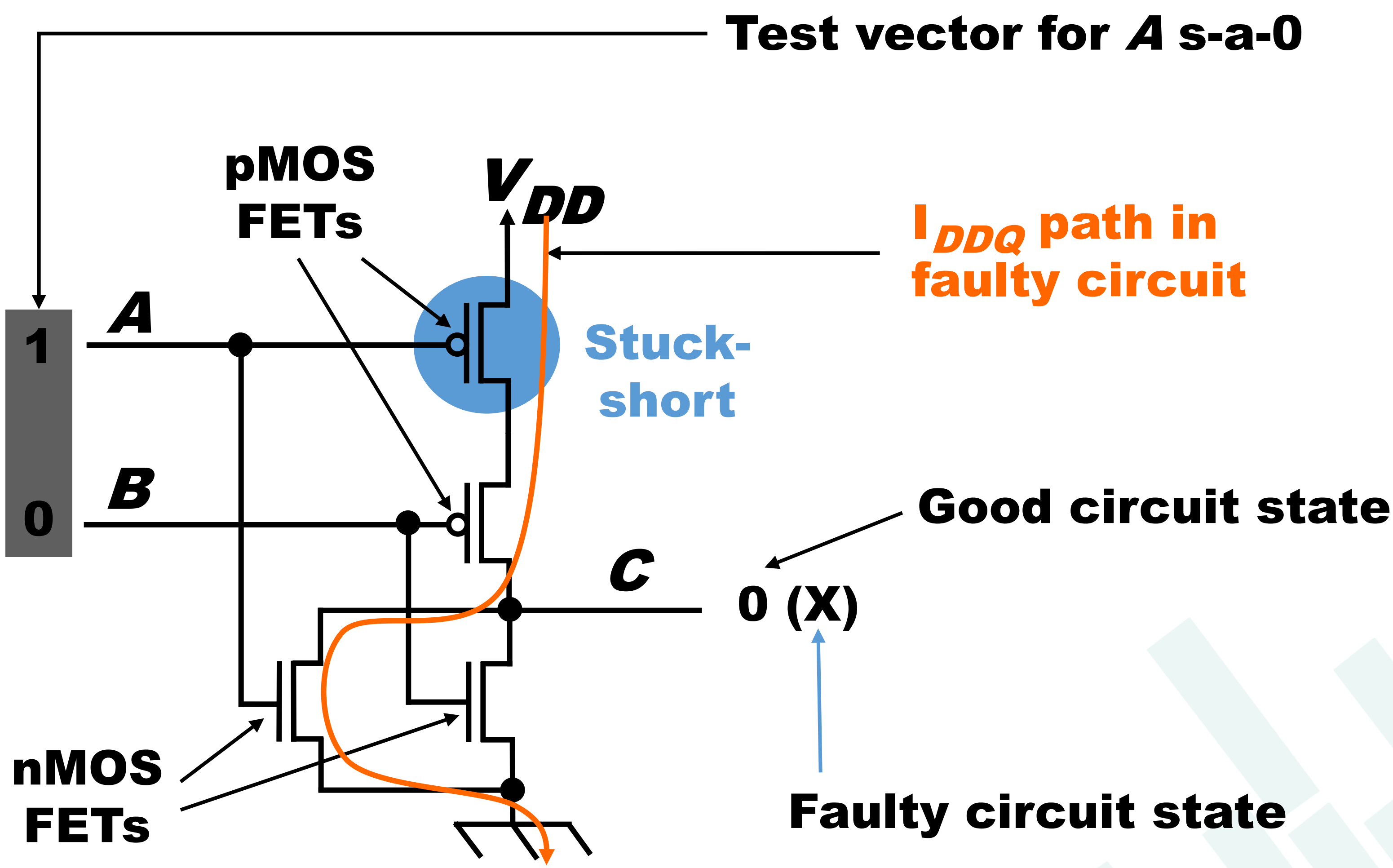
Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - Stuck-open -- a single transistor is permanently stuck in the open state.
  - Stuck-short -- a single transistor is permanently shorted irrespective of its gate voltage.
- Detection of a stuck-open fault requires two vectors.
- Detection of a stuck-short fault requires the measurement of quiescent current (I_{DDQ}).

Stuck-Open Example



Stuck-Short Example



I_{DDQ} Current Testing

Lecture 17

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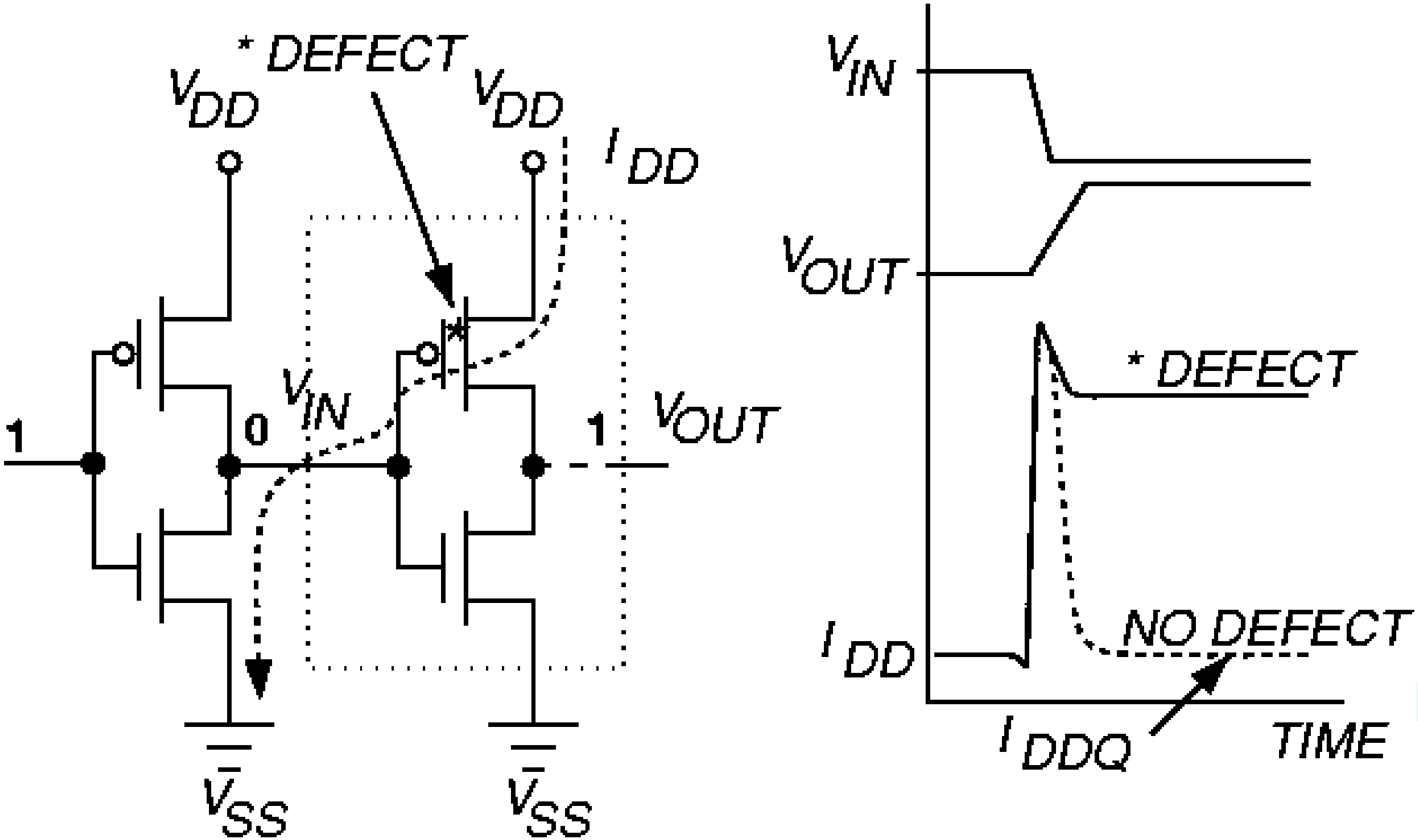
Basic Principle of I_{DDQ} Testing



- Measure I_{DDQ} current through V_{ss} bus

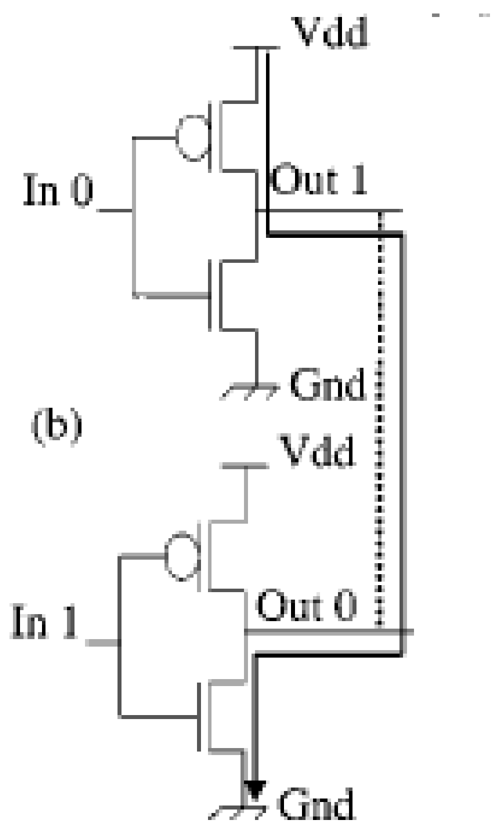
Basic Principles

- IDDQ testing refers to the integrated circuit (IC) testing method based upon measurement of steady state power-supply current.
- Iddq stands for quiescent Idd, or quiescent power-supply current.
- In case of a defect such as gate-oxide short or short between two metal lines, a conduction path from power-supply (Vdd) to ground (Gnd) is formed and subsequently the circuit dissipates significantly high current.
- This faulty current is a few orders of magnitude higher than the fault-free leakage current.
- Iddq testing provides physical defect oriented testing

Physical Defects

- Wafer defects are found in clusters. These clusters are randomly distributed over the whole wafer. Every part of the wafer has an equal probability of having a defect cluster.
- Any part of a diffusion, Polysilicon, or metal line may have an open fault. Any contact between any two layers may be open.
- Bridging may occur between any two electrical nodes, whether they belong to one layer or different layers
- Only a small percentage of bridging and open faults can be modeled at the stuck-at level. The actual distribution varies and largely depends on the technology and fabrication process.

Bridging

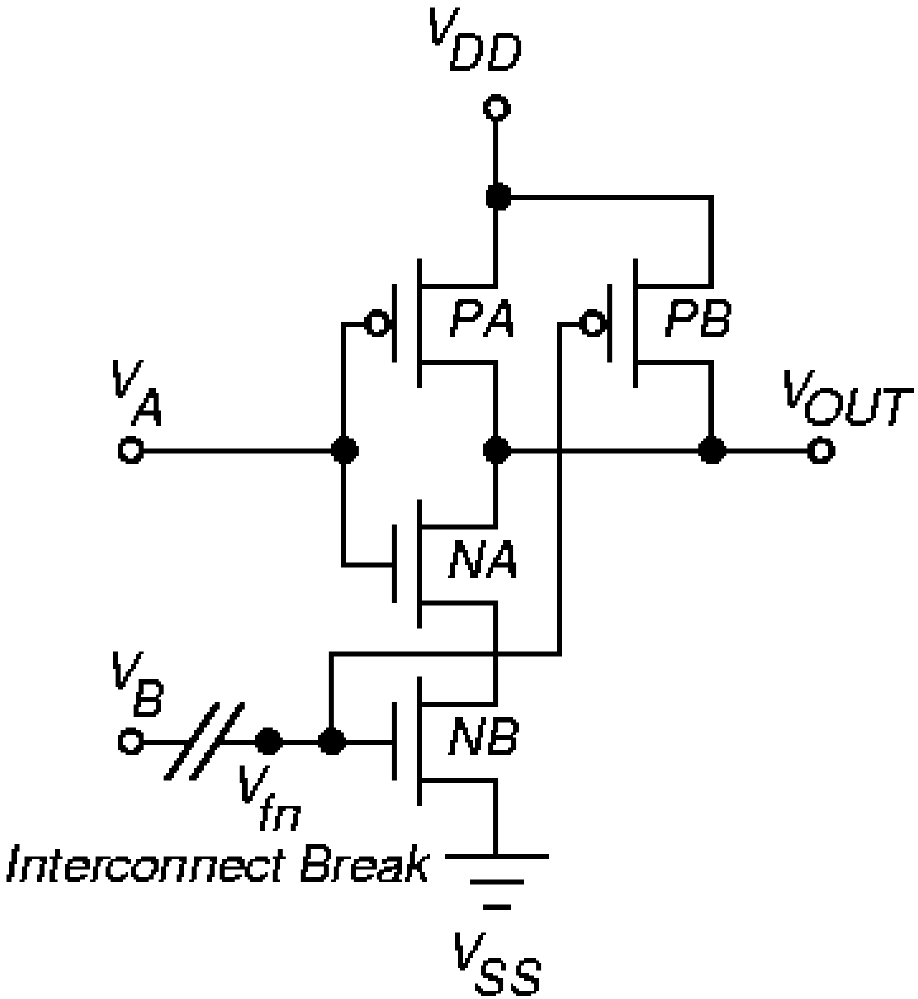


in the presence of bridging, a conduction path is formed from Vdd to Gnd.
Subsequently, the circuit dissipates a large current through this path, and thus, simple monitoring of the supply current can detect bridging.

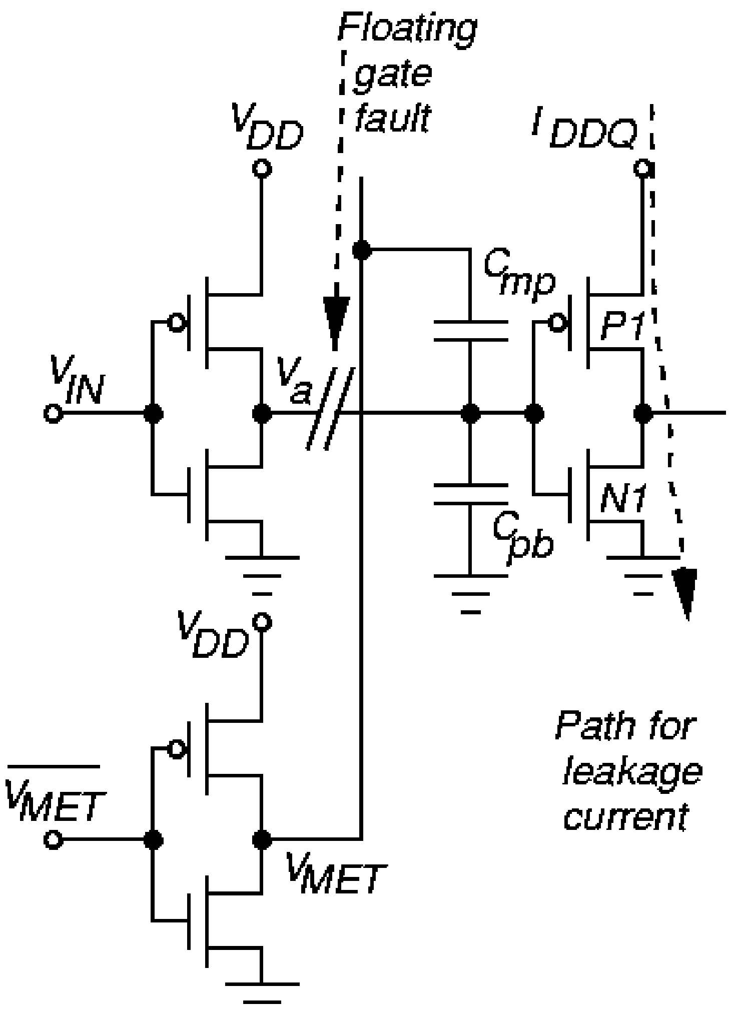
Floating Gate Defects

- Small break in logic gate inputs (100 – 200 Angstroms) lets wires couple by electron tunneling
  - Delay fault and I_{DDQ} fault
- Large open results in stuck-at fault – not detectable by I_{DDQ} test
  - If $V_{tn} < V_{fn} < V_{DD} - | V_{tp} |$ then detectable by I_{DDQ} test

NAND Open Circuit Defect – Floating gate



Capacitive Coupling of Floating Gates



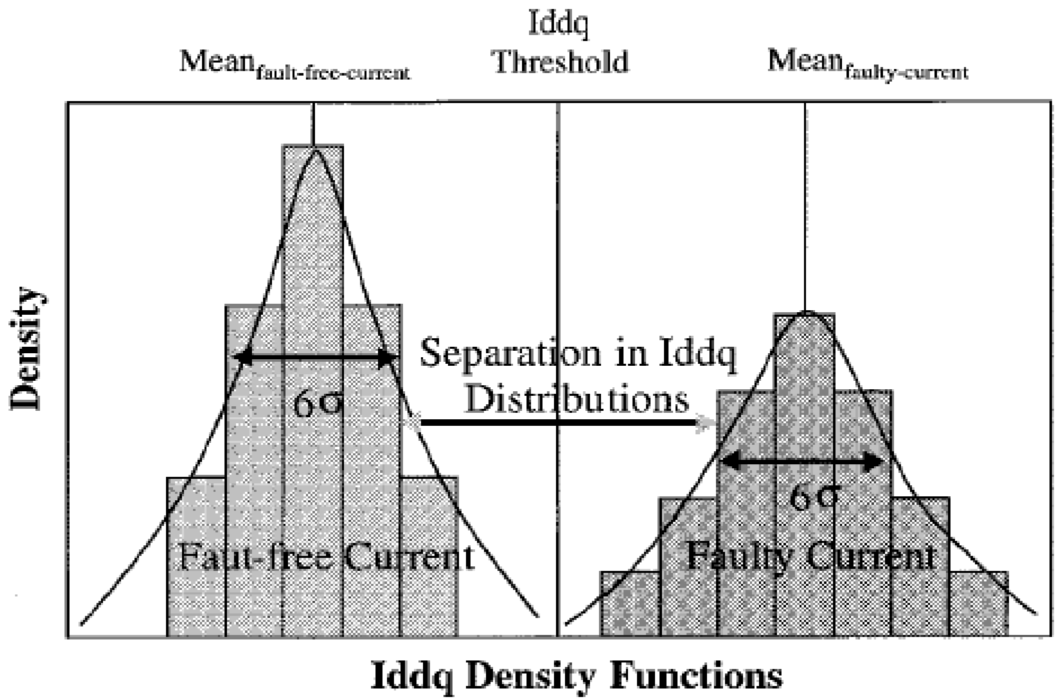
- C_{pb} – capacitance from poly to bulk
- C_{mp} – overlapped metal wire to poly
- Floating gate voltage depends on capacitances and node voltages
- If *n*FET and *p*FET get enough gate voltage to turn them on, then I_{DDQ} test detects this defect
- K is the transistor gain

Iddq Testing in SoCs

- SoCs contain huge number of transistors
- Summation of leakage current of all transistors becomes too large to distinguish between faulty and fault-free chips
- Most of the SoCs contain multiple power supplies
- Iddq testing is done on one power supply at a time

Iddq Testing in DSM

- The theoretical basis of Iddq testing is based upon estimation of defect-free current in the circuit and then setting a limit (popularly, called as Iddq threshold) above which a circuit is considered defective.



Iddq Testing in DSM

- When the density functions of defect-free and defective current are separate from each other, the clear distinction between the good and the defective IC can be made.
- However, with technology shrink (increased sub-threshold leakage) and increasing number of gates in an IC, the mean value of the distribution of defect-free current increases and approaches the Iddq threshold limit (set from earlier technology).
- Just changing the threshold limit to a higher number does not resolve the issue because with high leakage in the circuit, change in defect-free and defective current is very small

Iddq Testing in DSM

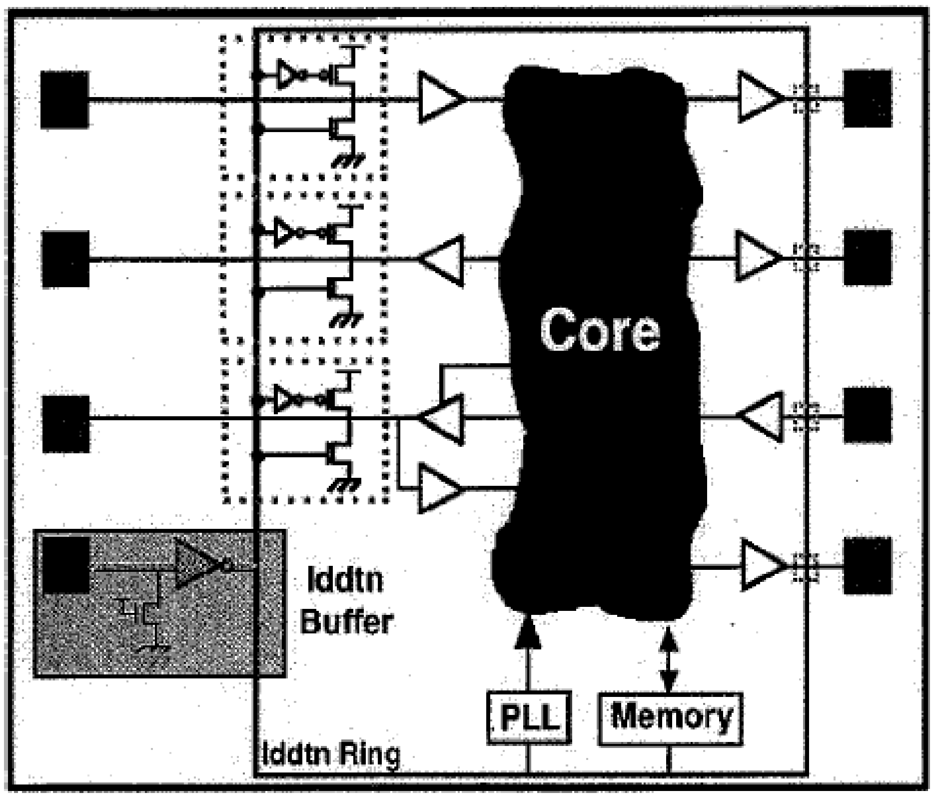
Technology (µm)	Vdd (V)	T_{ox} (Å)	V_t (V)	I_{off} (pA/µm)	
				NMOS	pMOS
0.8	5	150-100	0.8-0.7	0.01 – 0.05	0.005 – 0.02
0.6	5 – 3.3	100-80	0.75-0.65	0.05 – 0.5	0.01 - 0.2
0.5	5 – 2.5	90-70	0.7-0.6	0.1 - 2	0.1 – 1
0.35	3.3 – 2.5	80-60	0.65-0.55	0.5 - 10	0.1 - 10
0.25	3.3 – 1.8	70-50	0.6-0.5	6 - 60	0.5 - 24
0.18	2.5 – 1.8	55-35	0.55-0.45	40 - 600	20 -300

Two mechanisms have been proposed to reduce I_{off}:
reduced temperature and substrate bias.

Design-for-Iddq-Testing

- Avoid any possible static high current state in the circuit; if a high current state is unavoidable, then re-design so that it can be isolated during Iddq testing.
- All static current dissipating logic should be switched off, this includes memory sense-amps, dynamic logic, asynchronous logic, pull-up/pull-down resistors, special I/O buffers and analog circuitry.

Design-for-Iddq-Testing



Global control signal to switch off static current dissipating logic

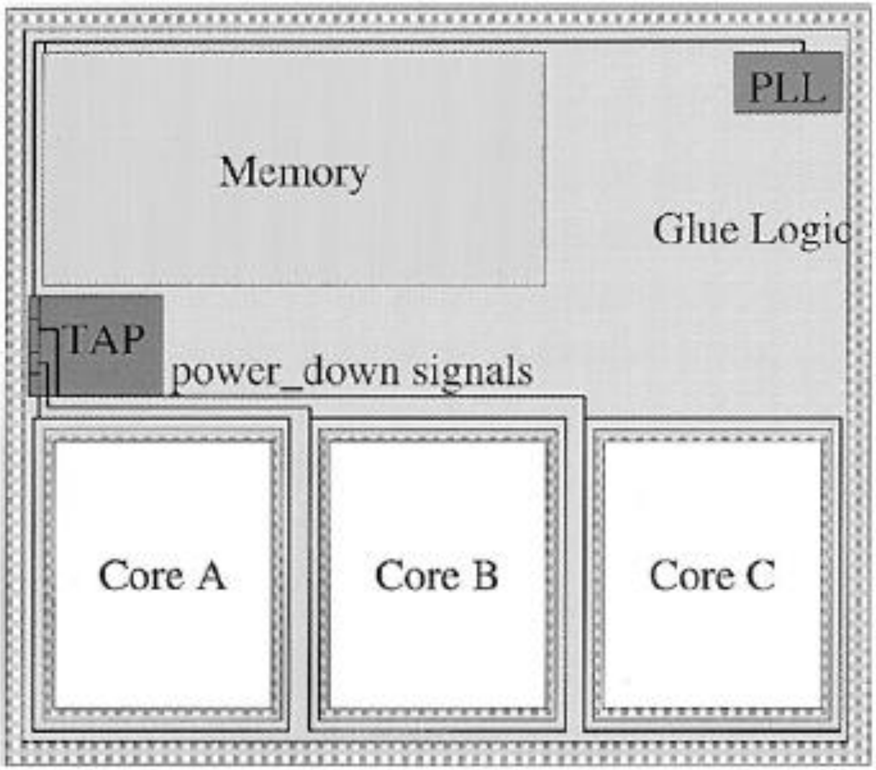
Iddq Testing in SoC

- The global power-down control signal based design methodologies are also very important for system-on-a-chip (SoC) designs using embedded cores.
- In SoCs we need one power supply control signal per core
- One pin per core is needed
- Extra overhead

Iddq Testing in SoC

- Some type of partitioning method is needed for Iddq testing in embedded core-based system chips
- Power_Down control signals are used to selectively switch off portions of the SoC

Iddq Testing in SoC



Quiz IV

- Find the test vectors for detecting single stuck-at faults in the circuits below: