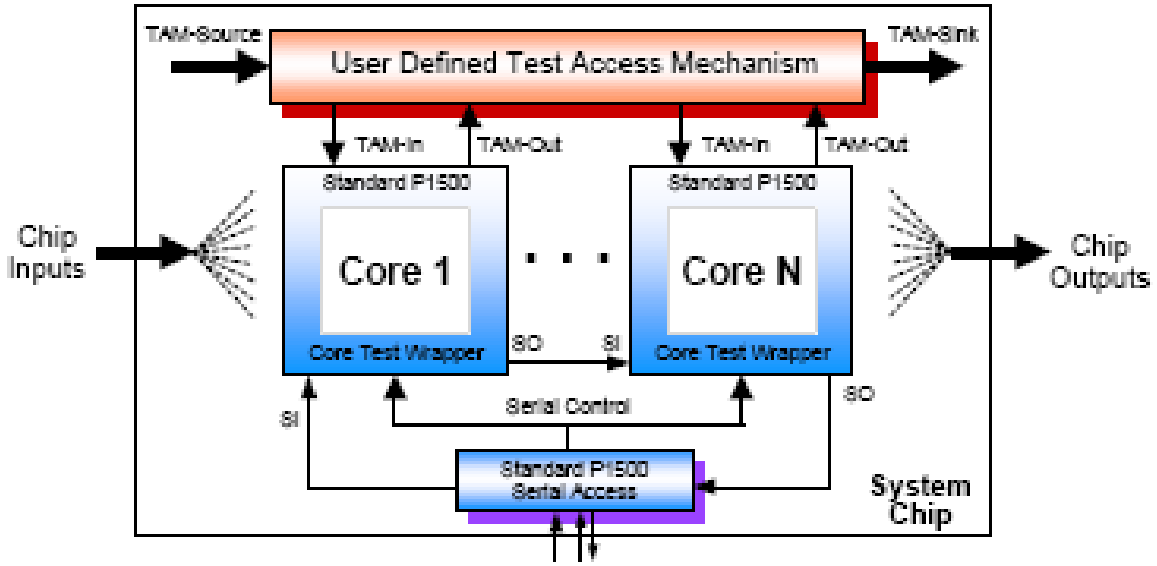
ECE 715
System on Chip Design and Test

Lecture 19

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Wrapper Standardization - P1500



- TAM Source/Sink
  - From chip I/O and from test bus, test rail, BIST, etc.
- TAM In/Out
  - 0 to n lines for parallel and/or serial test data, or test control
- Standard P1500 Serial Access & Control
  - From chip-level TAP controller, chip I/O, etc.

P1500 Core Test Requirements
Test Functions at Core Terminals

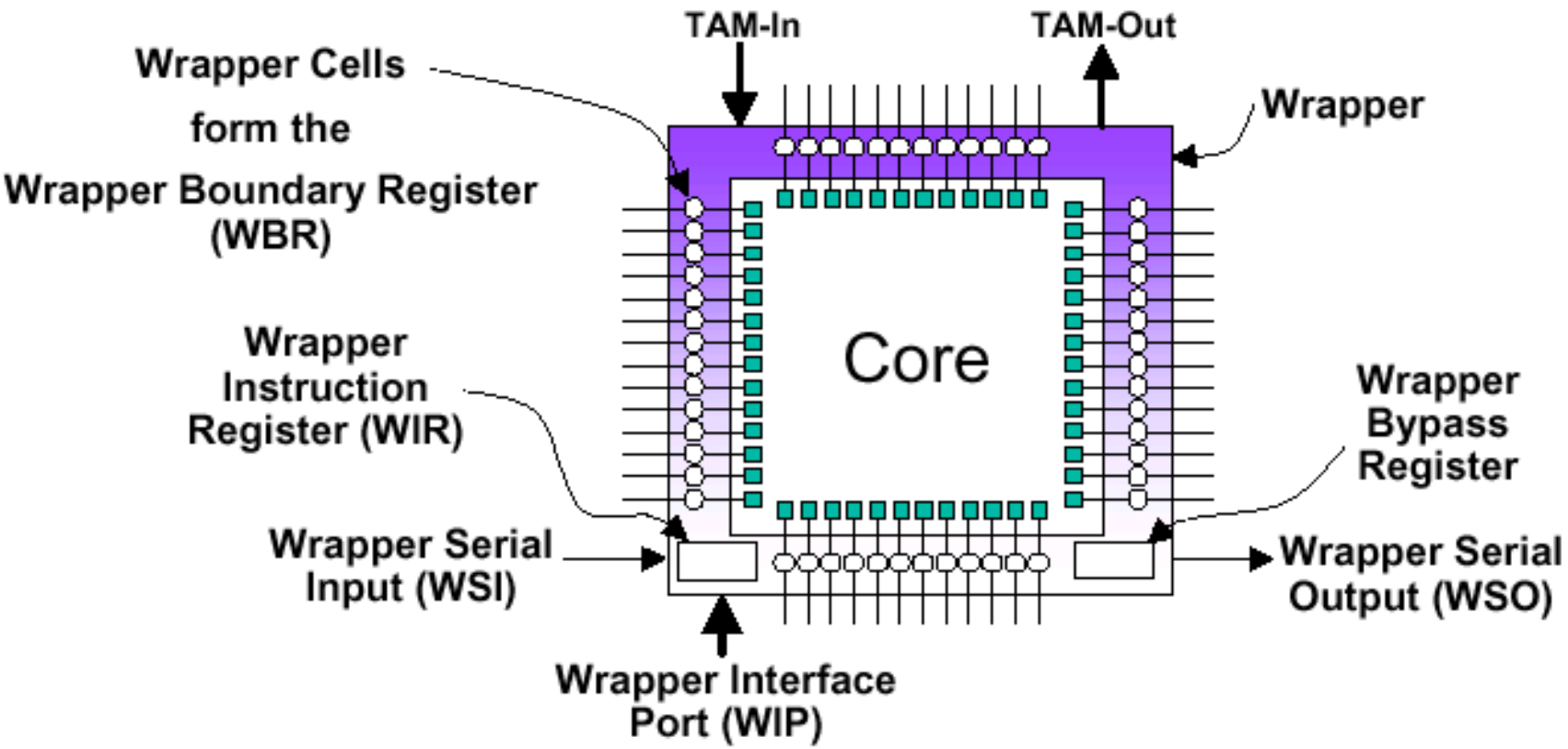
Input Test Functions

- **Input Observation:** Allows logic values applied to core input terminals, from logic external to the core, to be observed.
- **Input Control:** Allows test data to be applied to core input terminals, such that it can be propagated into the core internal logic.
- **Input Constraint:** Forcing, or constraining, core input terminals to fixed logic values – to prevent damage to the core, reducing power consumption, etc.

Output Test Functions

- **Output Observation:** Observation of logic values that have propagated to core outputs terminals from the core's internal logic.
- **Output Control:** Allows test data to be applied at core output terminals, such that it can be propagated to logic external to the core.
- **Output Constraint:** Constraining appropriate non-three-state core output terminals to fixed logic values – to prevent damage to logic external to the core, etc.
- **Output Disable:** Allows forcing three-state core outputs to their inactive state – to prevent damage to other three-state drivers on the same bus.

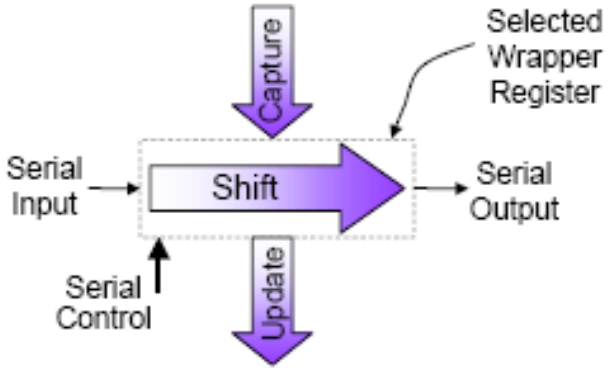
Wrapper Standardization - P1500(cont'd.)



P1500 Wrapper Instruction Register
Proposed Required Instructions

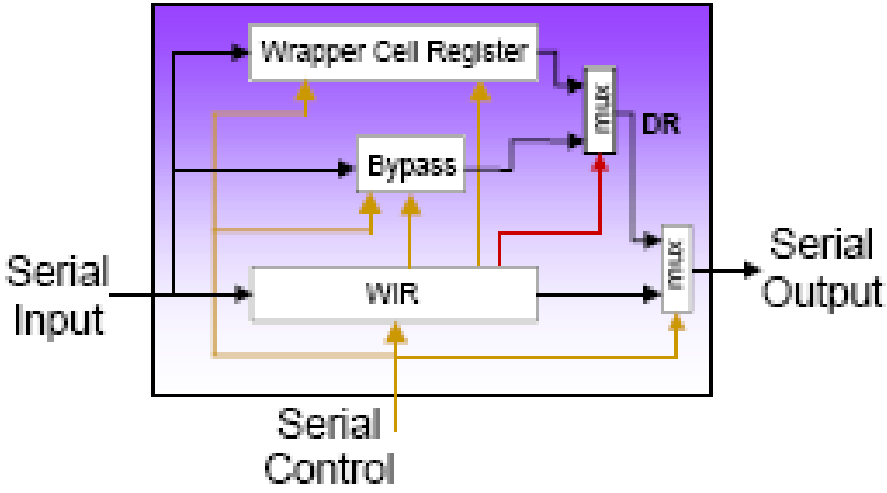
- Normal
  - Wrapper cells allow normal core inputs/outputs to pass through the wrapper for normal system operation
- Core Test
  - Wrapper cells are configured to disable the core's normal mode & connected to TAM and/or wrapper serial input/output for core test
  - Sources & sinks, and core test methods are user defined
- Serial External Test
  - Wrapper cells are configured to disable the core's normal mode, and are connected serially between the wrapper serial input/output
- Isolation
  - Wrapper cells are configured to disable the core's normal mode, and enable setting of appropriate core inputs or outputs to constrained and/or disabled values for core isolation

Scan Protocol Behavior of Wrapper Registers



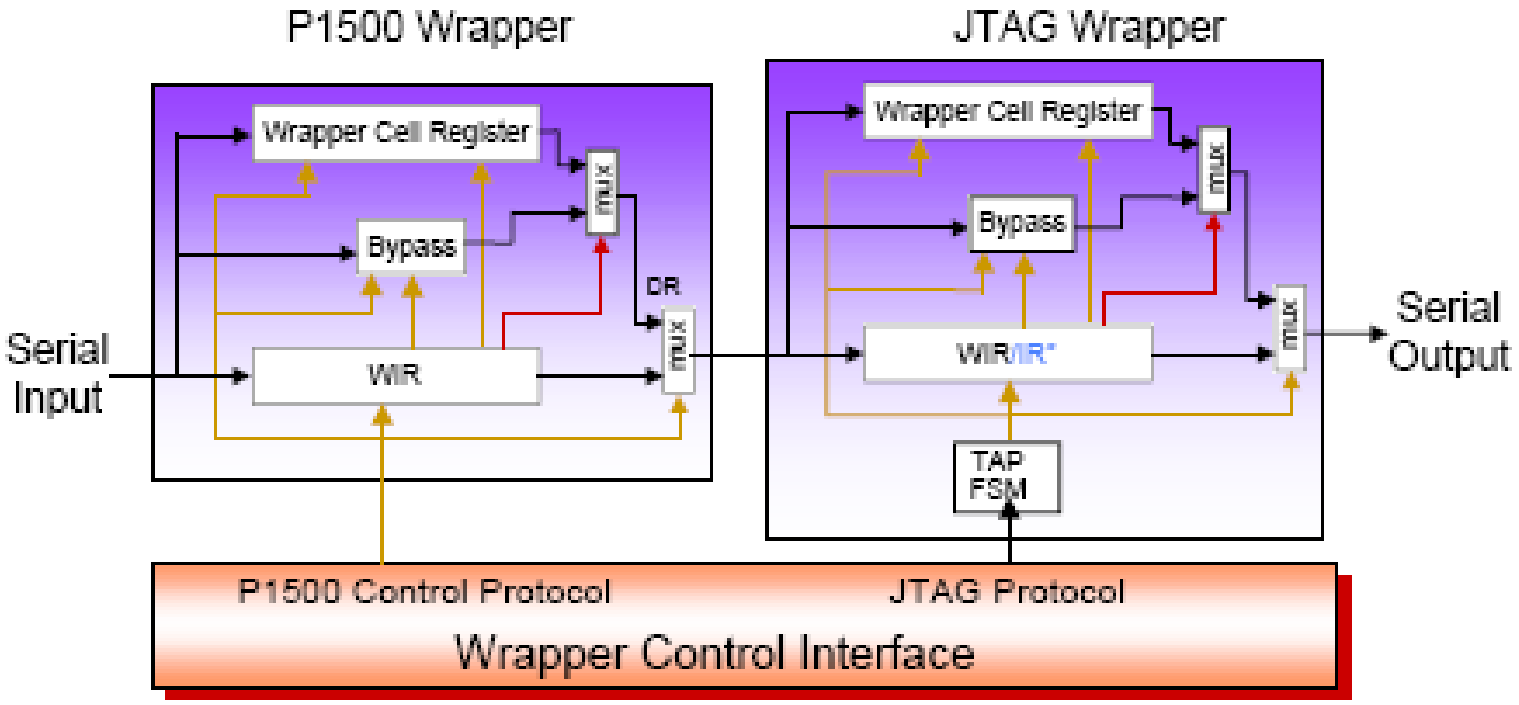
- **Standard P1500 protocol for Wrapper Registers will provide for:**
  - **Parallel capture of input data into the selected register**
  - **Serial shift of the register from serial input to serial output**
  - **Update scan-in data of register to a parallel update stage**

P1500 Wrapper Registers
Standard Serial Scan Path Configuration



- Serial Control lines enable & perform scan, and select between:
  - Wrapper Instruction Register (WIR)
  - Or other Data Registers (DRs), e.g. Wrapper Cell Register, Bypass, etc.
- Updated WIR then selects between DRs

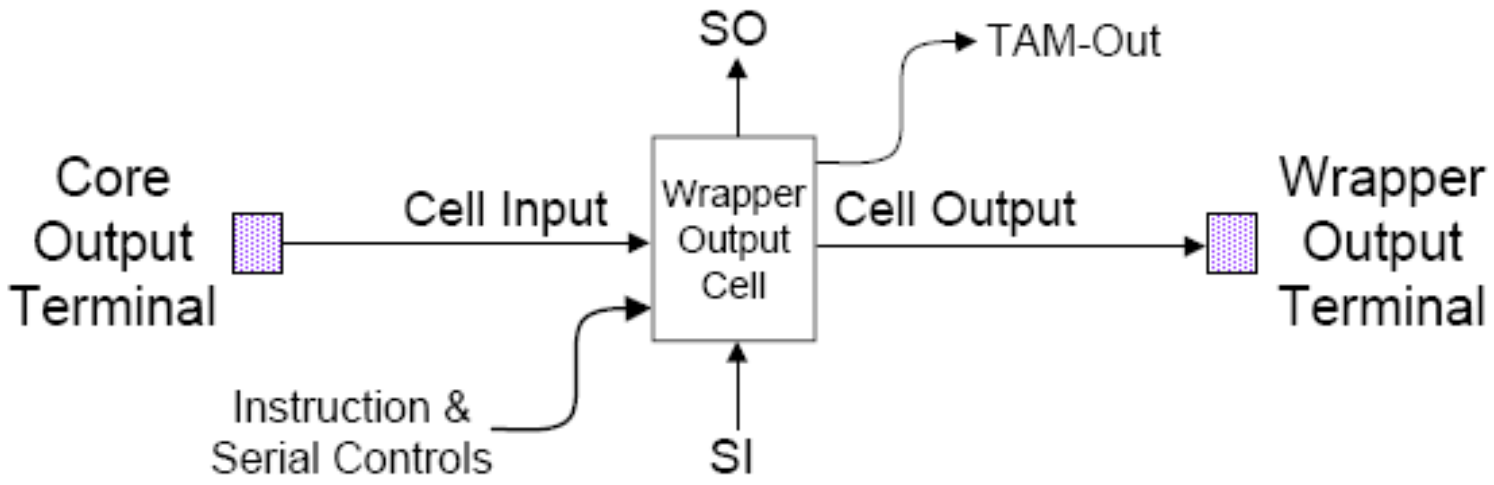
P1500 Wrapper Connection



- **Wrapper Control Interface is configured by system chip integrator**
- **P1500 & JTAG inter-operate at wrapper & serial data interfaces**

P1500 Wrapper Cell Example

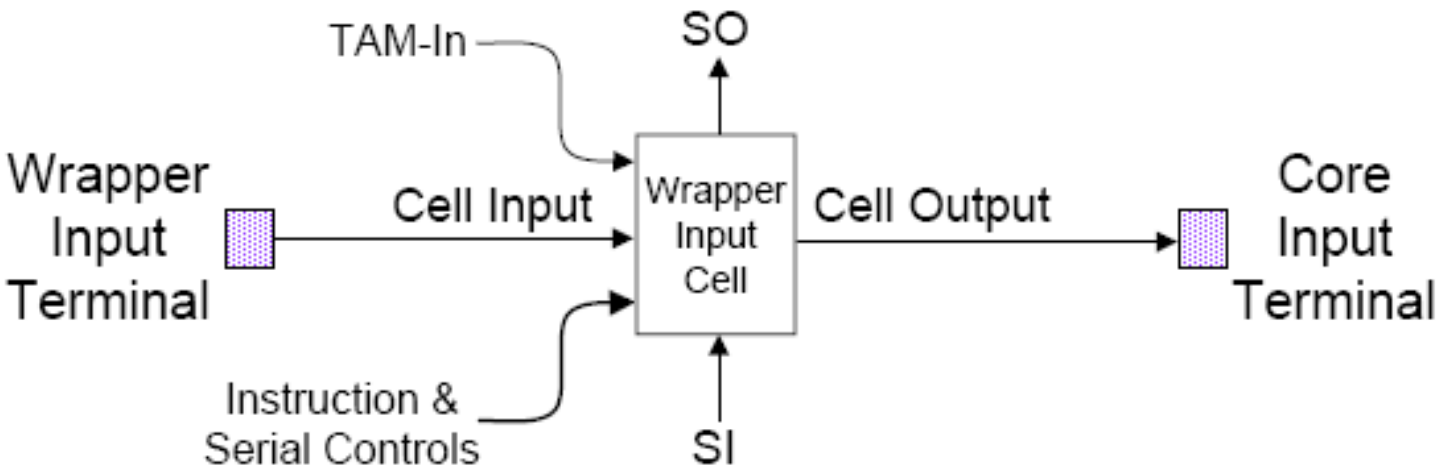
Dedicated Output Cell with Update Stage & TAM-Out



- **Cell behavior for Wrapper Scan Protocol**
  - **Captures data at cell input**
  - **Shifts data from scan input (SI) to scan output (SO)**
  - **Updates shift stage data to update stage**

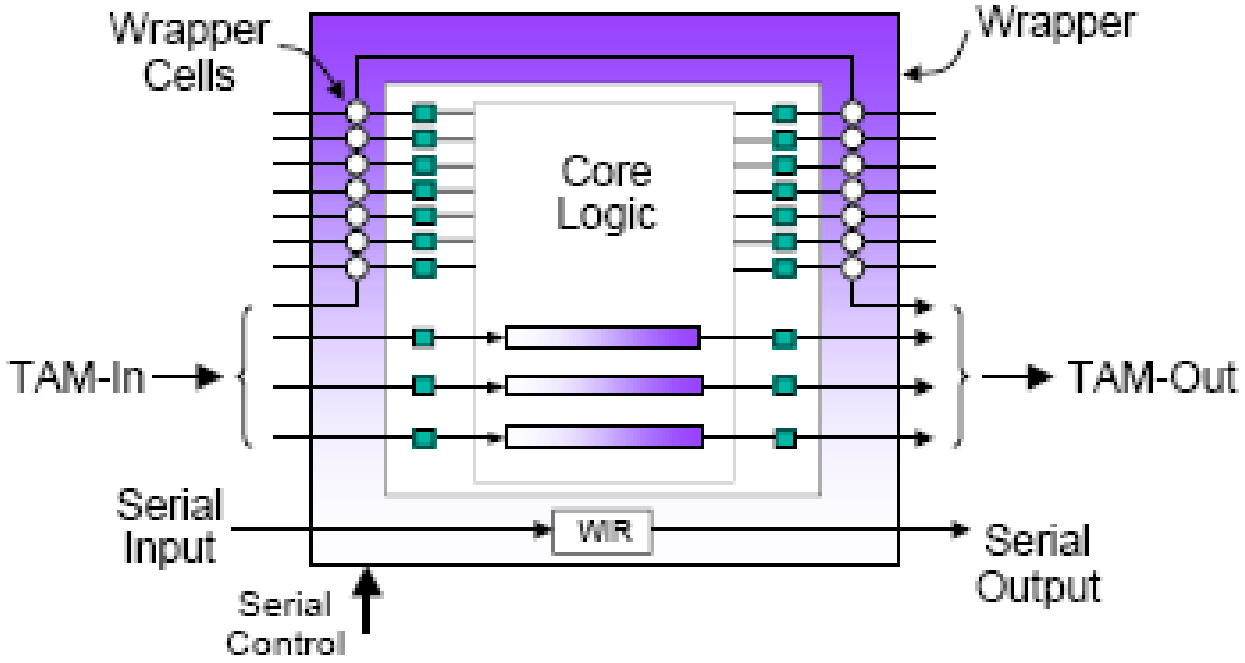
P1500 Wrapper Cell Example

Dedicated Input Cell with Update Stage & TAM-In



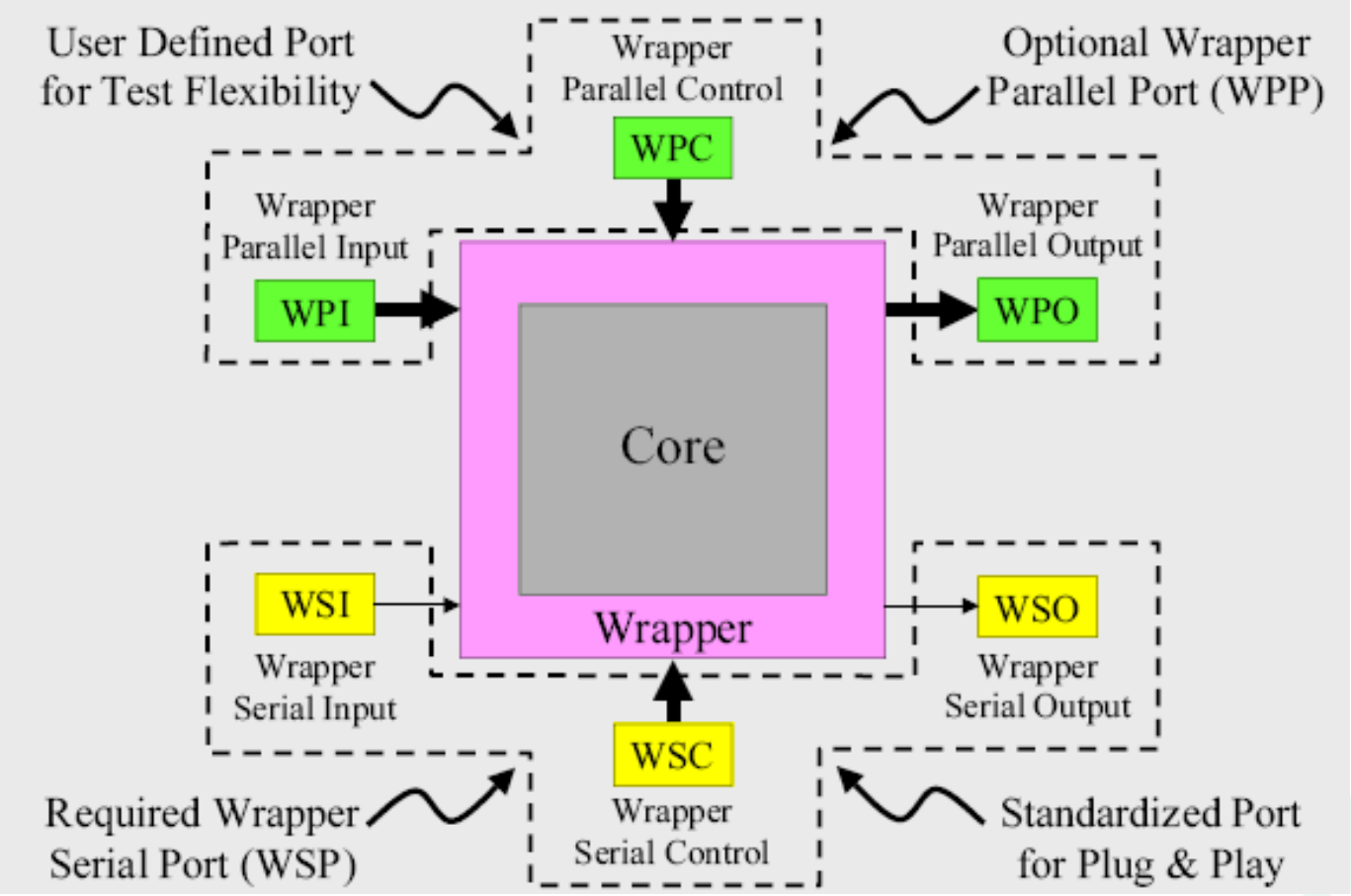
- **Cell behavior for Wrapper Scan Protocol**
  - **Captures data at cell input**
  - **Shifts data from scan input (SI) to scan output (SO)**
  - **Updates shift stage data to update stage**

P1500 TAM Connection Example- Core with Parallel Internal Scan

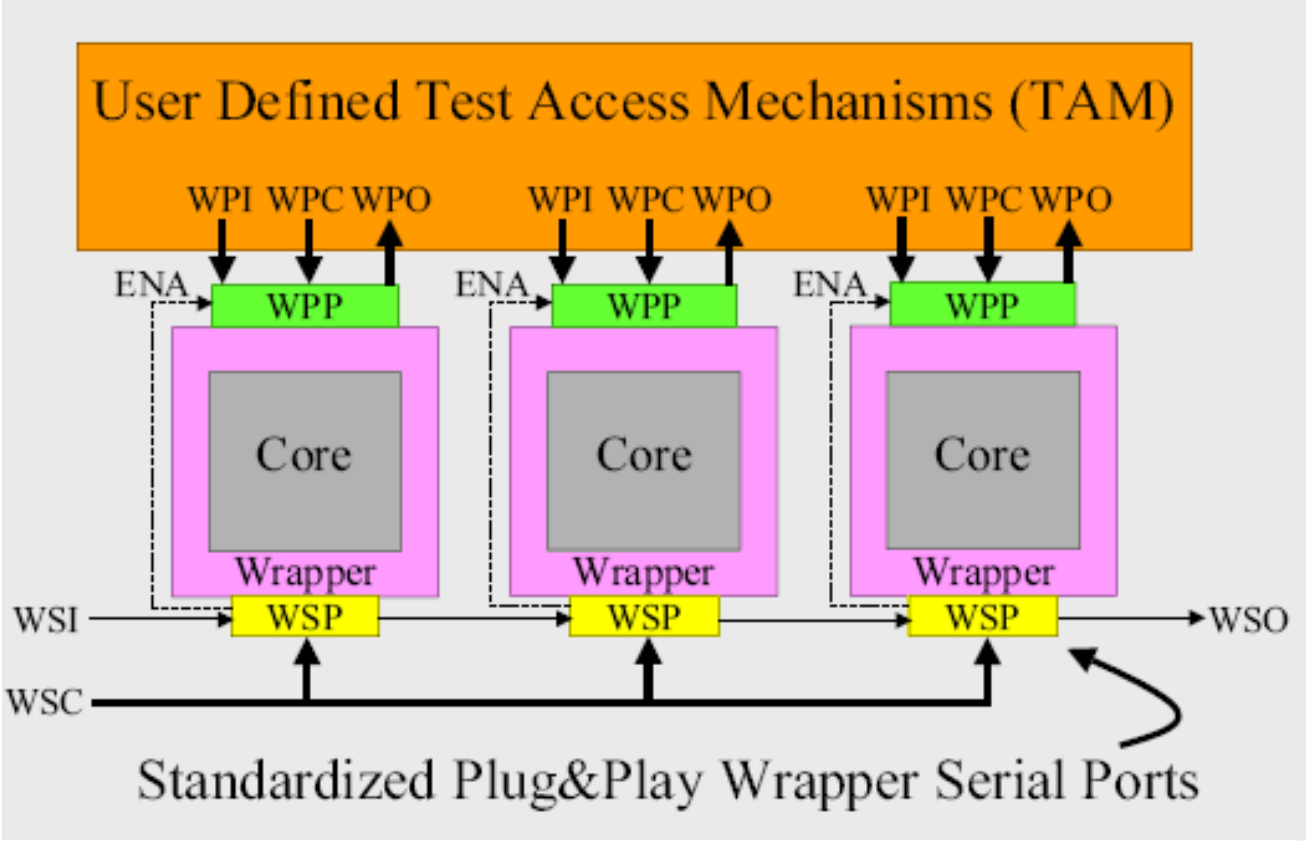


- **Core internal scan path & Wrapper Cell Register are connected in parallel to TAM by a Core Test instruction**
- **Many other TAM connections and configurations are possible!**

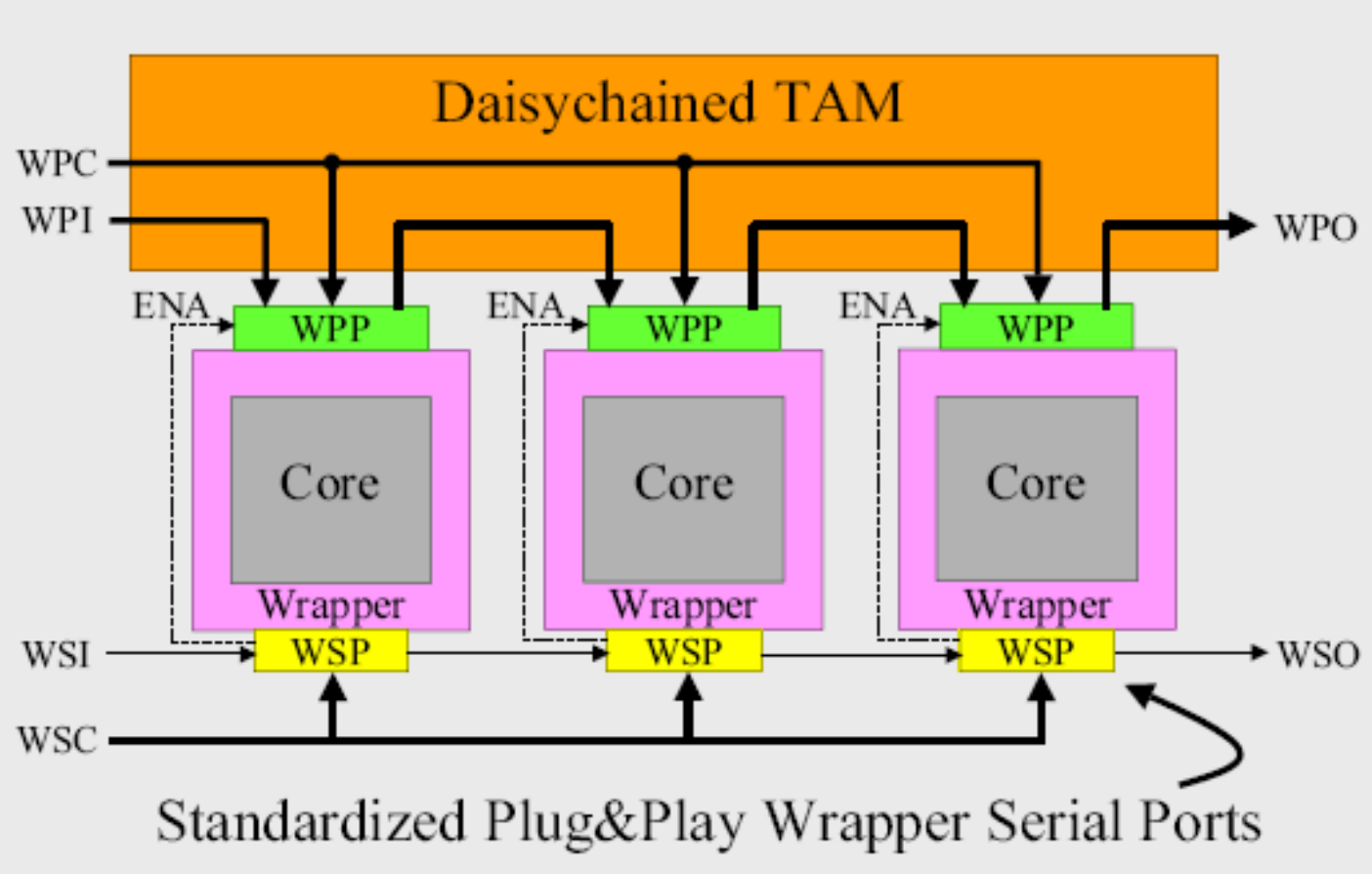
Block level overview of P1500 wrapper



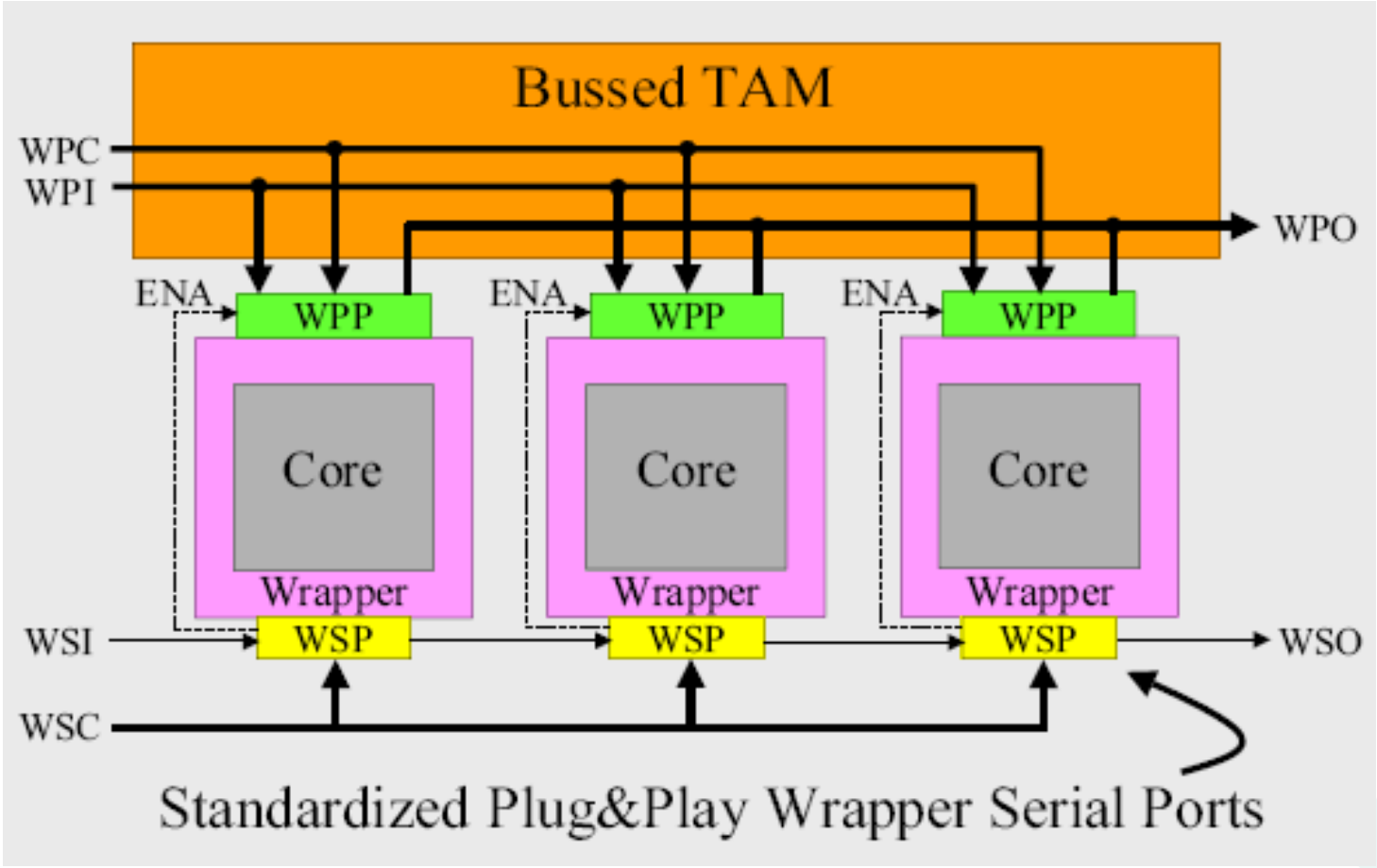
P1500 wrapper configurations



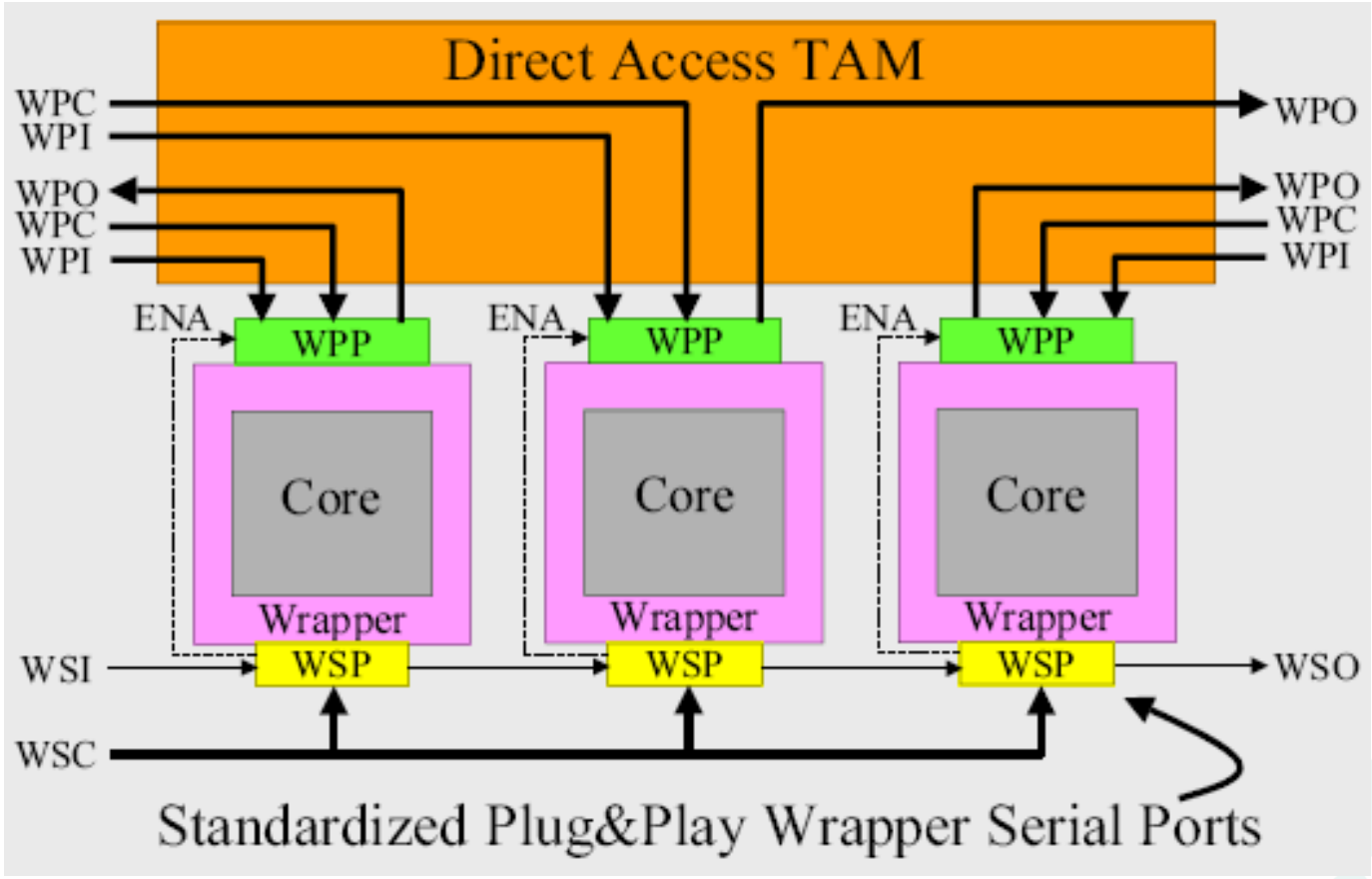
P1500 wrapper configurations



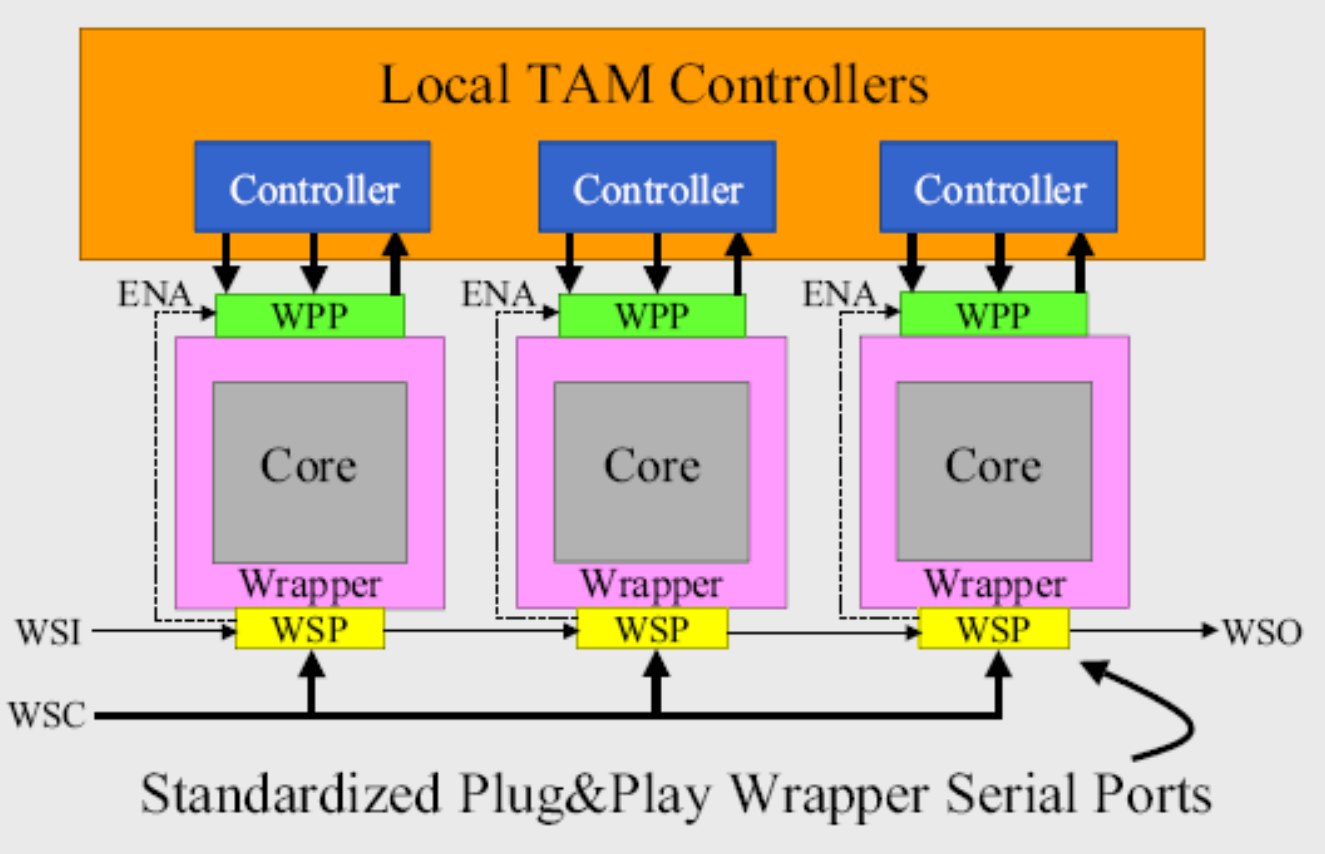
P1500 wrapper configurations



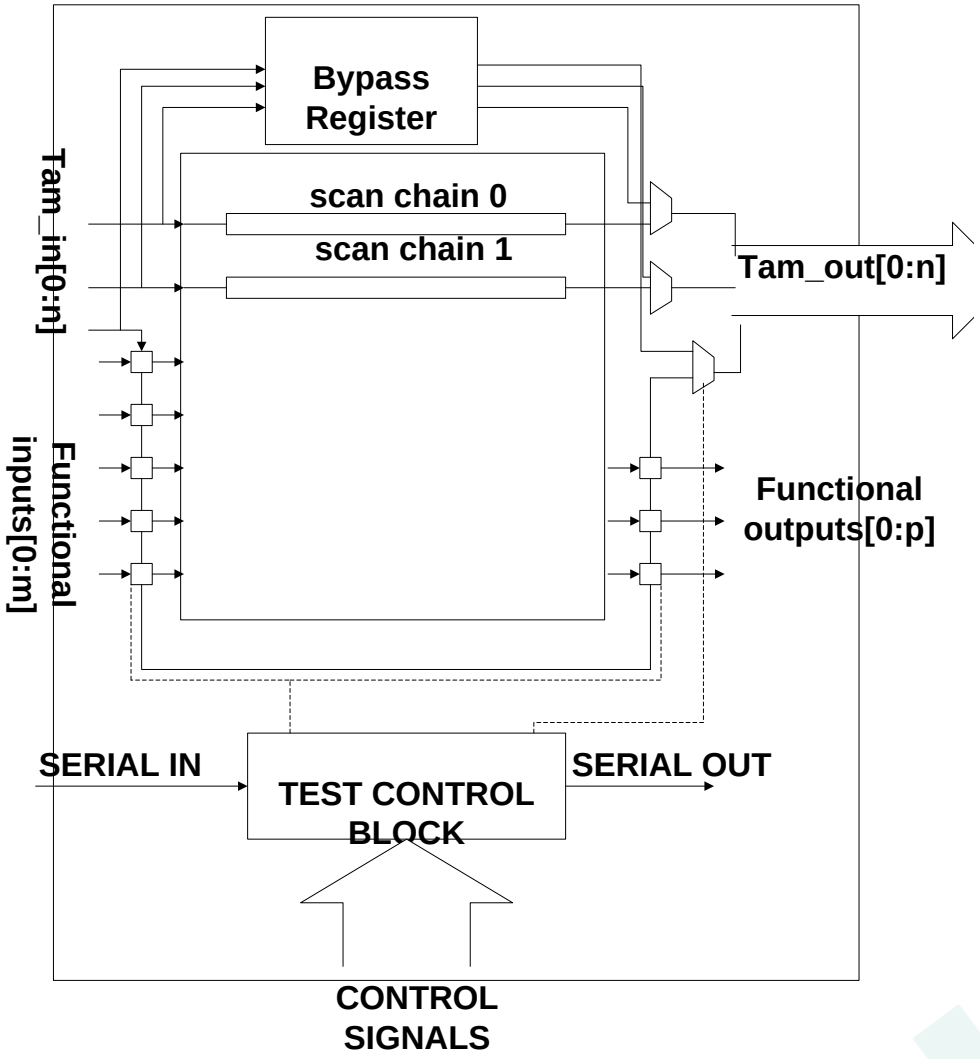
P1500 wrapper configurations



P1500 wrapper configurations



Convergence of P1500 and Test Rail



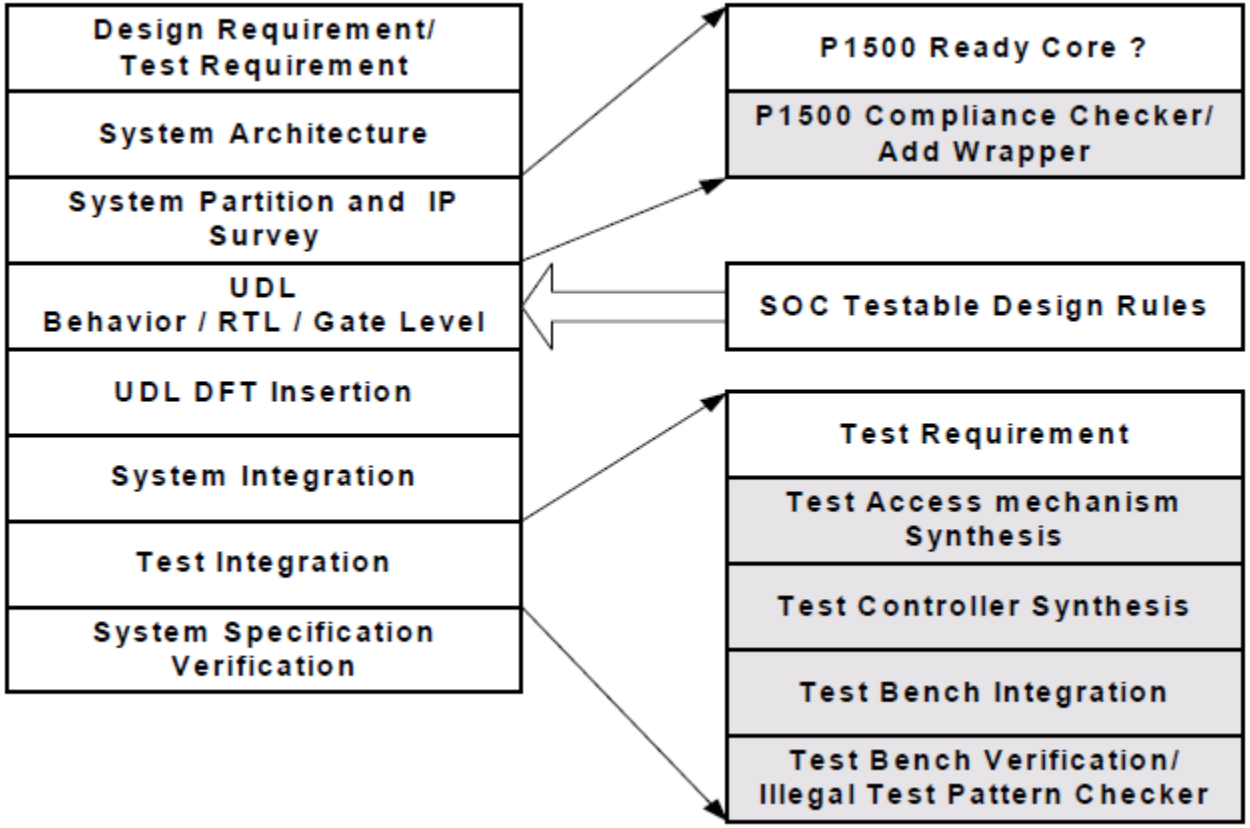
SoC Test Methodology

- Study functions and architectures in each module of a general SoC
- Design each module
- Apply proper testing methods to each module
- Add wrapper to each core (module)
- Integrate the IP testing using a P-1500 like structure

Development of Testable SoC

- Testing for digital components
- Testing for analog components
- Testing for memory components
- Wrapper for each core
- Define Test Access Mechanism
- Test integration
- Testable design flow

SoC Testable Design Flow

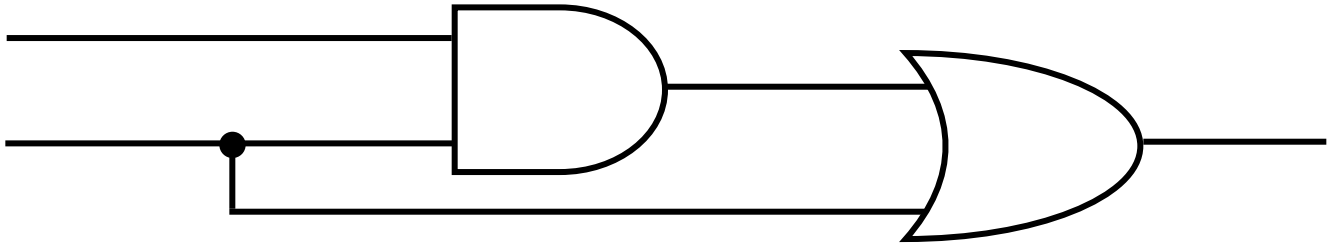


Conclusions

- SoC testing is a must
- Standard not defined yet
- Even when standard is defined, many details need to be implemented
- Component testing needs to consider test reuse
- Automation of wrapper generation & system chip interface must be done
- Tools for linking design flow
- Test access mechanism is to be user-defined, hence test engineer will be keeping his job
- Mixed-mode testing in SoC is urgent

Quiz V

1. What is the total number of single stuck-at faults, counting both stuck-at-0 and stuck-at-1, in the following circuit?



2. Can both NANDs in the following circuit be tested for stuck-at-1 fault simultaneously? How?