ECE 715
System on Chip Design and Test

Lecture 20

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

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ECE 715

Power Dissipation in CMOS Circuits

Lecture By

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Why should we study about Power Dissipation?

Why should we study about Power Dissipation?

- Degradation of Performance
- Reliability Issue

Power Issue in VLSI Circuit

Why Power issue has become an important concern in the present day VLSI circuit realization?

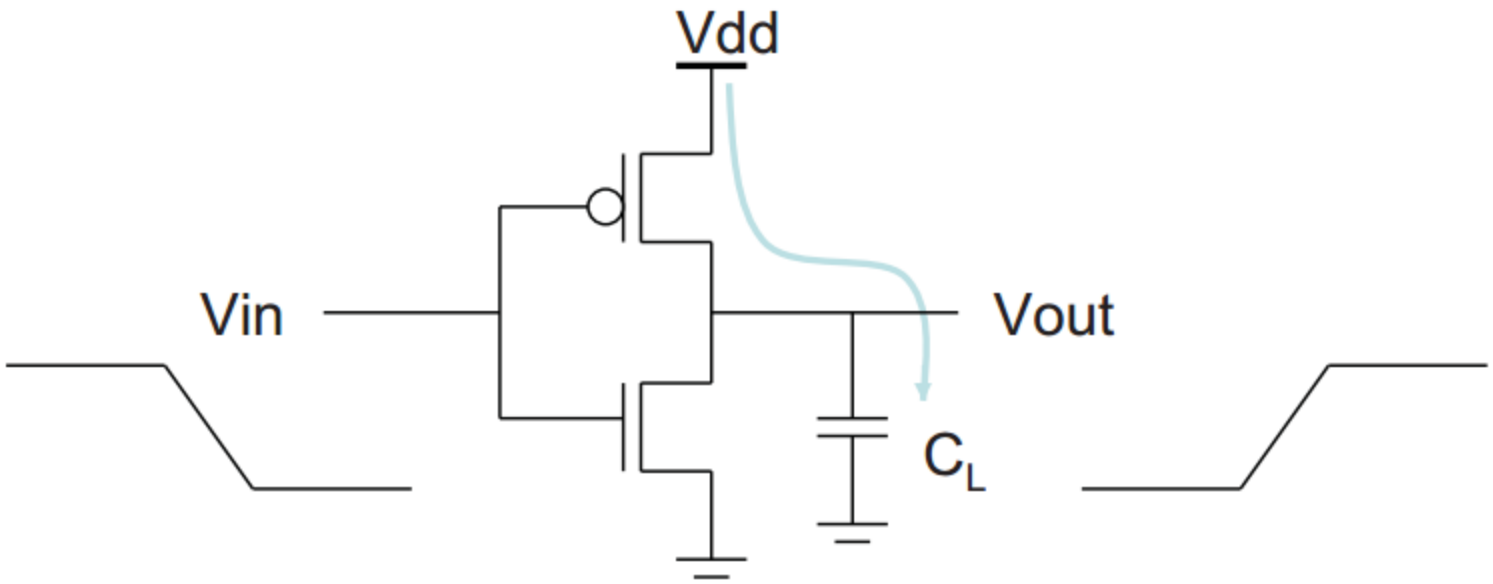
- Higher speed of operation
- Greater device leakage currents
- Increasing transistor count

Where Does Power Go in CMOS?

- Dynamic
  - Charging & Discharging of Capacitors
  - Short-circuit
- Static
  - Leakage

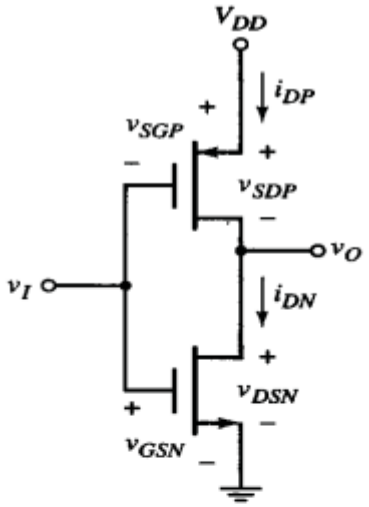
$$P_{total} = P_{dyn} + P_{stat}$$
$$P_{tran} + P_{sc} + P_{stat}$$

Dynamic Power Consumption



Dynamic Capacitive Power and Energy stored in the PMOS Device

Case I: When the input is at logic 0



PMOS is conducting and NMOS is in cutoff mode
The load capacitor must be charged through the PMOS device.
Power dissipation in the PMOS transistor is given by:

$$P_P = i_L V_{SD} = i_L(V_{DD}-V_O)$$

The current and output voltages are related by:

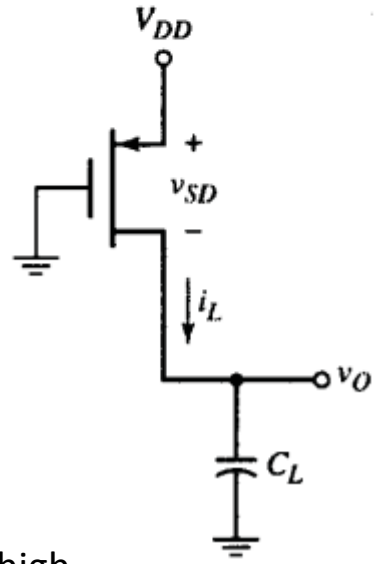
$$i_L = C_L dv_O/dt$$

Energy dissipation in the PMOS device as the output switches from low to high:

$$E_P = \int_0^\infty P_P dt = \int_0^\infty C_L(V_{DD} - v_O)\frac{dv_O}{dt}\,dt, E_P = C_L V_{DD}\int_0^{V_{DD}} dv_O - C_L\int_0^{V_{DD}} v_O dv_O$$

$$E_P = C_L V_{DD} v_O\Big|_0^{V_{DD}} - C_L\frac{v_O^2}{2}\Big|_0^{V_{DD}}, E_P = (C_L V_{DD} V_{DD} - 0) - (C_L\frac{V_{DD}^2}{2} - 0)$$

$$E_P = \frac{1}{2}C_L V_{DD}^2$$



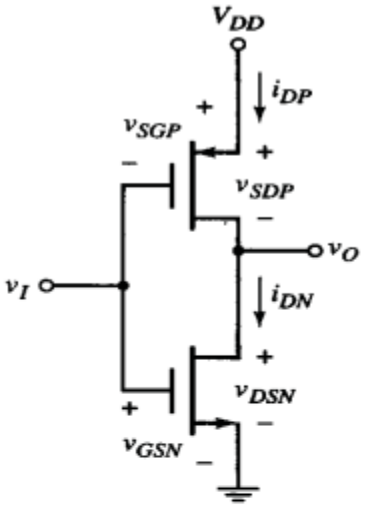
Above equation showed the energy stored in the capacitor C_L when the output is high.

Power Dissipation and Total Energy Stored in the CMOS Device

Case II: when the input is high and out put is low:

During switching all the energy stored in the load capacitor is dissipated in the NMOS device.
The energy dissipated in the NMOS inverter can be written as,

$$E_N = \frac{1}{2} C_L V_{DD}^2$$



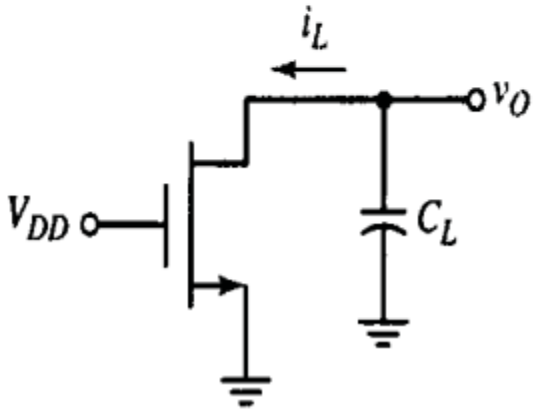
The total energy dissipated during one switching

$$E_T = E_P + E_N = \frac{1}{2} C_L V_{DD}^2 + \frac{1}{2} C_L V_{DD}^2 = C_L V_{DD}^2$$

The power dissipated

$$E_T = Pt \Rightarrow \quad P = \frac{E_T}{t} \Rightarrow \quad P = fE_T \Rightarrow \quad fC_L V_{DD}^2$$

This implied that the power dissipation in the CMOS inverter is directly proportional to switching frequency and VDD^2



Dynamic capacitive power

Formula for dynamic power: $P_{dyn} = C_L V_{DD}^2 f$

Most gates do not operate / switch at every clock cycle, they are often accompanied by a factor α, called the activity factor.

Now, the dynamic power dissipation may be re-written as

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

Observations:

- Not a function of transistor sizes!
- A function of switching activity!

Lowering Dynamic Power

Capacitance:
Function of fan-out,
wire length, transistor sizes

Supply Voltage:
Has been dropping with
successive generations

$$P_{dyn} = C_L V_{DD}^2 f$$

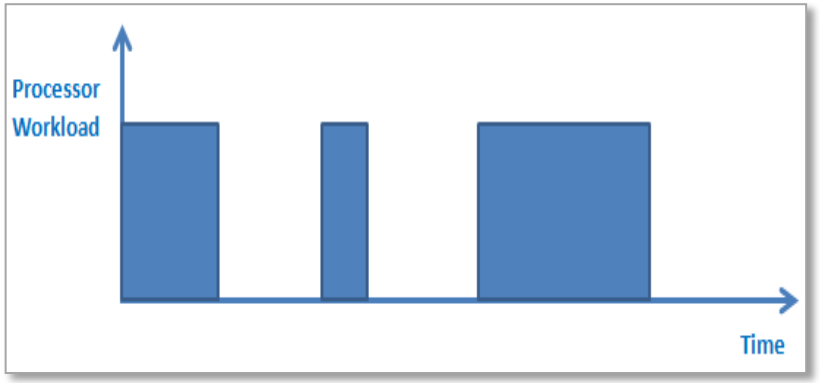
Clock frequency:
Increasing…

Dynamic Power Reduction Techniques:

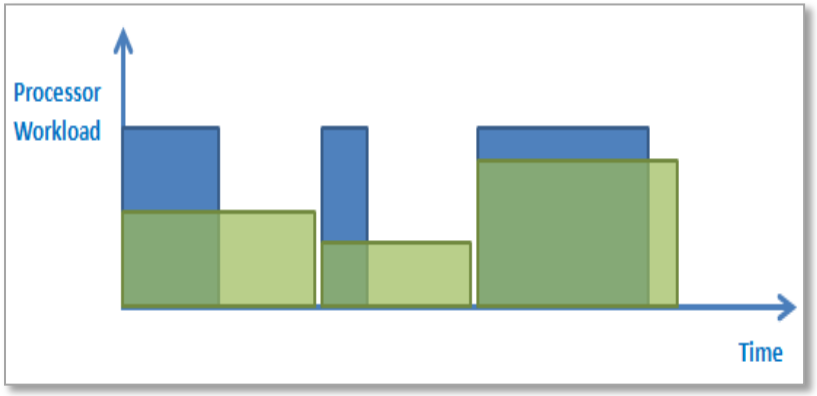
- ❑ Clock Gating
- ❑ Multy V_{DD}
- ❑ DVFS (Dynamic Voltage & Frequency Scaling)

DVFS

DVFS dynamically scales the operating frequency and supply voltage to provide just enough performance to process the application workload while meeting the compute time, and thereby, reducing the energy dissipation.



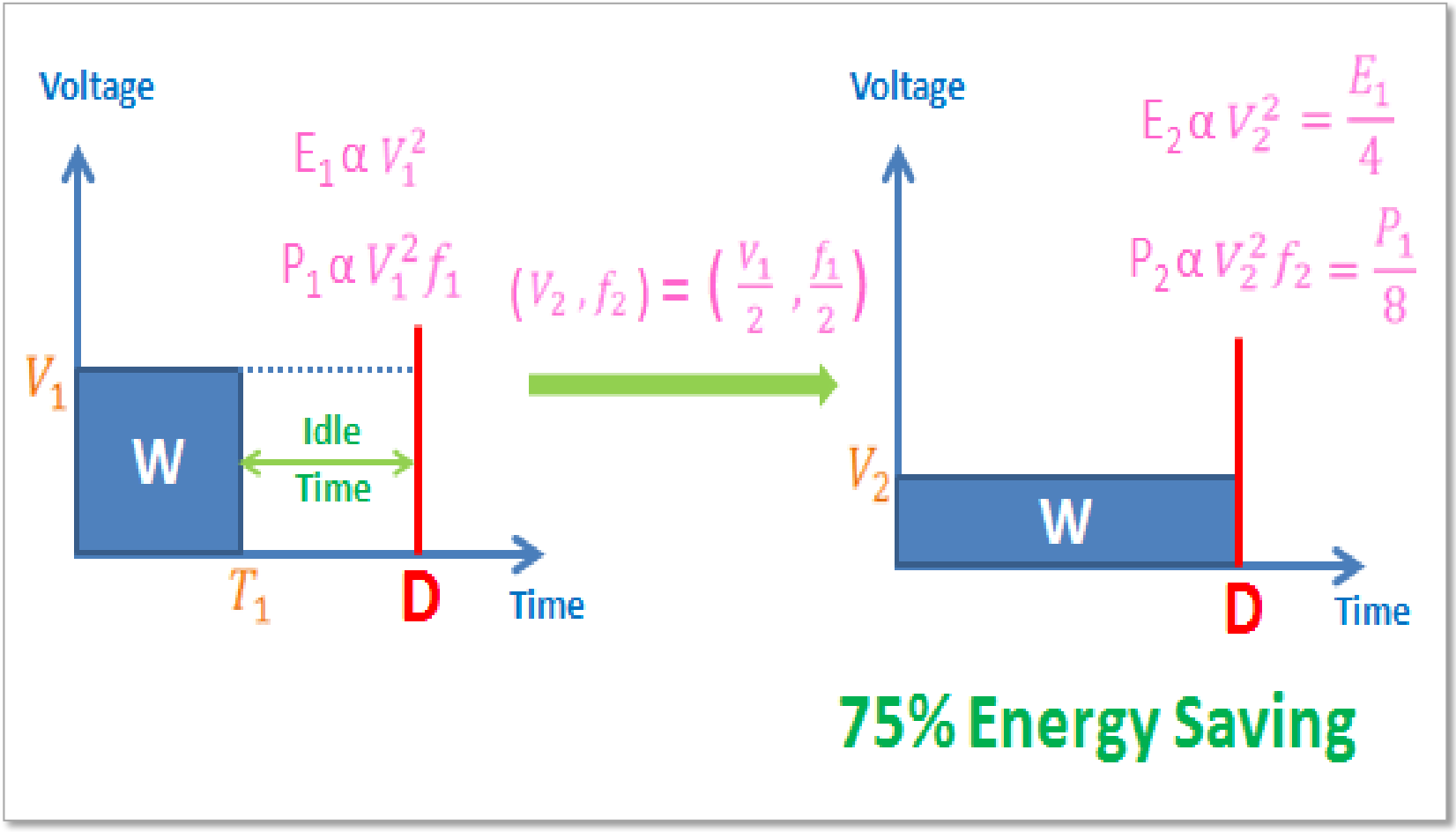
A typical workload pattern with tasks and idle time between tasks



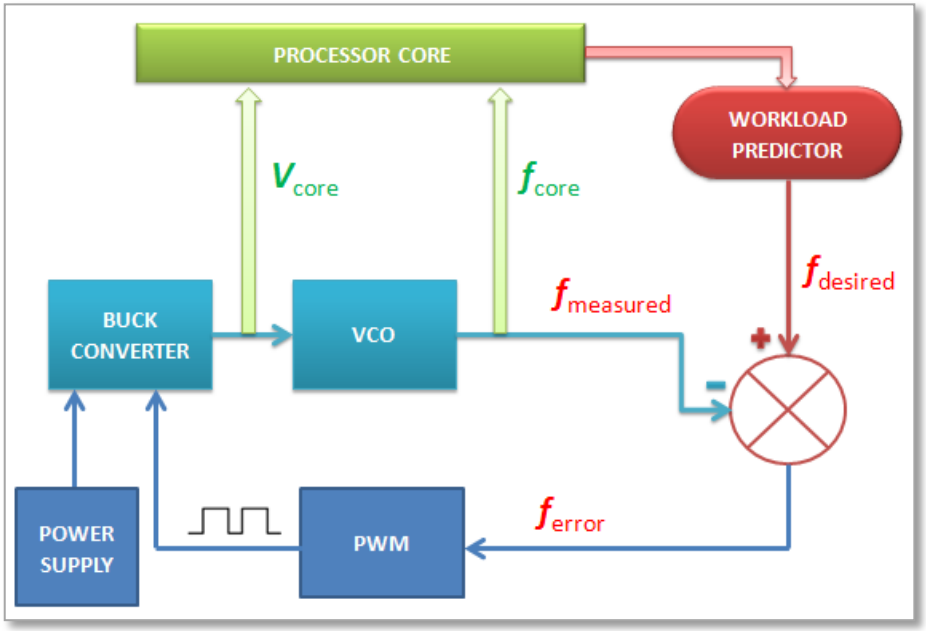
A typical workload pattern with DVFS technique

The DVFS technique can significantly improve the processor energy efficiency especially for portable systems which are battery or UPS powered electronic devices.

Energy saving calculation in DVFS technique



Block diagram of DVFS Control Loop



Sequence of Operation of the Control Loop

1. Workload Predictor will decide the desired frequency in the next DVFS interval.

2. An Adder will generate an error frequency value from the predicted frequency of the next DVFS interval and the measured frequency of the current DVFS interval.

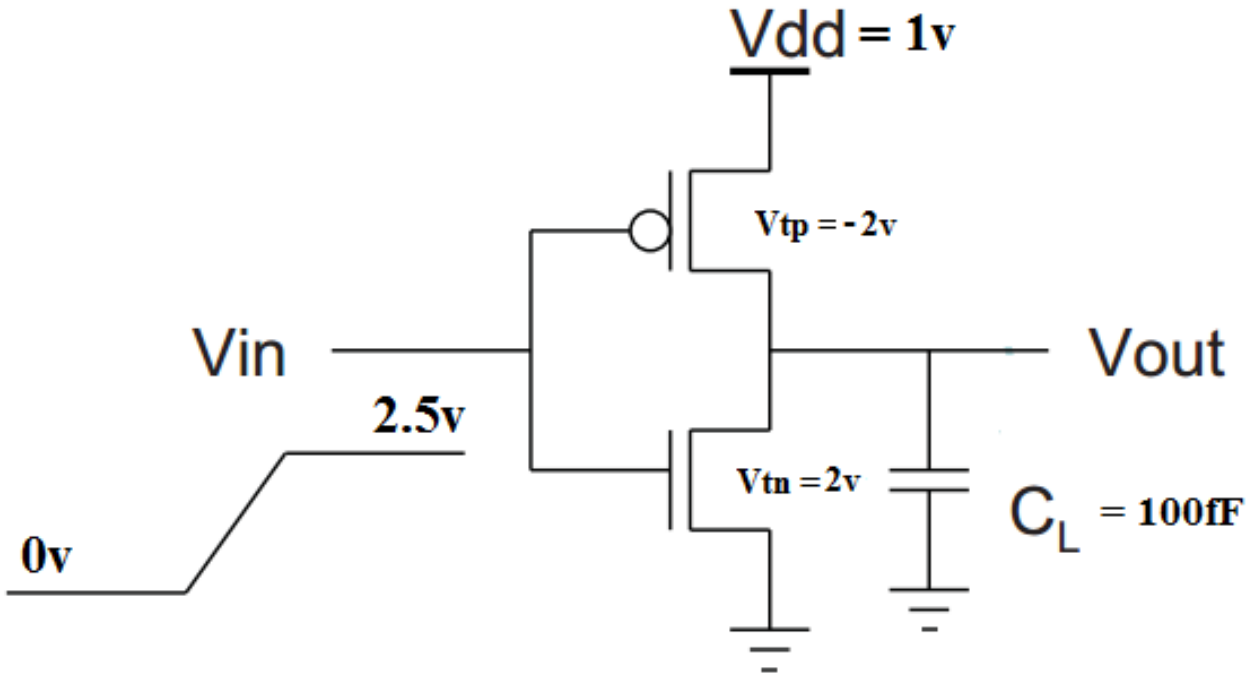
3. The value of error frequency will control the duty cycle of the modulated pulse generated at the output of the Pulse Width Modulator.

4. Buck Converter will take the input from the power supply and a controlled input as the PWM modulated signal. This generates the required voltage level for the processor.

5. The dc voltage generated by the Buck Converter will be the controlled voltage for the VCO and the required frequency level for the processor will be generated.

Activity

Find the Dynamic Power dissipation of the following CMOS inverter circuit.



The operating frequency of the circuit is 1GHz and consider the activity factor as $\alpha = 1$

Static Power in Submicron Rregion

- What does “Static” mean in CMOS VLSI Circuits?

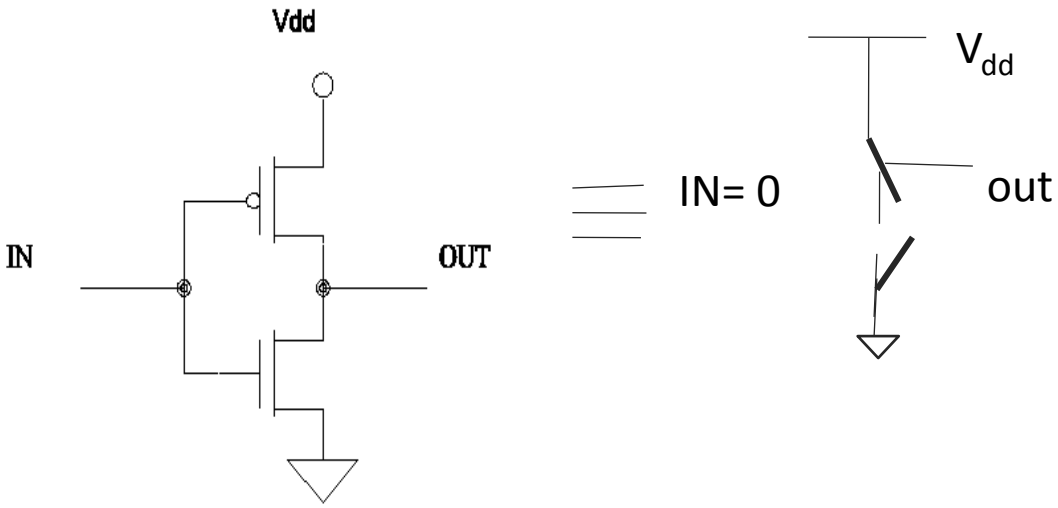


Fig 1 : CMOS inverter

- Active Mode - While chip is doing useful work
- Standby Mode - Chip is idle (clocks are stopped power due to switching is saved)
- Sleep Mode - No supply to functionally inactive block in chip

Static Power in Submicron Rregion

- Why is “Static Power” so significant in Deep Submicron Technology?

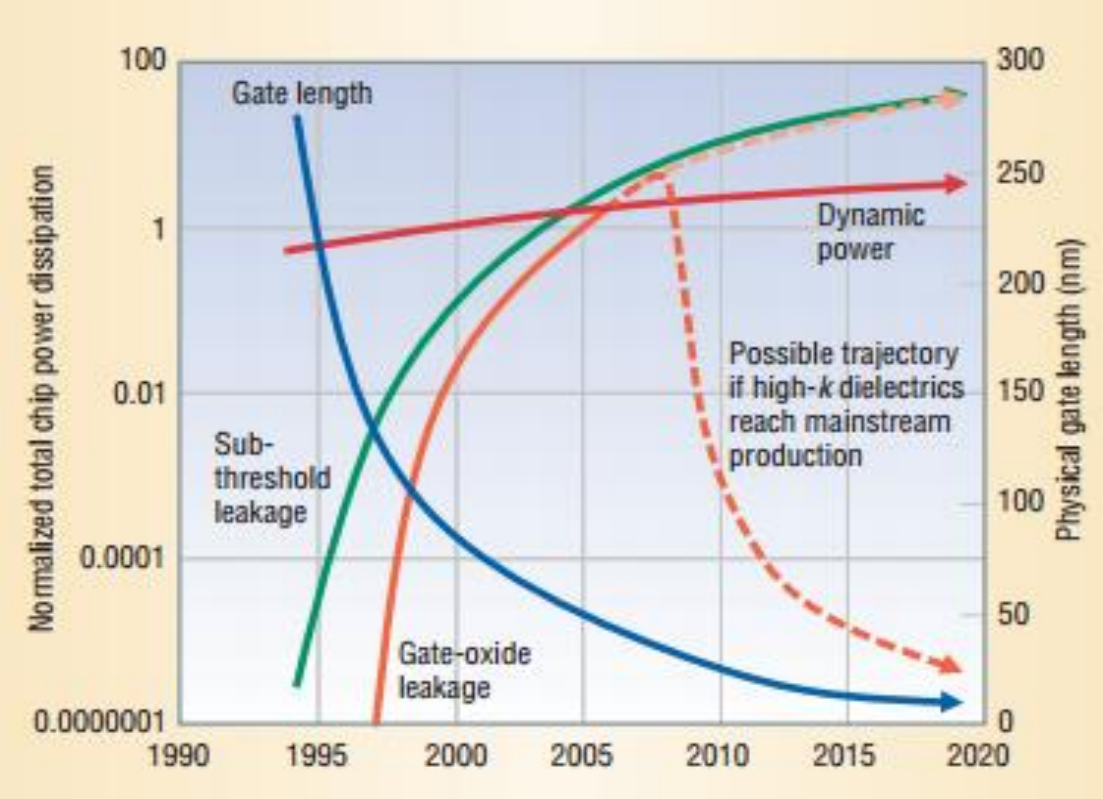


Fig 2 : Dynamic and Static power dissipation according to ITRS

Source of Static Power Dissipation

- Static power dissipation due to
  - Sub-threshold leakage through OFF transistors
  - Gate leakage through gate dielectric (gate to body)
  - Junction leakage from source/drain diffusions to body or well

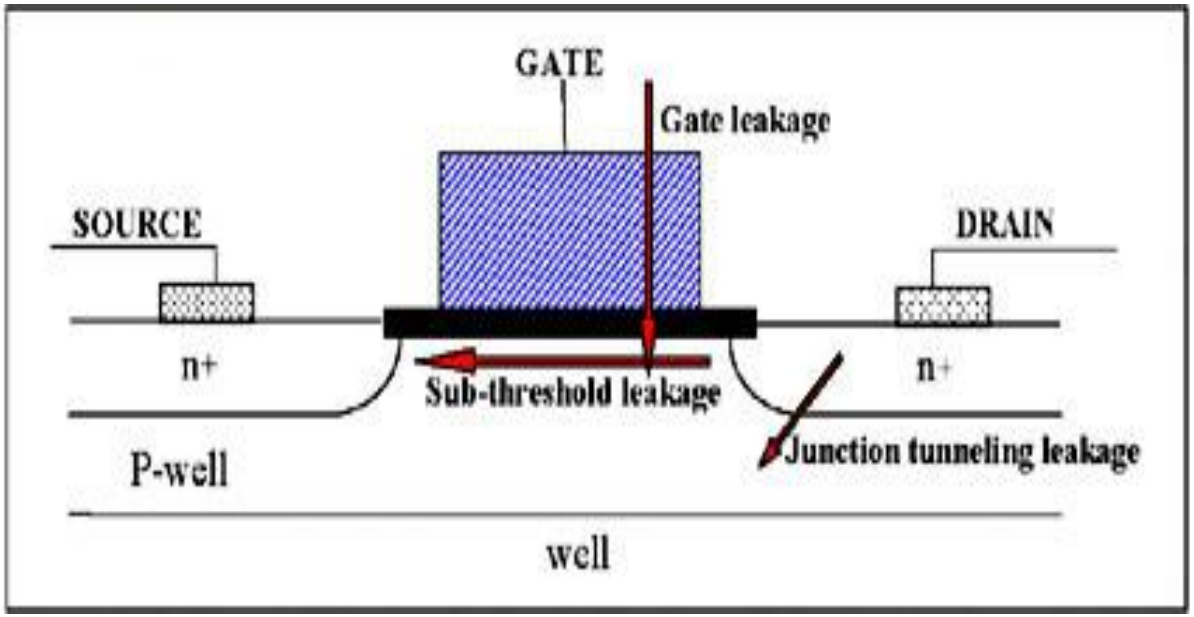


Fig 3 : Leakage Current in a Transistor

Sub-threshold Leakage

when transistors are nominally OFF, they leak small amounts of current from drain to source called sub-threshold

- For Vds > 50 mV (typical value of V_{th})

$$I_{sub} \approx I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{DD}) - k_\gamma V_{sb}}{S}}$$

- I_{off} = leakage at $V_{gs} = 0$, $V_{ds} = V_{DD}$

η DIBL coefficient typically around 100 mV/V for a 65 nm transistor

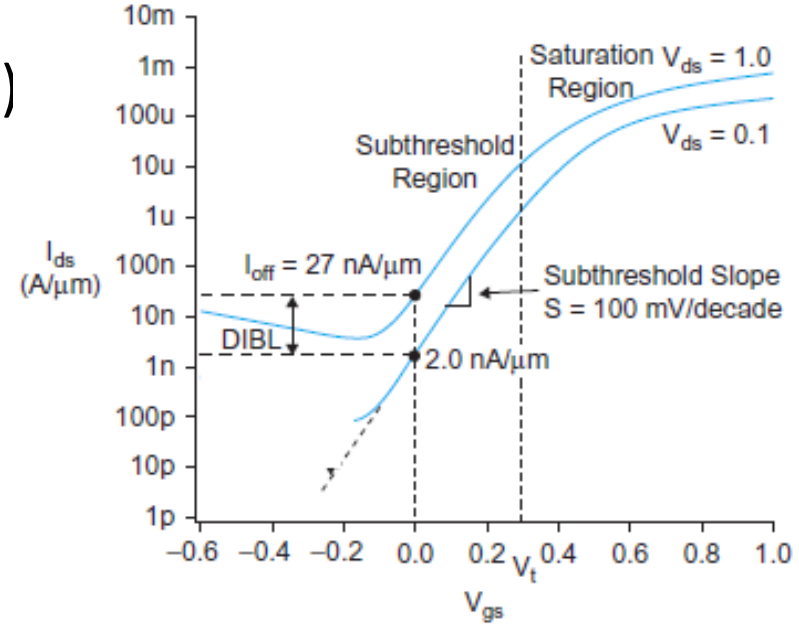


FIGURE 2.20 I-V characteristics of a 65 nm nMOS transistor at 70 °C on a log scale

I_{off} is a key process parameter defining the leakage of a single OFF transistor range from 100nm/um at low V_{th} to 1nm/um at high V_{th}

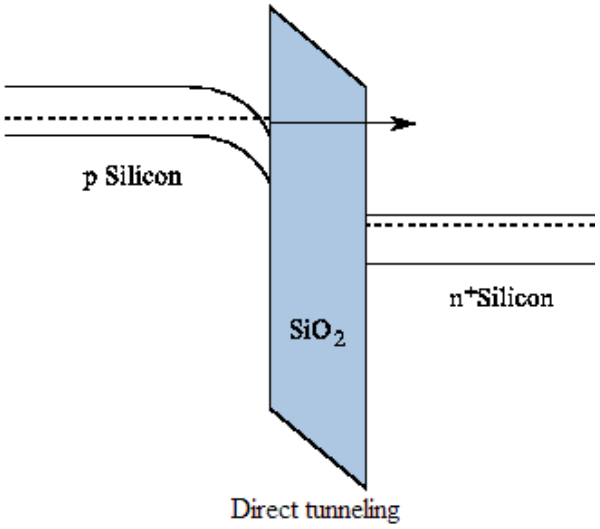
k_γ *is the body effect coefficient*

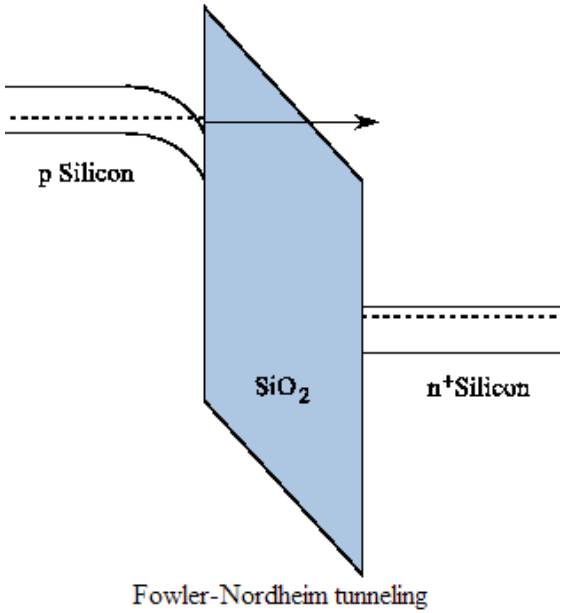
Gate Leakage

- It is quantum-mechanical effect caused by tunneling through the extremely thin gate dielectric.

Two physical mechanisms for gate tunneling are

- Direct tunneling Important at - Low voltage and thin oxides (dominant leakage component)
- Fowler-Nordheim (FN) tunneling – High voltage and Moderate thickness





Junction Leakage

- The p–n junctions between diffusion and the substrate or well form diodes
- Keep Well at high voltage and body at low voltage forms reverse biased junction hence leakage

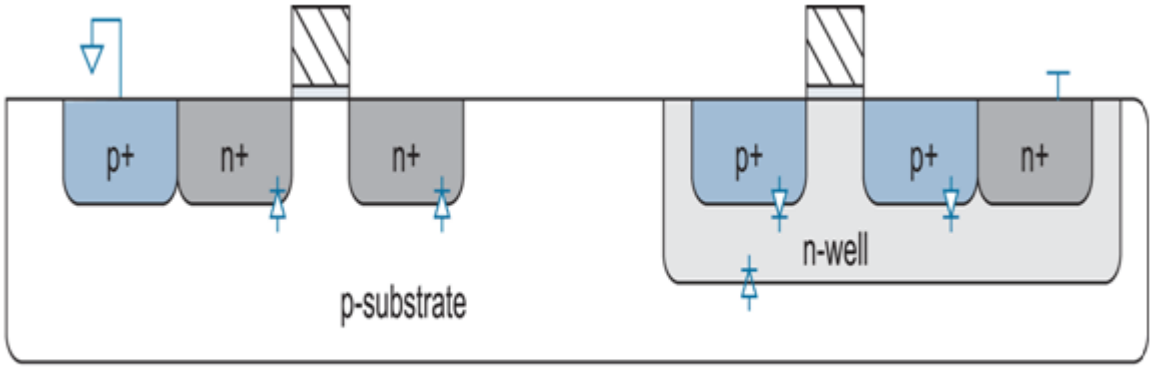
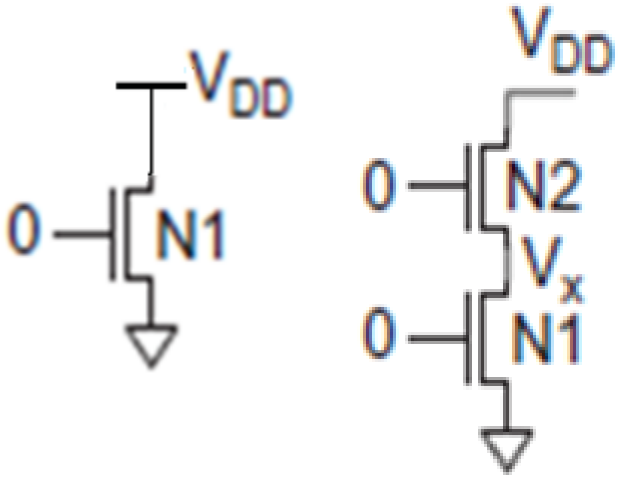


Fig 4 : Reveres biased pn junction diodes in CMOS

Leakage Reduction Technique

- Stack Effect



$$I_{sub} \approx I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{DD}) - k_\gamma V_{sb}}{S}}$$

Fig 5 : Series off transistor for demonstrating stack effect

- If *Vx is small, N1 will see a much smaller DIBL effect and will leak less*
- As *Vx rises, V_{gs} for N2 becomes* negative, reducing its leakage

Leakage Reduction Technique ..

- Power Gating

Reduction in static current during sleep mode is to turn off the power supply to the sleeping blocks this technique called **Power Gating**

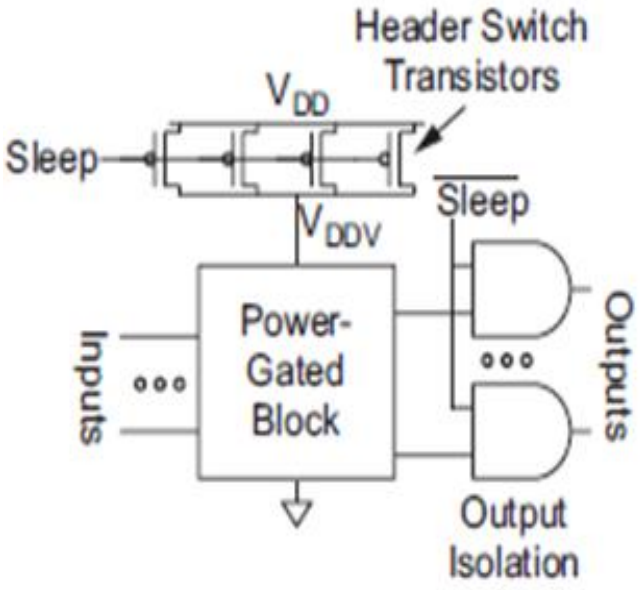


Fig 6 : Power Gating

Note : Power gating introduces a number of design issues

Leakage Reduction Technique ..

Multiple V_{th}

- Low V_{th} -- Used for high performance in critical circuit
- High Vth -- Used for rest of circuit (95%) for low leakage

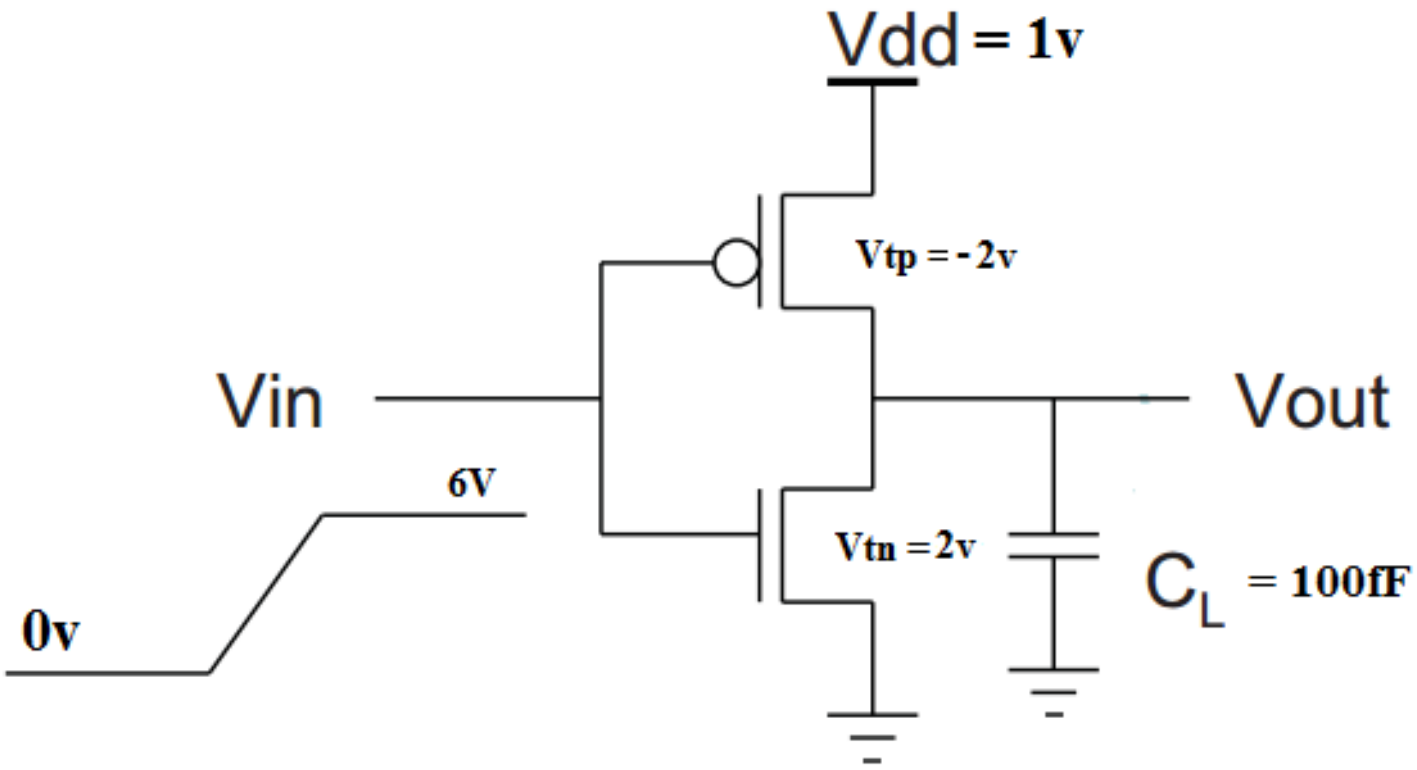
$$V_{th} = V_{th0} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}) \quad \Rightarrow \quad V_{th} = V_{th0} + k_\gamma V_{sb}$$

Here $\gamma = \dfrac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$ $\phi_s = 2v_t \ln \dfrac{N_A}{n_i}$ $k_\gamma = \dfrac{\gamma}{2\sqrt{\phi_s}}$

Note : body bias can intentionally be applied to alter the threshold voltage, permitting trade-offs between performance and sub-threshold leakage current

Activity

Let both the transistors are in 65nm technology. Which is the major leakage current component for the NMOS over here.



Thank You