NAME _____
First Last

Student ID# _____

STONY BROOK UNIVERSITY

COMPUTER SCIENCE DEPARTMENT

MIDTERM #1 EXAMINATION
VERSION B

CSE 320
Spring Semester 2012
February 27, 2012

This is a closed-book exam. (80 minutes)
Use this form for your work and return it.

The exam has 7 problems.
It is crucial to show all work done on the provided paper.

#1 _____	(8 pts)	#5 _____	(15 pts)
#2 _____	(12 pts)	#6 _____	(20 pts)
#3 _____	(20 pts)	#7 _____	(15 pts)
#4 _____	(10 pts)		

TOTAL _____ (100 Max)

1 [1 pt each] Multiple Choice. Write in the correct answer.

_____ A 2-level NOR-NOR gate representation is NOT equivalent to which of the following (select all that apply)
(a) 2-level AND-OR (b) 2-level OR-AND (c) Sum-Of-Products
(d) Product-Of-Sums (e) Minterm Expression (f) Maxterm Expression

_____ An ISA does not specify which of the following?
(a) number formats (b) register assignment (c) memory size (d) addressing modes
(e) instruction set

_____ A multiplexer with 3 selector bits has how many input values?
(a) 2 (b) 5 (c) 8 (d) 16 (e) 32

_____ A MIPS register file is capable of reading ___ registers at a time.
(a) 0 (b) 1 (c) 2 (d) 3 (e) 4

_____ What type of combinatorial circuit maps a binary value of size n to one of 2^n outputs?
(a) Encoder (b) Decoder (c) Half Adder (d) XOR gate (e) Multiplexor

_____ A flip-flop
(a) stores multiple bits of data (b) stores a single bit of data
(c) has a single output value, Q (d) flips its value each clock cycle

_____ Which of the following is not a MIPS addressing mode
(a) Displacement (b) Direct or absolute (c) Immediate (d) Register

_____ During the fetchstage, the PC contains
(a) the current instruction to execute (b) the memory address of the data
(c) the memory address of the current instruction (d) the memory address of the next instruction

2 [12pts] Short Answer

(i) [2 pts] What is the difference between a half-adder and a full-adder?

(ii) [3 pts] What is the advantage of fixed length instructions over variable length instructions? Which is preferred if code size is important? Why?

(iii) [3 pts] What is the critical path of a circuit? Why is it important?

(iv) [4 pts] Define RISC. Define CISC. Name two difference between RISC and CISC.

3 [20 pts] Boolean Expressions.

Functions F, G, and H are defined in the following way:

$$F = B'C' + A'C' + AB$$
$$G = A'B'C' + B'C' + A'C' + BC'$$
$$H = C' + BC' + A'B'C'$$

(a) [2 pts] How many literals appear boolean expression G? _____

(b) [6 pts] Which of the functions are equivalent? (Hint: Create truth table) Show your approach!

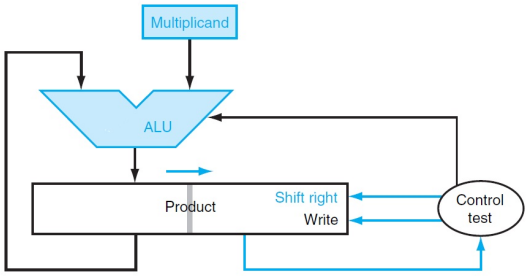
(c) [6 pts] Using Boolean algebra, simplify expression G.

(d) [6 pts] Implement $F = B'C' + A'C' + AB$ using a 2-level NAND-NAND network.
DO NOT SIMPLIFY!

4 [10 pts] Implement Z using a 4-input multiplexor (2-selector) and NOR gates.
DO NOT SIMPLIFY **THE INITIAL** EXPRESSION.

$$Z = a'b'c'd + a'bc'd' + a'b'cd + ab'c'd + abcd + abcd'$$

5 [15pts] Integer Multiplication.
Consider the following multiplication hardware for unsigned 6-bit numbers: $101011_2 \times 011001_2$.



(a) [7pts] How many bits are required for each hardware component? What are the initial register vales?

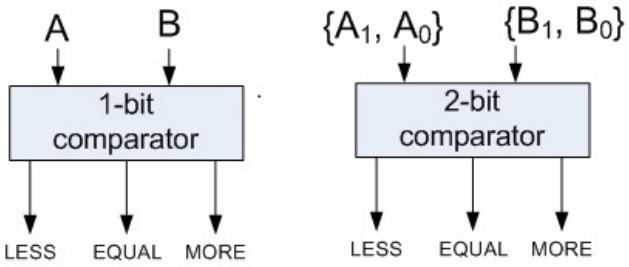
	Bit Size	Initial Value
ALU	_____	
Product	_____	_____
Multiplicand	_____	_____

(b) [5pts] At the end of the 3rd iteration, what is the value of the Product register?

(c) [3pts] If the multiplicand and multiplier are exchanged (ie $A \times B$ vs. $B \times A$), then

Does the number of iterations of the algorithm change? YES / NO
Does the number of performed additions change? YES / NO
Does the required execution time change? YES / NO

7 [15pts] Consider the 1-bit comparator unit as specified below. Build a 2-bit comparator (as shown) using two 1-bit comparators and AND, OR, NOT gates.
Hint: When comparing two 2-bit numbers bit by bit, how do the MORE, LESS and EQUAL signals for each unit combine to produce the MORE LESS and EQUAL signal outputs?



$A < B$, LESS $= A'B$ $A = B$, EQUAL $= AB + A'B'$ $A > B$, MORE $= AB'$

Extra space provided.

Extra space provided.

Boolean Identities

In a few instances, the AND operation is represented by a dot ($\cdot$) for clarity.

$x + 0$	$=$	x	identity	$x \cdot 1$	$=$	x
$x + 1$	$=$	1	null	$x \cdot 0$	$=$	0
$x + x$	$=$	x	idempotence	$x \cdot x$	$=$	x
$x + \bar{x}$	$=$	1	complementarity	$x \cdot \bar{x}$	$=$	0
$\overline{(\bar{x})}$	$=$	x	involution			
$x + y$	$=$	$y + x$	commutative	$x \cdot y$	$=$	$y \cdot x$
$x + (y + z)$	$=$	$(x + y) + z$	associative	$x(yz)$	$=$	$(xy)z$
$x(y + z)$	$=$	$xy + xz$	distributive	$x + yz$	$=$	$(x + y)(x + z)$
$\overline{(x + y)}$	$=$	$\bar{x} \cdot \bar{y}$	deMorgan	$\overline{(xy)}$	$=$	$\bar{x} + \bar{y}$
$x + xy$	$=$	x	absorption	$x(x + y)$	$=$	x
$x + \bar{x}y$	$=$	$x + y$	no-name	$x(\bar{x} + y)$	$=$	xy
$xy + yz + \bar{x}z$	$=$	$xy + \bar{x}z$	consensus	$(x + y)(y + z)(\bar{x} + z)$	$=$	$(x + y)(\bar{x} + z)$