ECE 314/514: Digital VLSI Design

Instructor: Sujay Deb

Meeting: Mon 11:00 AM & Wed 9:30 AM @ C03

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Before we start..

- Please answer following questions:
  - Please state your expectations from this course?
  - How will this course help you in achieving your goals?

Goal of the Course

- Learn the principles of VLSI Design
  - Learn to design and implement state-of-the-art digital Very Large Scale Integrated (VLSI) chips using CMOS technology
  - Understand the complete design flow
  - Be able to design state-of-the-art CMOS chips in industry
- Employ hierarchical design methods
  - Use integrated circuit cells as building blocks
  - Understand design issues at the layout, transistor, logic and register-transfer levels
  - Use commercial design software in the lab

Course Information

- Instructor:
  - Sujay Deb (sdeb@iiitd.ac.in)
  - Office A304 (Office Hours: Mon and Wed 4-5 PM)
- TA: Hemanta Kumar Mondal (hemantam@iiitd.ac.in)
- More on the course
  - Course web page: We will use PIAZZA for everything!
  - Sign up: https://piazza.com/iiitd.ac.in/fall2014/ece314514/home
  - Prerequisites: logic design, basic computer organization
  - Textbook: Weste and Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd Edition, 2006
  - Lectures and discussion in class will cover basics of course
  - Homework, Laboratory exercise will help you gain a deep understanding of the subject

Grading structure

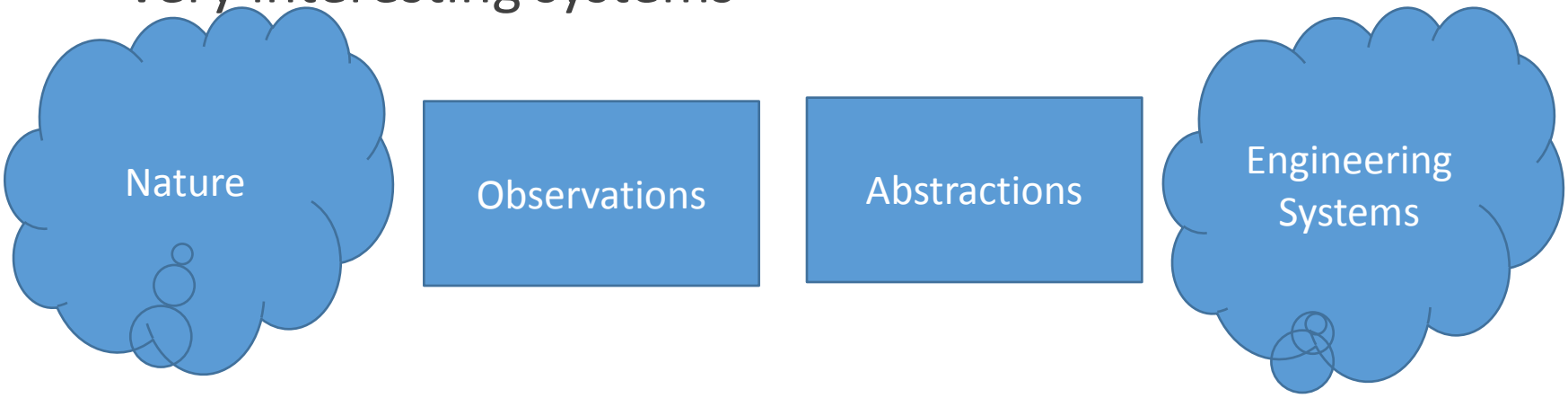
- Homework: 5%
- Reading Assignment: 5%
- Quiz: 5%
- Midterm: 25%
- Lab Assignments: 15%
- Term project: 20%
- Final: 25%

- Problems will be too long to complete the night before due, so please plan accordingly.
- Students are expected to work individually on the homework assignments.
- The lab assignments and project can be done in a group of two.
- Zero tolerance towards violation of Academic Integrity

- HW#0: Join PIAZZA and explore it!

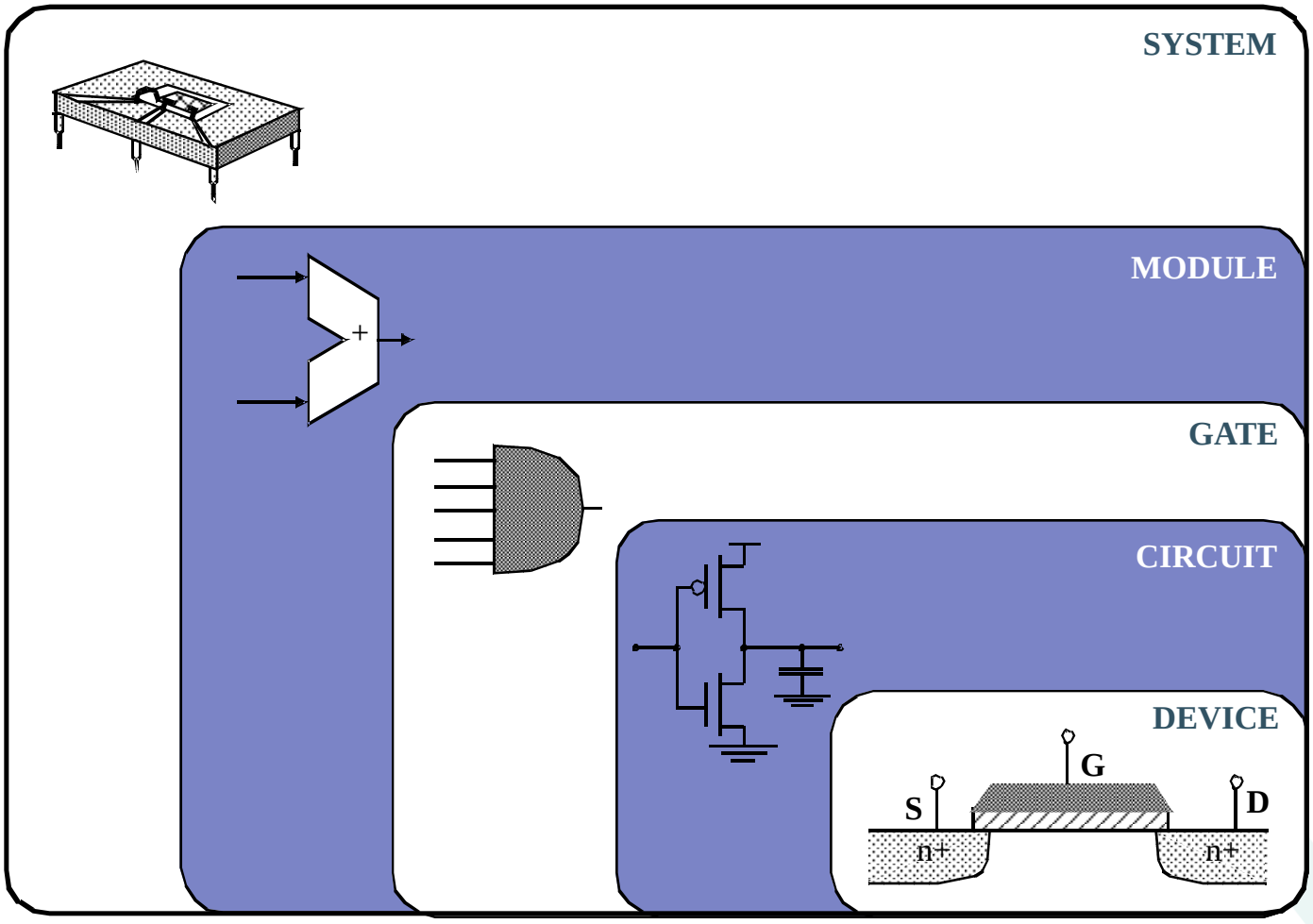
Overview

- What is Engineering?
  - the purposeful use of science
- We are here to employ the facts of nature to build very interesting systems



- Take complicated things, build layers of abstraction, and simplify things so that we can build useful systems.

Design Abstraction Levels



Course outline

- Introduction to CMOS circuits
- MOS transistor theory
- Circuit Characterization
  - Performance evaluation & optimization
- CMOS circuit logic and design
- Subsystem design
- Datapath design and analysis

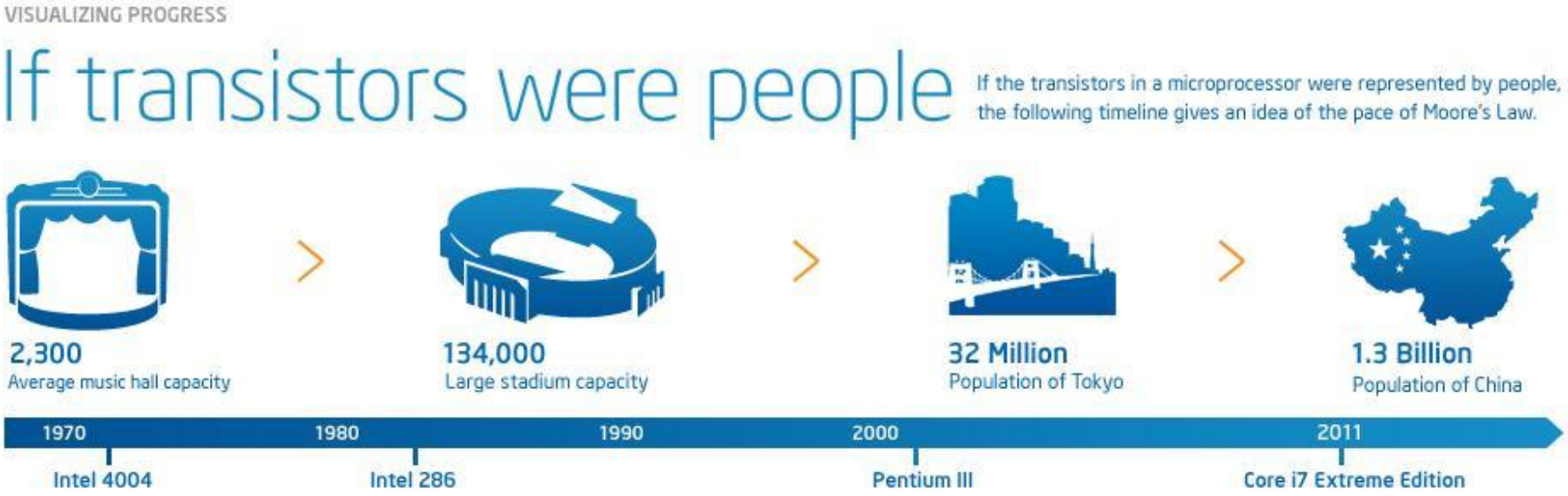
Solid State Devices

- Silicon
  - Doping
    - n-type, p-type silicon
  - Carriers
    - electrons and holes
- P-N junctions
  - 2 terminal devices
- Transistors
  - Bipolar Junction Transistors (BJT)
  - Metal Oxide Semiconductor (MOS)
    - 4 terminal devices
    - Main emphasis of this class
- History is very important. Do visit http://smithsonianchips.si.edu/ and explore other related resources
- Reading Assignment #1: Submit a report on 'Future of transistor and microprocessors' by 11/08. Details on Piazza.

Integrated circuits

- nMOS and pMOS devices
- Modeled as on-off switches
  - But a lot goes on inside!
- Complementary MOS (CMOS) circuit design methodology
  - Most common and widely used technique
  - But several other interesting techniques exist

Moore's Law

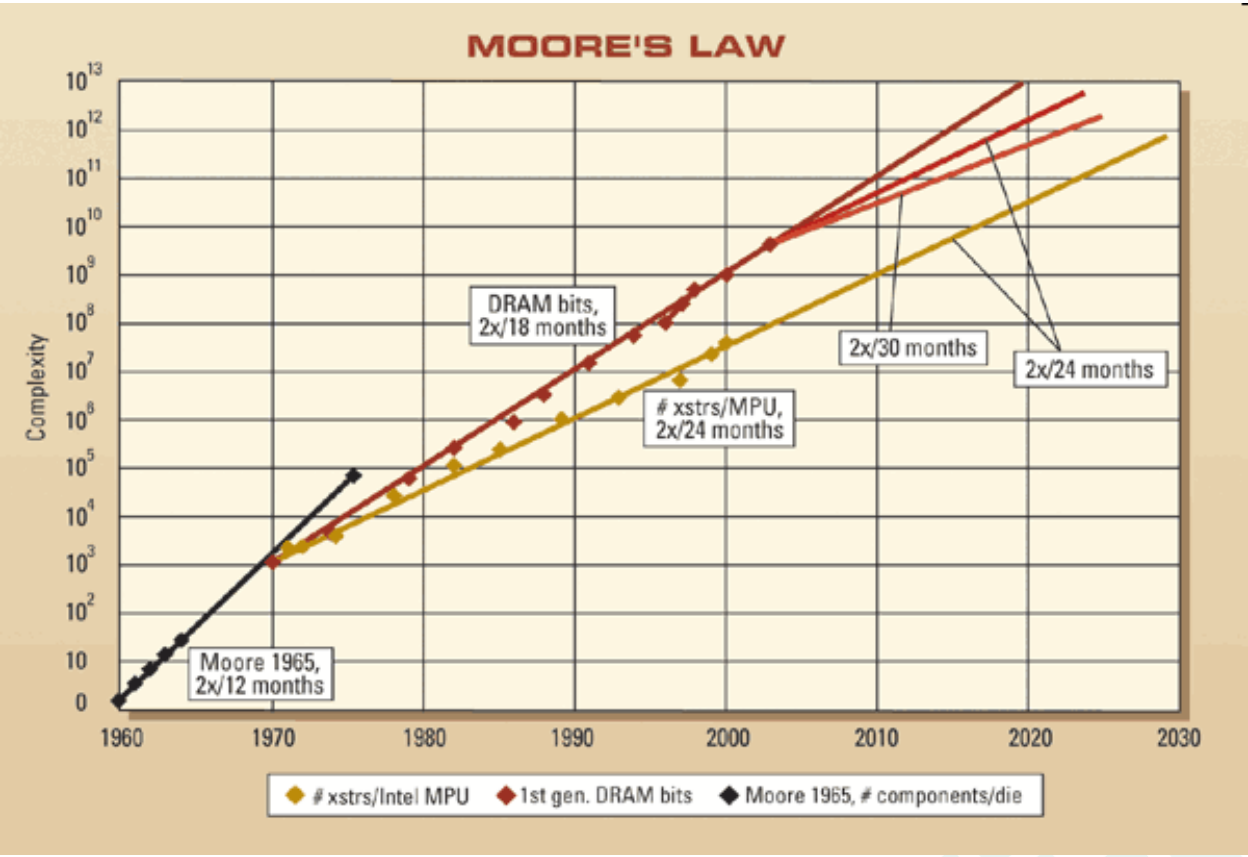


Courtesy:

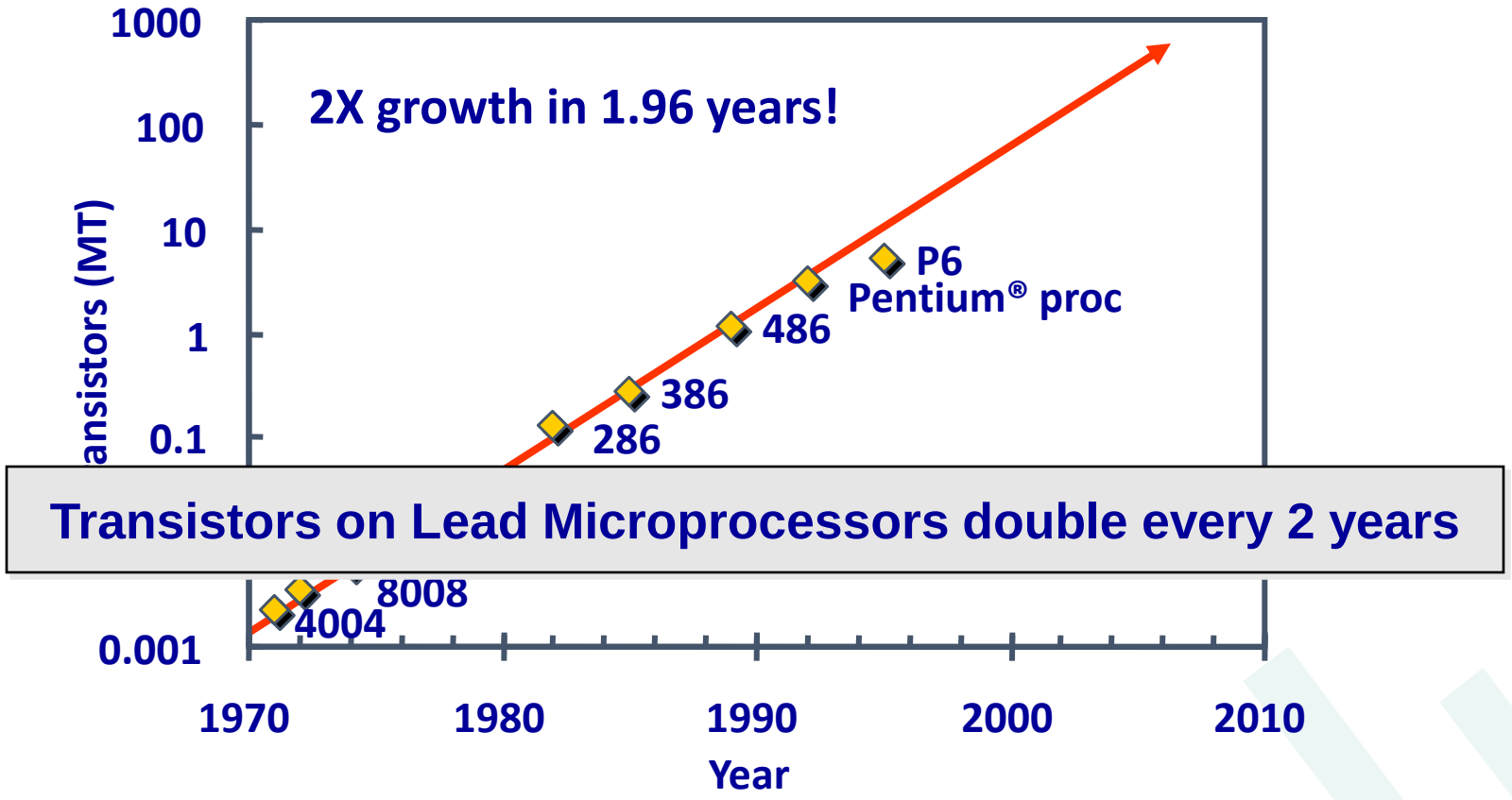
http://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html

Moore's Law continued..

- Number of components in an integrated circuit double every 2 years
- Signifies increase in computing capacity, memory and speed exponentially



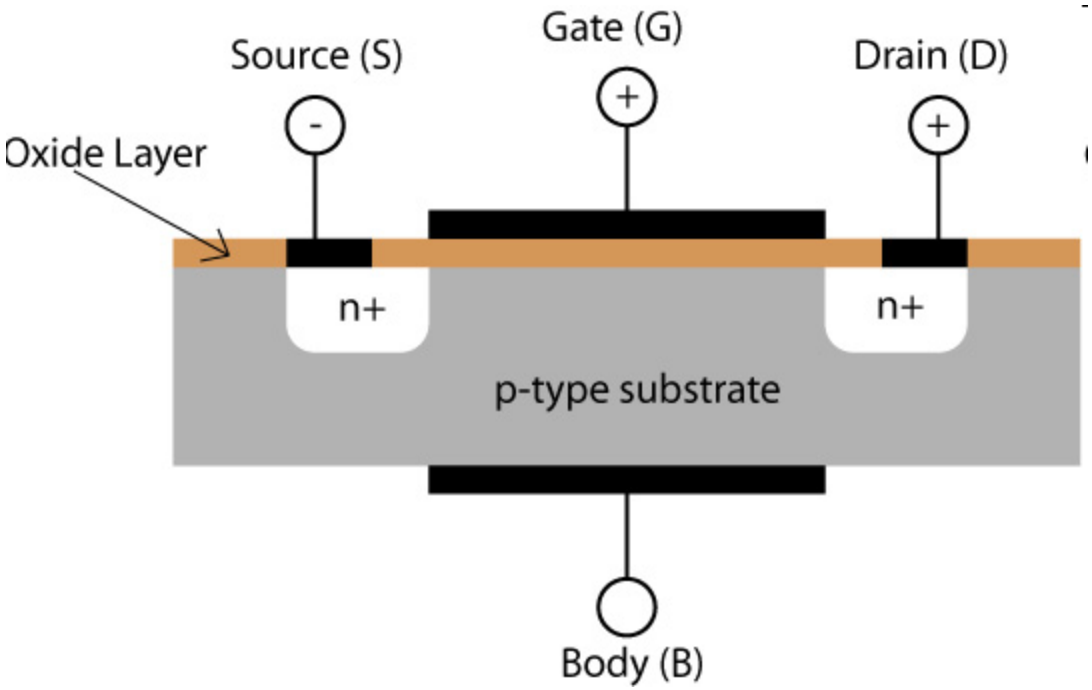
Moore's law in Microprocessors



Courtesy, Intel

MOS structure

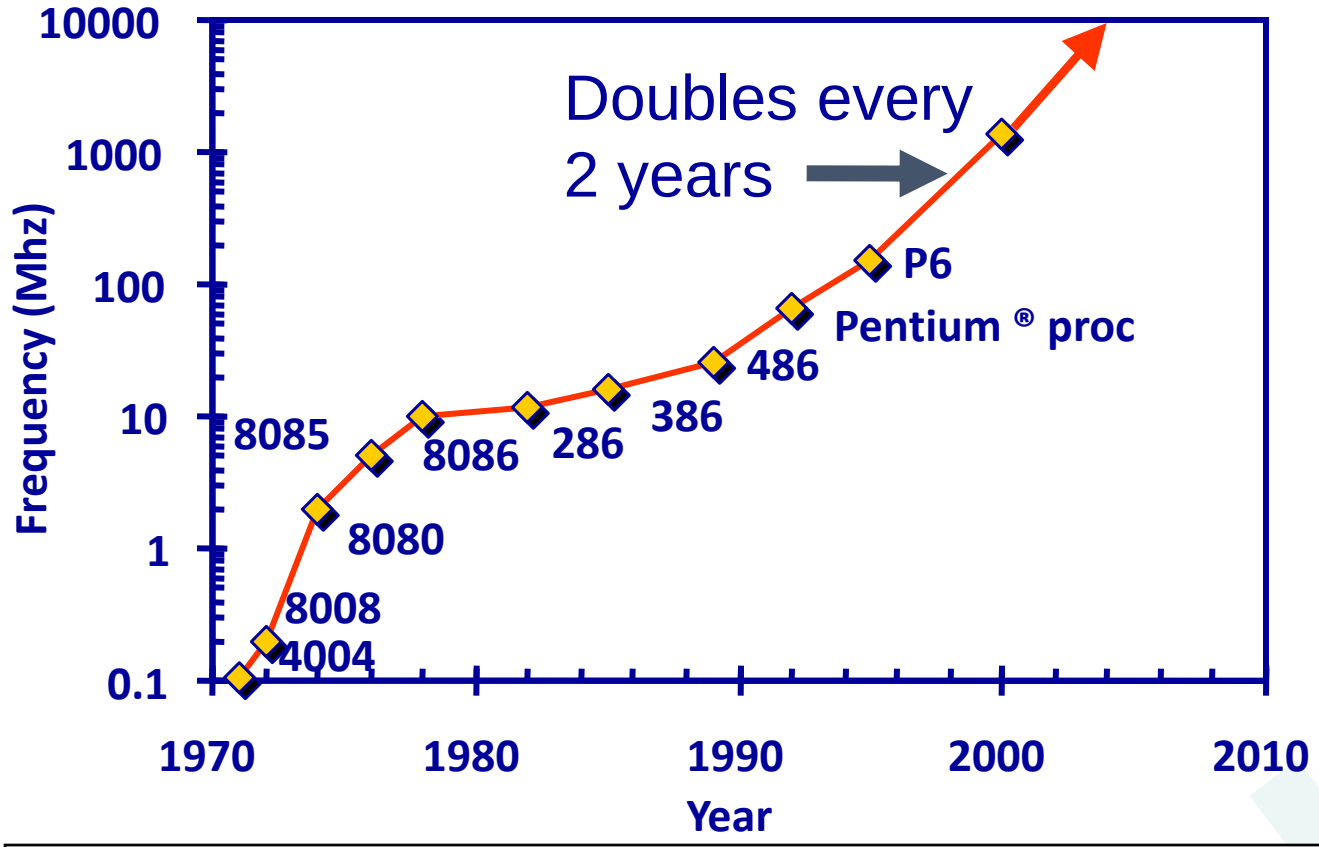
- n-channel
- p-channel



Technology nodes

- Scaling
  - 0.25um,0.18um,90nm,65nm,45nm,32nm, 22nm, 14nm…

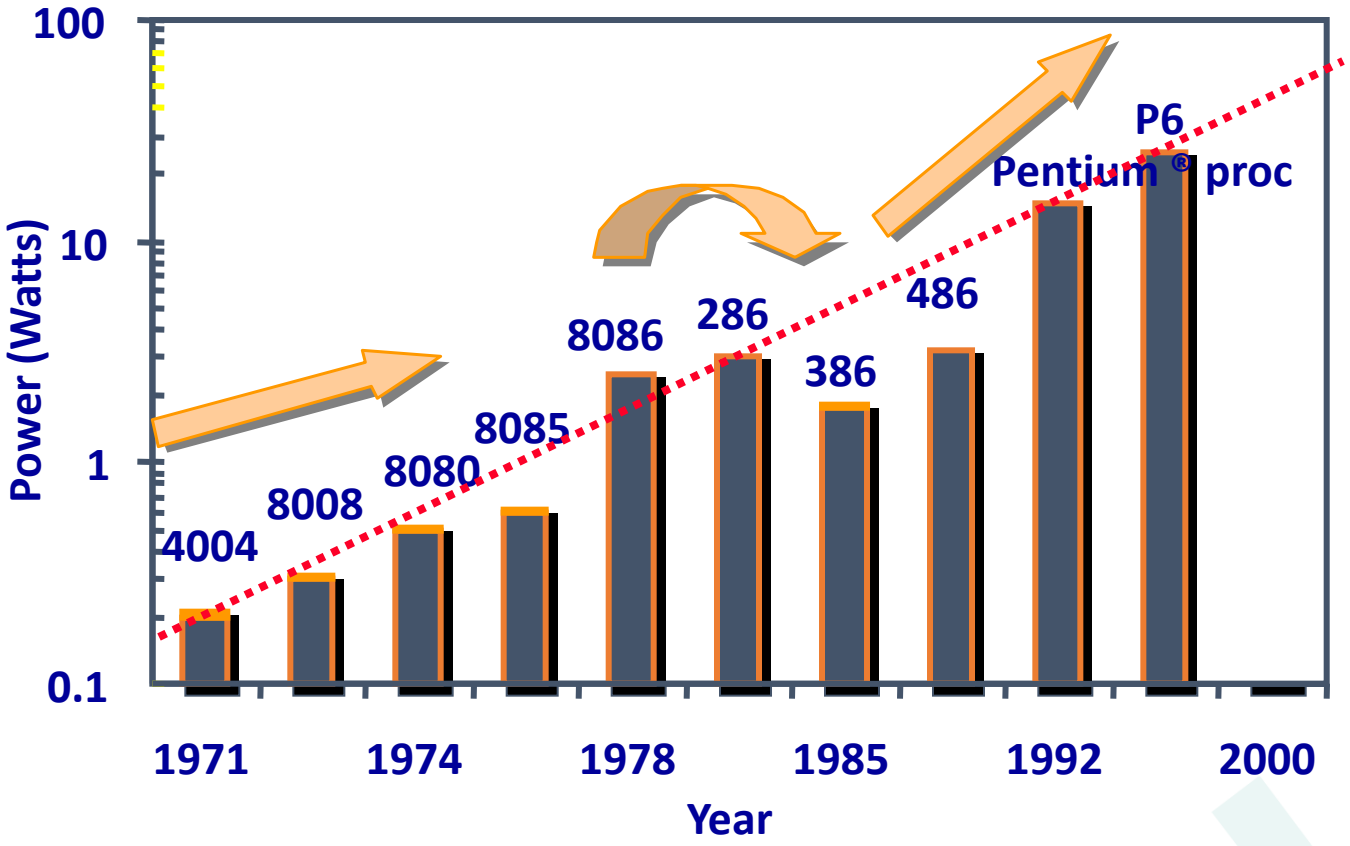
Frequency



Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel

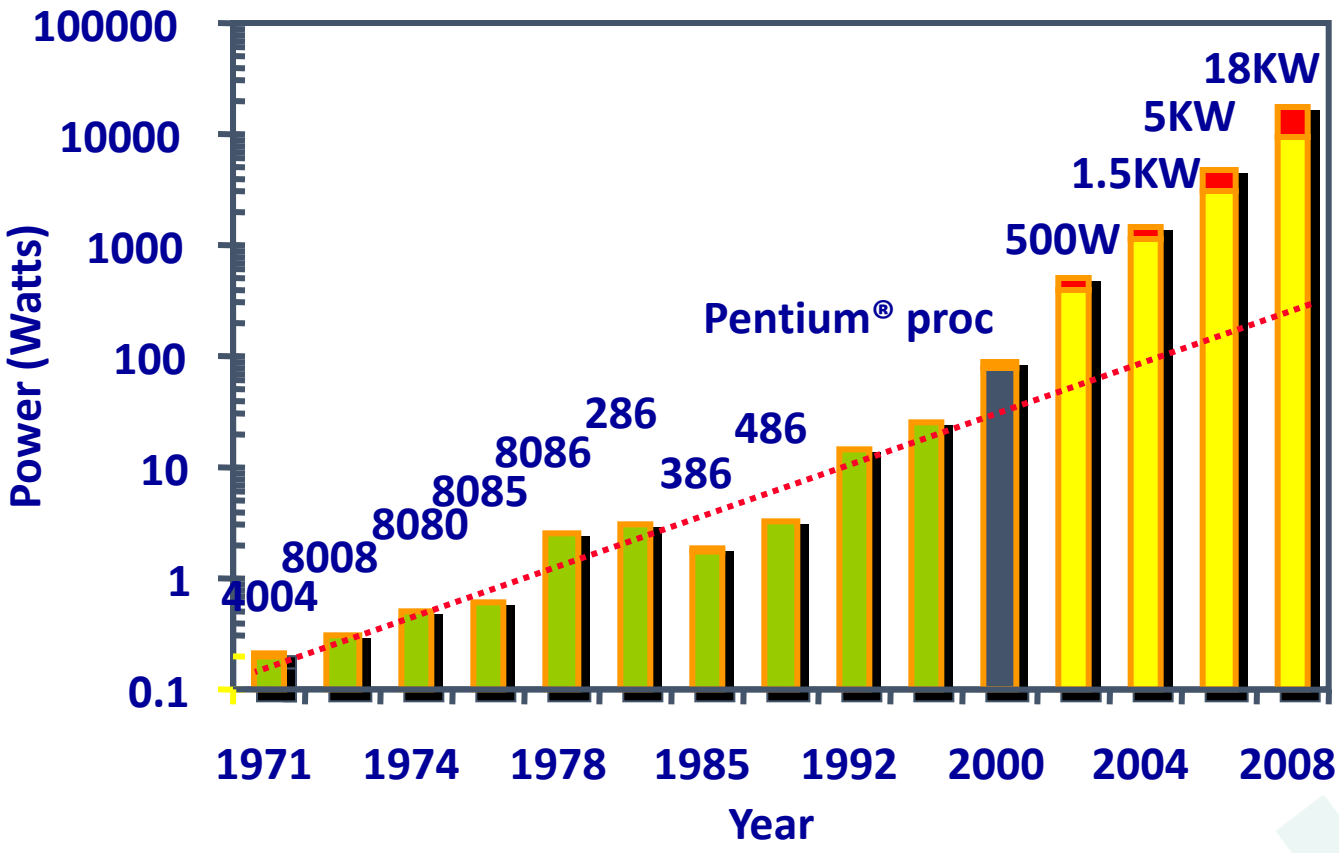
Power Dissipation



Lead Microprocessors power continues to increase

Courtesy, Intel

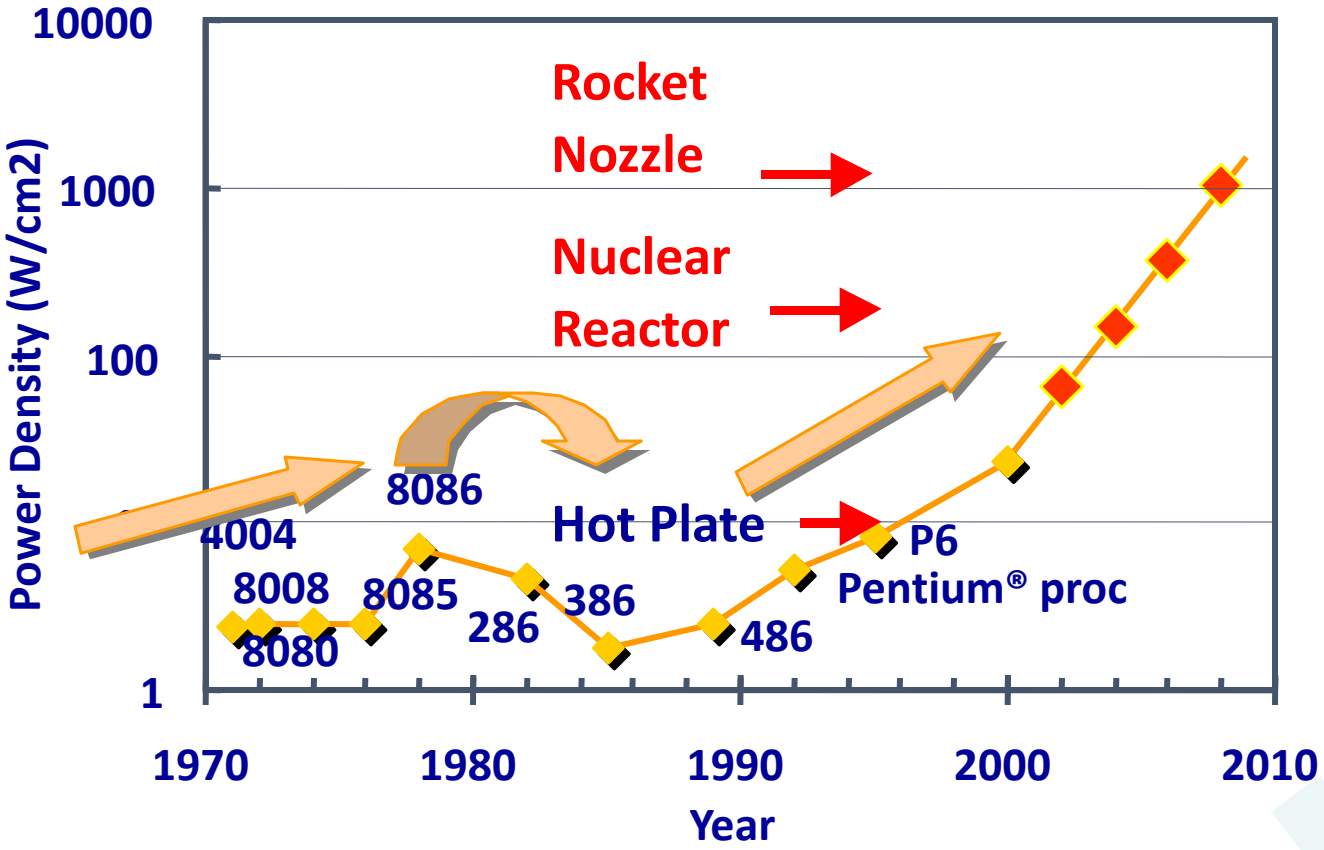
Power will be a major problem



Power delivery and dissipation will be prohibitive

Courtesy, Intel

Power density



Power density too high to keep junctions at low temp

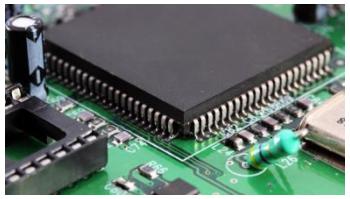
Courtesy, Intel

Current Computing Capabilities

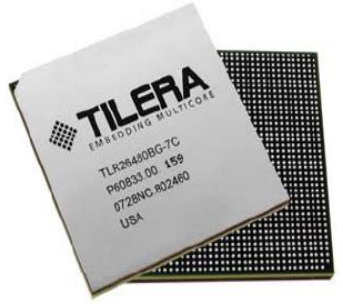
- Intel’s 80-core processor: ~Terra flops
- Over a billion transistors per chip
- 4-5 GHz chip clock

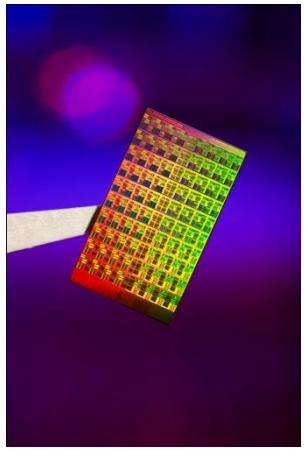
The era of Many-Core systems

- How to keep up with demands on computational power?
  - Can not scale clock frequency
  - Solution: Increase number of cores - parallelism
    - Mass Market production of Intel, AMD dual-core and quad-core CPUs
    - Custom Systems-on-Chip (SoCs)
  - Many Core chips from Tilera for networking, cloud computing and multimedia applications.

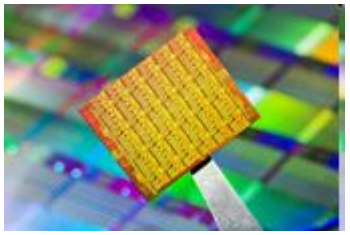


Adapteva's Epiphany





Intel 80 core processor



Single-chip Cloud Computer

'Number of cores will double every 18 months'

- Prof. A. Agarwal, MIT, founder of Tilera Corporation

The era of Many-Core systems

- We are at the early stage of Many-core Processor evolution
  - Many-core is going to be ubiquitous
- Immense possibilities:
  - Server-type performance on handheld devices

Issues and challenges of VLSI today

- High Power dissipation
- Faster operation
- Methodologies to address these issues

Looking ahead

- CMOS technology
  - Stable and well understood process
- Future technologies
  - Nano devices
  - Molecular devices
  - Single electron devices
  - Quantum dots
  - Many more…
- The future is basically yours to invent!