Xilinx ISE 13.2 Simulation Tutorial

This tutorial provides a step-by-step guide to simulating a Verilog description of a 2-input AND gate using Xilinx ISE 11.1 - 11.4.

- 1. Start Xilinx ISE Project Navigator
- 2. Create a new project
 - Click on File, then choose New Project on the drop down menu
 - Enter your project name, in this case the project is called "AND2gate"
 - Choose your project location, this project is stored at "Z:\Projects\AND2gate"
 - Leave the working directory entry blank.
 - Choose HDL as the source type from the Top-Level Source Type menu.
 - Click Next button

ecify project location		
Enter a name, location	ons, and comment for the project	
Name:	AND2gate	
Location:	Z:\Projects\AND2gate	
Working Directory:		
Description:		
Select the type of to	p-level source for the project	
Top-level source typ	e:	
HDL		

3. You will be asked to select the hardware and design flow for this project.

- For *Family*, choose *Spartan3E*For *Device*, choose *XC3S500E*
- For *Package*, choose *FG320*
- For *Speed*, choose -4
- For *Simulator*, choose *ISim (VHDL/Verilog)*
- Click *Next* button

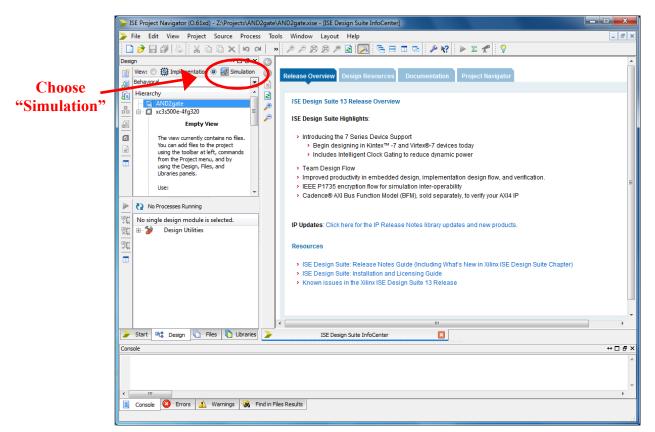
Property Name	Value	
Evaluation Development Board	None Specified	-
Product Category	All	-
Family	Spartan3E	-
Device	XC3S500E	
Package	FG320	-
Speed	-4	-
Top-Level Source Type	HDL	-
Synthesis Tool	XST (VHDL/Verilog)	-
Simulator	ISim (VHDL/Verilog)	-
Preferred Language	Verilog	-
Property Specification in Project File	Store all values	-
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	-

4. A project summary will appear. Click on the *Finish* button.

Project Navigator will creat	a new project with the following specifications.		
Project:			
Project Name:	AND2gate		
Project Path:	Z:\Projects\AND2gate		
Working Direc	tory:		
Description:			
Top Level Sou	rce Type: HDL		
Device:			
Device Family	: Spartan3E		
Device:	xc3s500e		
Package:	fg320		
Speed:	-4		
Top-Level Sou	rce Type: HDL		
Synthesis Too	1: XST (VHDL/Verilog)		
Simulator: IS	im (VHDL/Verilog)		
Preferred Lar	guage: Verilog		
Property Spec	ification in Project File: St	tore all values	
Manual Compil	e Order: false		
VHDL Source A	nalysis Standard: VHDL-93		
	ring, disabled		

5. You now have a project by the name of "AND2gate". Next you want to specify the files in this project are for behavioral simulation.

• Click on Simulation



- 6. Now we want to add a new file to our project.
 - Click on *Project*, choose *New Source*
 - Choose *Verilog Module* as the file type
 - In the *File name*: box enter the desired file name, in this case the file is named "and2gate.v"
 - Click on the *Next* button

Select Source Type Select source type, file name and its location. IP (CORE Generator & Architecture Wizard) Schematic System Generator Project User Document Vierliog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Dackage VHDL Test Bench Embedded Processor	File name: and2gate.v Location: Z:\Projects\AND2gate
More Info	Next Cancel

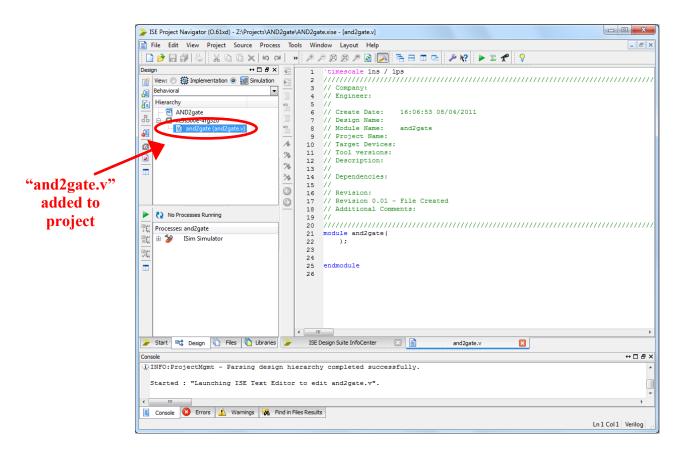
7. You will be asked for the module's port names/types. You can skip this step and click on the Next button.

becify ports f lule name a						
	Port Name	Directio	n	Bus	MSB	LSB
		input	•			
		input	•			
		input	•			
		input	-			
		input	•			
		input	-			
		input	-			
		input	-			
		input	-			
		input	-			
		input	-			

8. A project summary will appear. Click on the *Finish* button.

Summary	
Project Navigator will create a new skeleton source with the following specifications	
Add to Project: Yes Source Directory: Z: \Projects\AND2gate Source Type: Verilog Module Source Name: and2gate.v	
Module name: and2gate Port Definitions:	
More Info	Finish Cancel

9. The "and2gate.v" file has been added to your project.



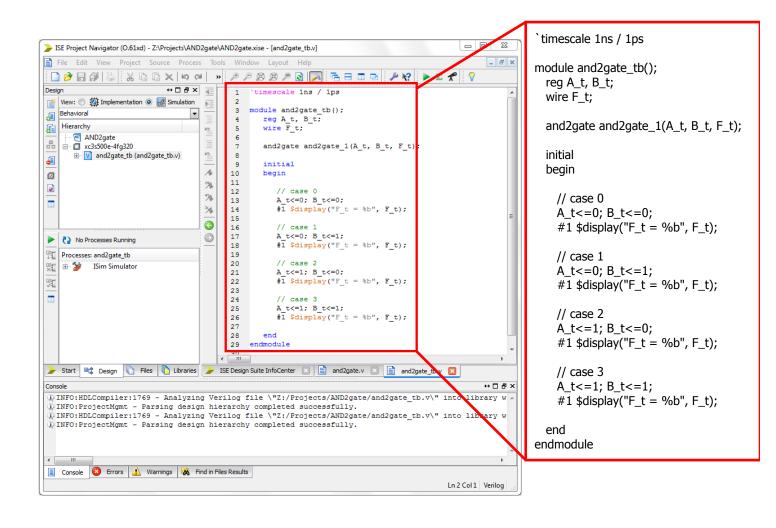
10. Click on the and2gate.v tab to show the file contents. You are now ready to specify the and2gate module's functionality.

> ISE Project Navigator (O.61xd) - Z:\Projects\AND2gate\AND2gate.xise - [and2gate.v]	
File Edit View Project Source Process Tools Window Layout Help	_ <i>8</i> ×
🗋 🌶 🗄 🕼 🐰 🖬 🖬 🗙 🐚 🔍 🛏 🔍 🔺 アクタタク 🖉 🧖 🚰 🖽 🖕 🖋 🕨 🕿 🗶	
Design $\leftrightarrow \Box B \times \blacksquare 1$ `timescale ins / ips	1. · · · · · · · · · · · · · · · · · · ·
Image: Simulation Image: Simulation	
2 // Company:	
de 4 // Engineer:	
6 // Create Date: 16:06:53 08/04/2011	
- 🖾 xc3s500e-4fg320 7 // Design Name:	
and2gate (and2gate.v) 8 // Module Name: and2gate	
g // Project Name:	
11 // Tool versions:	
12 // Description:	
14 // Dependencies:	
3 15 // Revision:	
17 // Revision 0.01 - File Created	🔪 🔪 workspace
No Processes Running	
Tig Processes: and/gate 21 module and/gate (
ISim Simulator 22);	
23 24	
25 endmodule	
Click on	
"and2gate.v"	
tab	
	•
> Start 🗠 Design 🖒 Files 🐧 Libraries > ISE Design Suite InfoCenter 🔝 📄 and2gate.v	
Console	⇔⊡∄×
<pre>INFO:ProjectMgmt - Parsing design hierarchy completed successfully.</pre>	A
Started : "Launching ISE Text Editor to edit and2gate.v".	
Started . Baunching is lext Editor to eart and/gate.v".	
<	
Console 🙆 Errors 🔔 Warnings 🙀 Find in Files Results	
	Ln 1 Col 1 Verilog

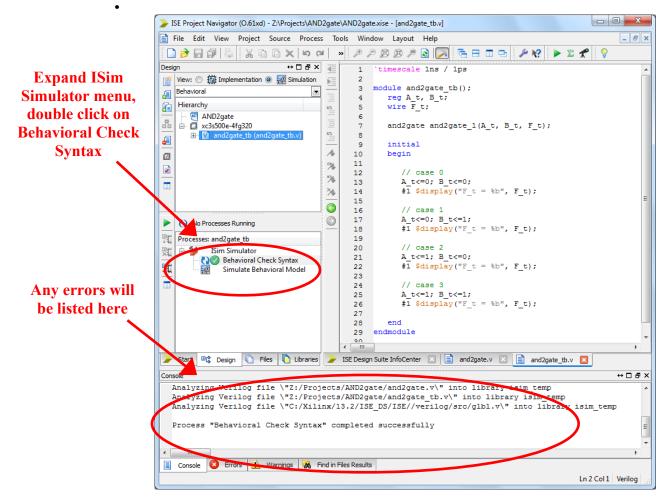
- 11. Notice that the ISE has already entered a comments sections along with a couple of lines of code for us.
 - The line "`timescale 1ns/1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator.
 - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
 - We finish specifying the functionality of the and2gate module as shown below.

> ISE Project Navigator (D.61xd) - Z.\Projects\AND2gate\AND2gate.xise - [and2gate.v]	
File Edit View Project Source Process Tools Window Layout Help	`timescale 1ns / 1ps
Design Image: Provide and Provide A	module and2gate(A, B, F); input A, B; output F; reg F; always @ (A, B) begin F <= A & B; end endmodule
Processes kultiling Processes and2gate	
🛒 🗁 🎾 ISim Simulator	
Start C Design Files Itbraries Itb Design Suite InfoCenter and2pate.v	
Console	
INFO:ProjectMgmt - Parsing design hierarchy completed successfully. INFO:HDLCompiler:1769 - Analyzing Verilog file \"Z:/Projects/AND2gate/and2gate.v\" into library work INFO:ProjectMgmt - Parsing design hierarchy completed successfully. 	
Console Errors 🔔 Warnings 🦝 Find in Files Results	

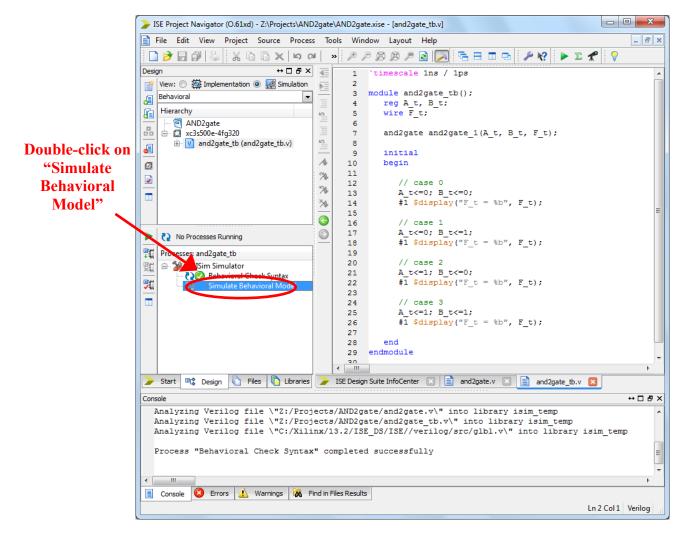
12. We also want to add a test bench and again follow Steps 8 – 11 to add "and2gate_tb.v". Then we add the functionality of the testbench module as shown below.



- 13. After saving both "and2gate.v" and "and2gate_tb.v", we want to check the syntax of both files.
 - Expand the ISim Simulator menu, double click on Behavioral Check Syntax
 - If the syntax was correct, a checkmark appears beside the Check Syntax menu
 - If the syntax was incorrect, the window at the bottom will list the individual errors.



- 14. Now it's time to simulate the design.
 - Double-click on the Simulate Behavioral Model icon



15. The ISim Simulator open in a new windows displaying a waveform and run a default simulation for some number of time units. We can now check the and2gate module's functionality. Further, the \$display statements included in the testbench appear in the lower window.

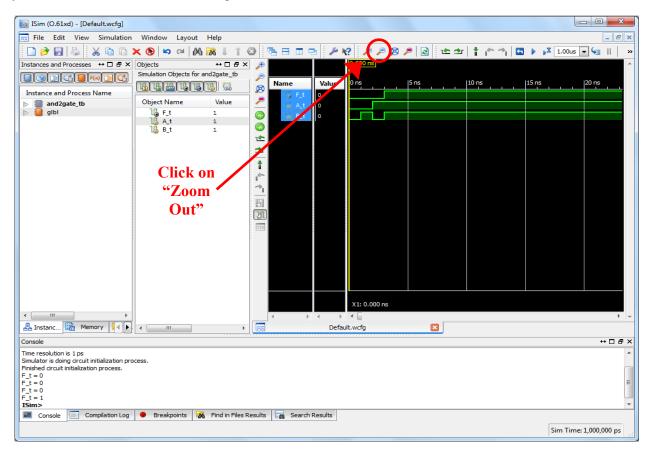
ISim (O.61xd) - [Default.wcfg]										x
File Edit View Simulation	Window Layout	Help							-	a ×
	× 🕲 🗠 🖓			5 i 🖉 K	? 🗦 🗩 🗩	🙉 🏓 🗟 🗄	*** * *		🛙 1.00us 💌 🔙	»
Instances and Processes ↔ □ ×			• • • • •						1,000,000	JS A
	Simulation Objects for									
		16 🔛 🧯	Name	Value	<u></u>	999,996 ps	999,997 ps	999,998 ps	999,999 ps	
Instance and Process Name and2gate_tb	Object Name	Value		1						
	ll F_t	1	L@A_L	1			_	_		
	lla A_t La B_t	1		-						
	1 10 L	-								
	-	. =	br I							
		1	ł							
			h							
		i.								
					X1: 1,000,0	00 ps				
۰ III ا				<	•				E.	• •
🛃 Instanc 📴 Memory 🚺	•	۱	<u>98</u>	Defau	lt.wcfg	×				
Console									↔ 🗆	đΧ
Trace resolution is 1 ps Simulator is doing circuit initialization pro										^
Finished circut initialization process.	ACC20.									
F_t = 0 F_t = 0										=
F_t = 0 F_t = 1										
ISim>										-
Console Compilation Log	🔸 Breakpoints 👔	🔥 Find in Files Resu	lts 🚮 Search	Results						
									Sim Time: 1,000,000	ps

\$display statements appear here

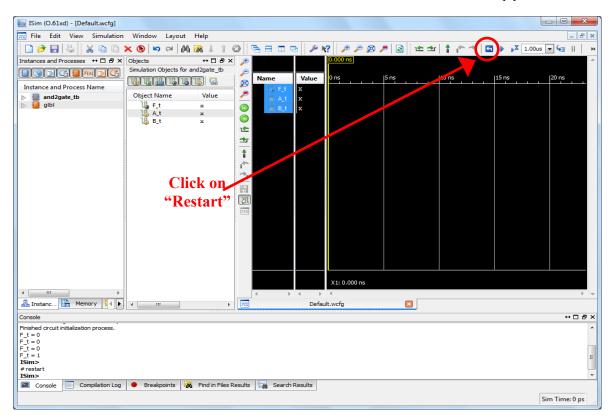
16. To view the beginning of simulation, click on the *Go To Time 0* button.

Click on "Go To Time 0"	ISim (O.61xd) - [Default.wcfg] File Edit View Simulation Instances and Processes ↔ □ ♂ × Instance and Process Name and2gate tb glbl	î 🔊 🖓 🗠 📬 🔗 🗙	× * * * * * * * * * * * * * * * * * * *			: ➔r 甞 i़ t ∽iı 🖸	
	د الله المعاون المعالي المعالي المعالي المعالي	<		X1: 1,000 A b 4 Default.wcfg	1,000 ps		
	Console Time resolution is 1 ps Simulator is doing circuit initialization pro Finished circuit initialization process. F_t = 0 F_t = 0 F_t = 1 JSim> Console Compilation Log	ess. Breakpoints 🦝 Find in File	is Results 📷 Search	1 Results			+ ← 戸 F ×

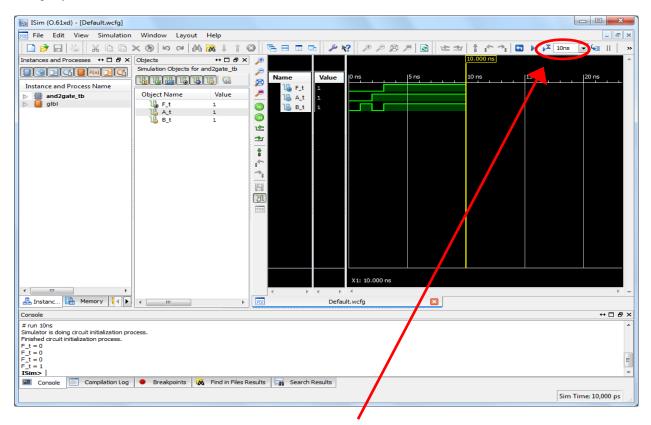
17. We can now see the simulation waveform for the beginning of our simulation. Click on the *Zoom Out* button until you see the waveform shown in the image below.



18. To control the simulation time, we can restart the simulation and simulate for a specific length of time. Either click on the *Restart* button or select *Restart* from the *Simulation* menu. We will now have an empty waveform.



19. To simulate for a specific length of time, enter the desired simulation time and click on the *Run for the time specified in the toolbar button*. In our case, we want to simulate for 10 ns.



Enter the simulation time and click on "Run for..."