PCI, DMA, Interrupt

For UMass Lowell 16.480/552

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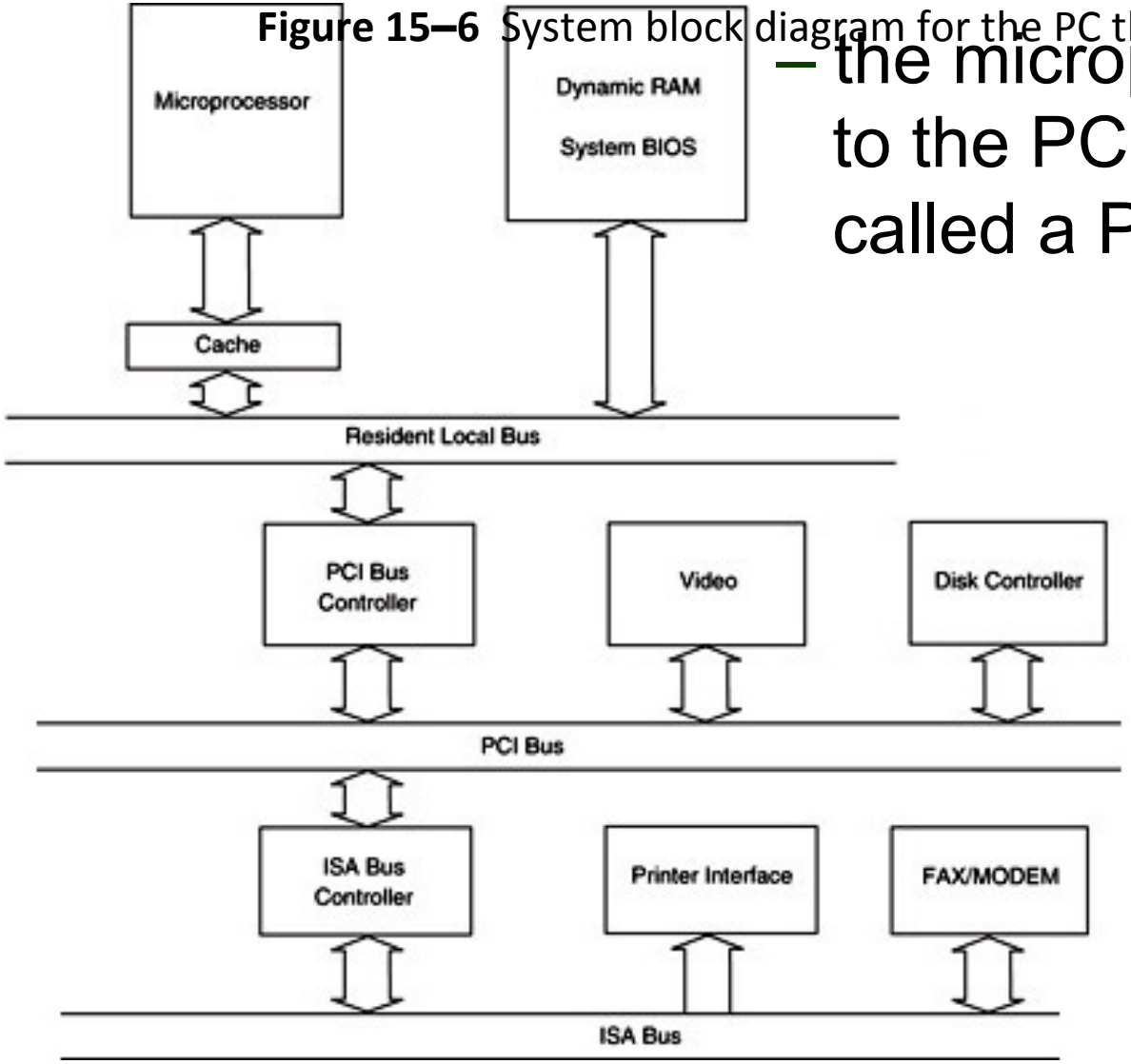
Peripheral Component Interconnect

15–2 PERIPHERAL COMPONENT INTERCONNECT (PCI) BUS

- PCI (**peripheral component interconnect**) is virtually the only bus found in new systems.
  - ISA still exists by special order for older cards
- PCI has replaced the VESA local bus.
- PCI has plug-and-play characteristics and ability to function with a 64-bit data bus.

- A PCI interface contains registers, located in a small memory device containing information about the board.
  - this allows PC to automatically configure the card
  - this provides plug-and-play characteristics to the ISA bus, or any other bus
- Called plug-and-play (PnP), it is the reason PCI has become so popular.
- Figure 15–6 shows the system structure for the PCI bus in a PC system.

Figure 15–6 System block diagram for the PC that contains a PCI bus.



- the microprocessor connects to the PCI bus through an IC called a PCI bridge
  - virtually any processor can interface to PCI with a bridge
  - The resident local bus is often called a front side bus

Another View of a Typical PCI system

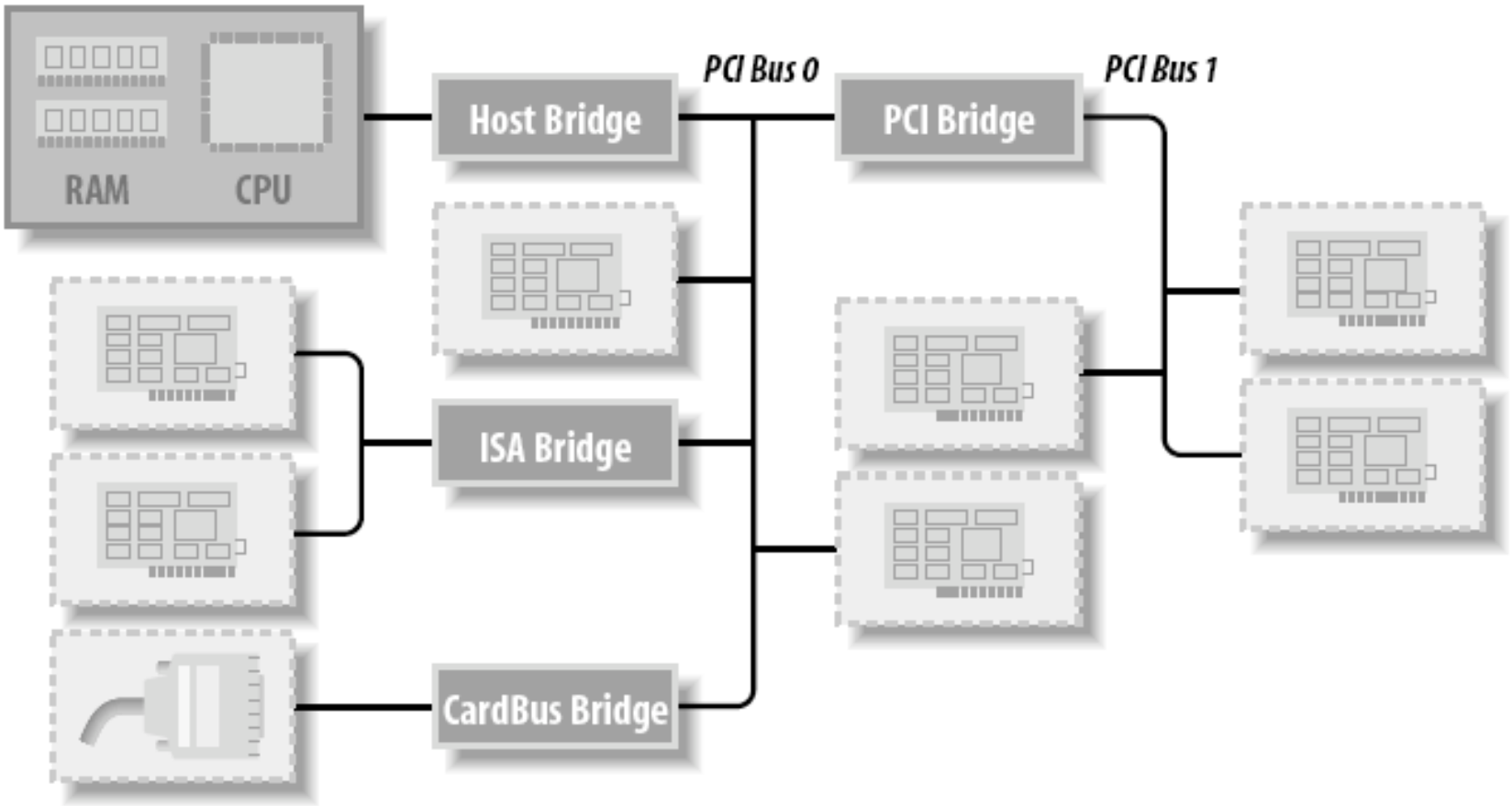
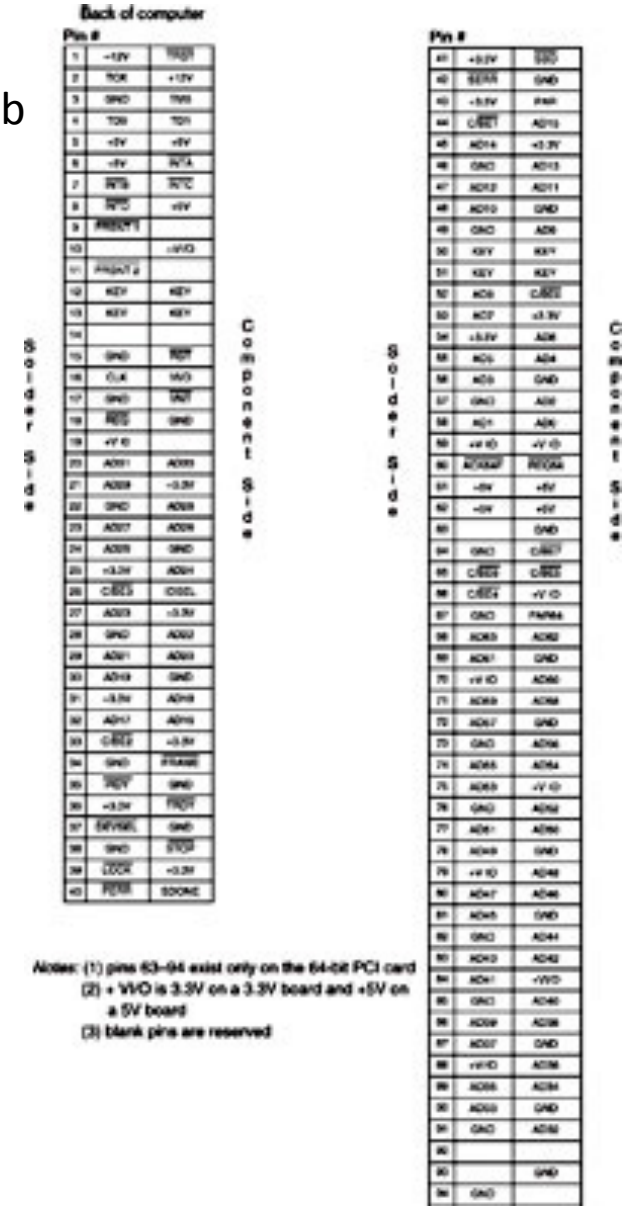


Figure source: The Linux Device Driver, 3rd Ed.

The PCI Bus Pin-Out

- PCI functions with a 32- or 64-bit data bus and a full 32-bit address bus.
  - address and data buses, labeled AD_0–AD_{63} are multiplexed to reduce size of the edge connector
- A 32-bit card has connections 1 through 62, the 64-bit card has all 94 connections.
- The 64-bit card can accommodate a 64-bit address if required at some future point.
- Figure 15–7 shows the PCI bus pin-out.

Figure 15–7 The pin-out of the PCI b

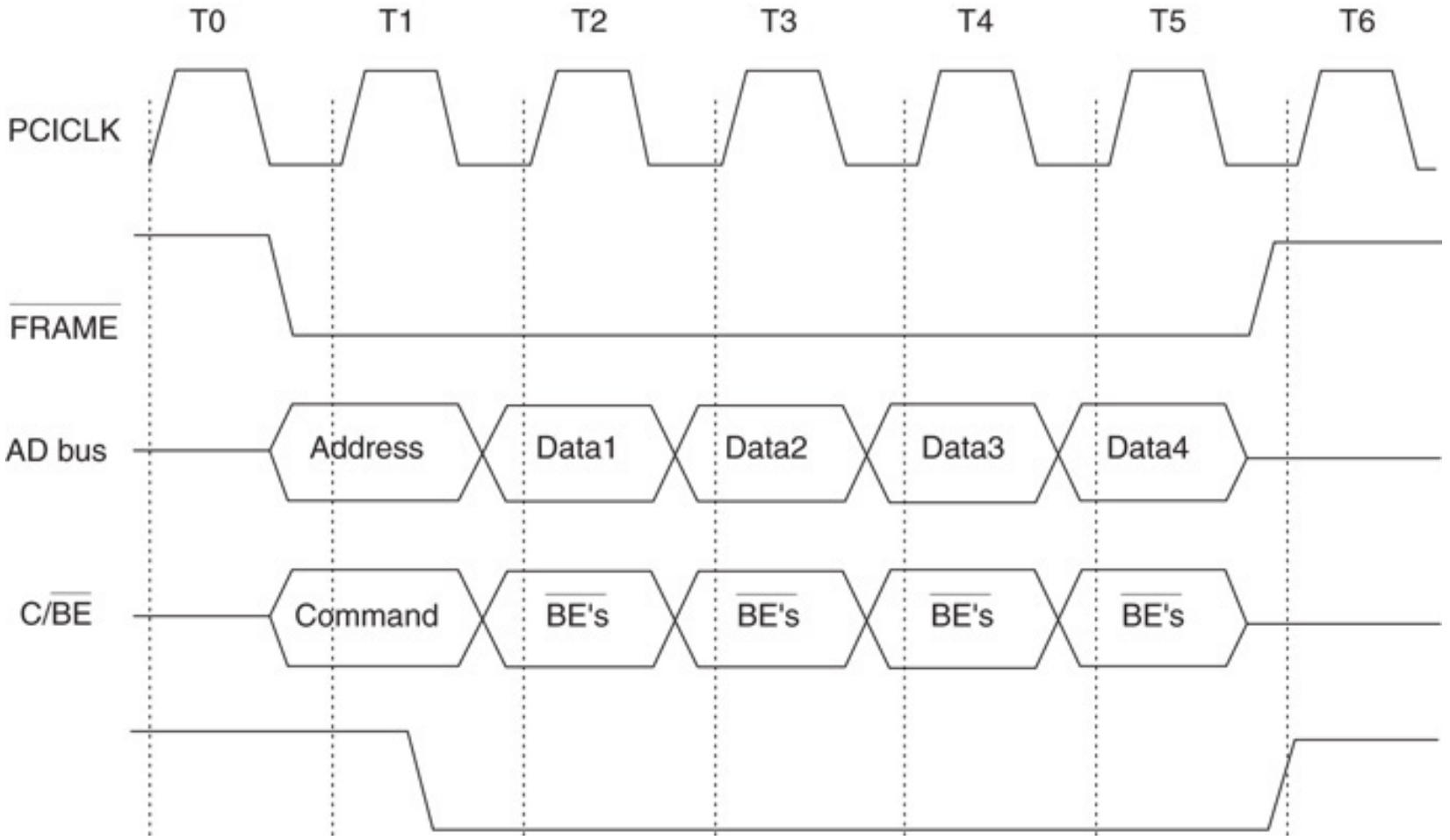


- PCI is most often used for I./O interface to the microprocessor
- memory could be interfaced, but with a Pentium, would operate at 33 MHz, half the speed of the Pentium resident local
- PCI 2.1 operates at 66 MHz, and 33 MHz for older interface cards
- P4 systems use 200 MHz bus speed (often listed as 800 MHz)

The PCI Address/Data Connections

- The PCI address appears on AD_0–AD_{31} and is multiplexed with data.
  - some systems have a 64-bit data bus using AD_{32}–AD_{63} for data transfer only
  - these pins can be used for extending the address to 64 bits
- Fig15–8 shows the PCI bus timing diagram
  - which shows the address multiplexed with data and control signals used for multiplexing

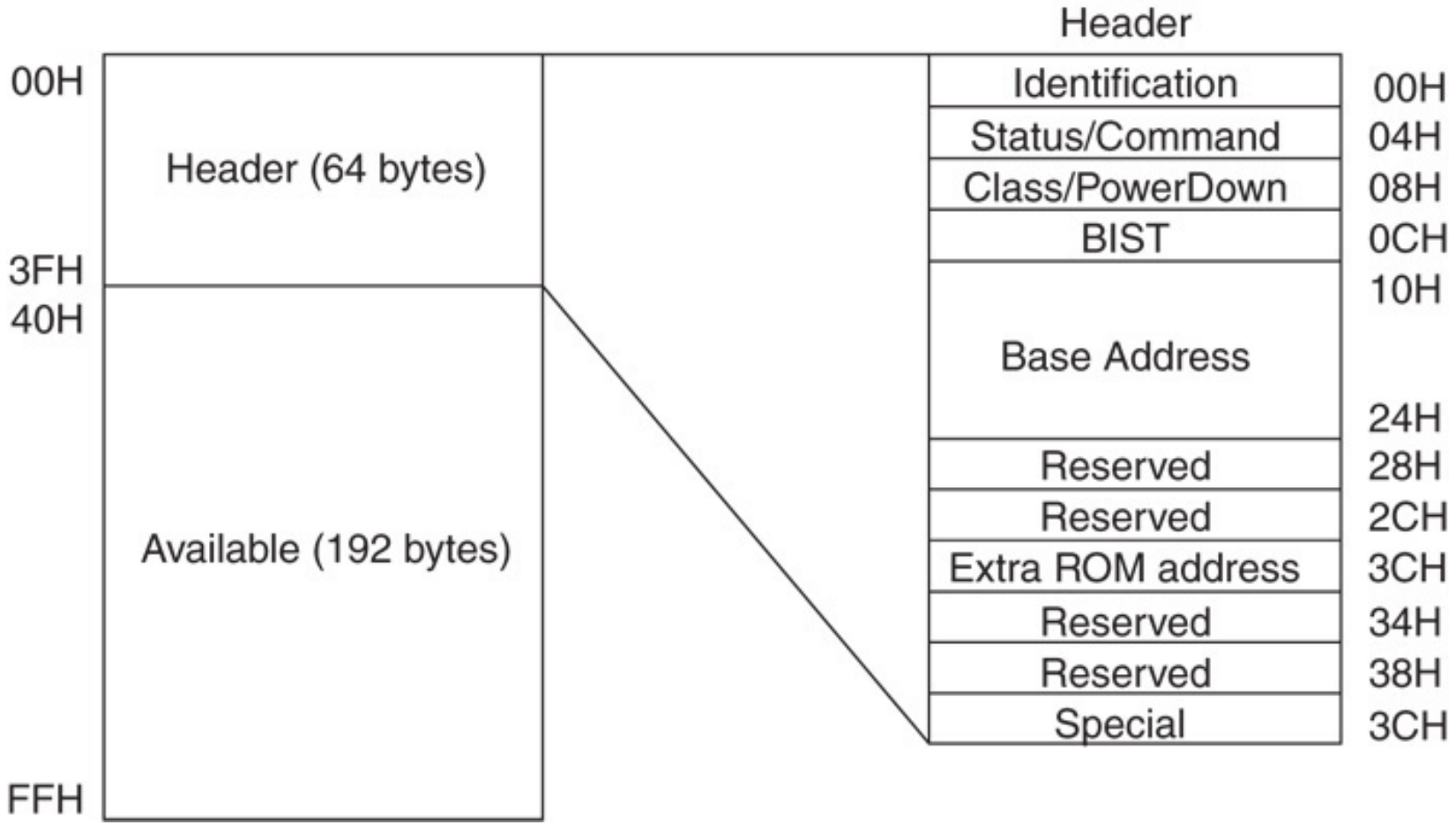
Figure 15–8 The basic burst mode timing for the PCI bus system. Note that this transfers either four 32-bit numbers (32-bit PCI) or four 64-bit numbers (64-bit PCI).



Configuration Space

- PCI contains a 256-byte memory to allow the PC to interrogate the PCI interface.
  - this feature allows the system to automatically configure itself for the PCI plug-board
  - Microsoft calls this plug-and-play (PnP)
- The first 64 bytes contain information about the PCI interface.
- The first 32-bit doubleword contains the unit ID code and the vendor ID code.
- Fig15–9 shows the configuration memory.

Figure 15–9 The contents of the configuration memory on a PCI expansion board.



A more detailed view of the PCI configuration space (first 64B)

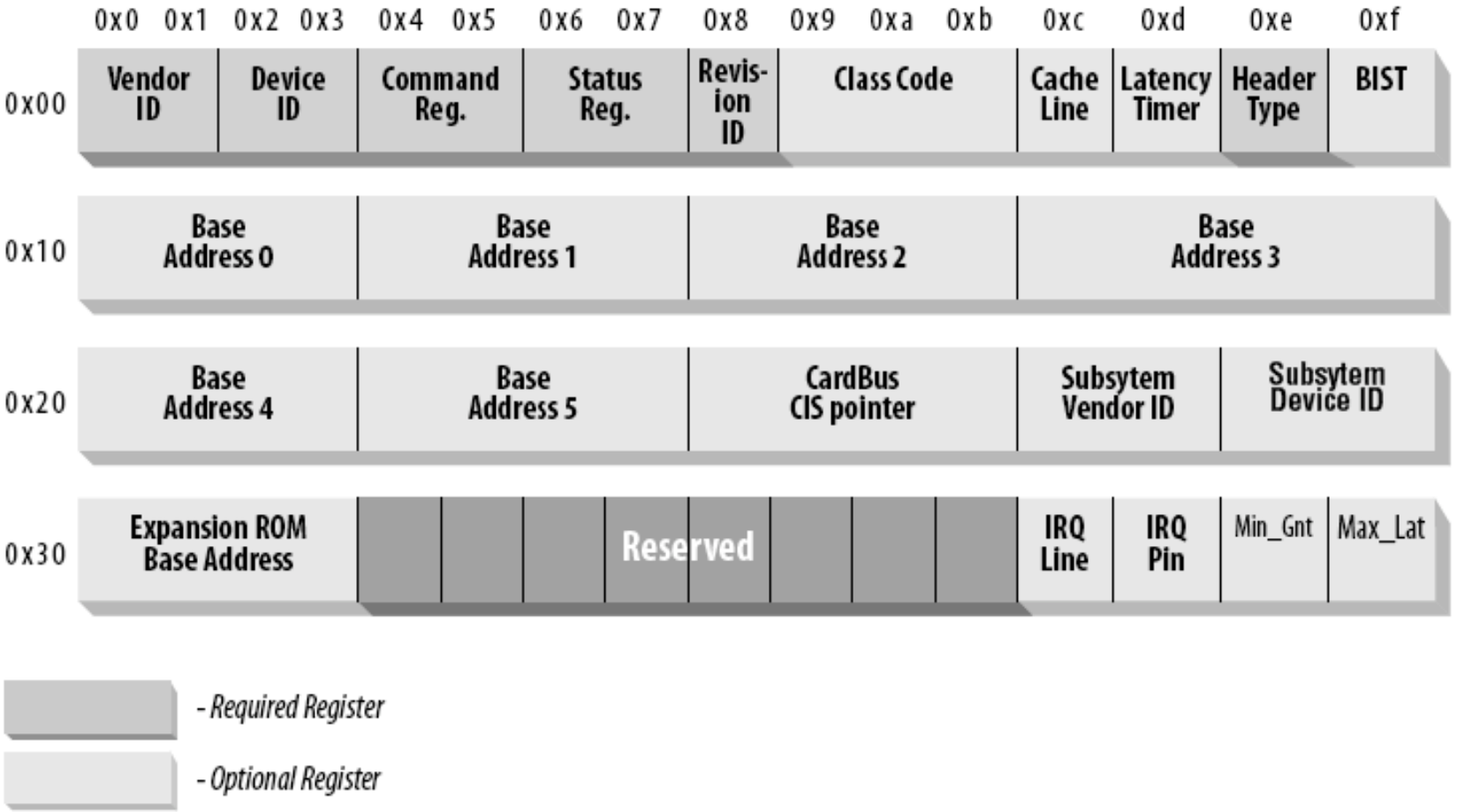


Figure source: The Linux Device Driver, 3rd Ed. (fig. 12-2)

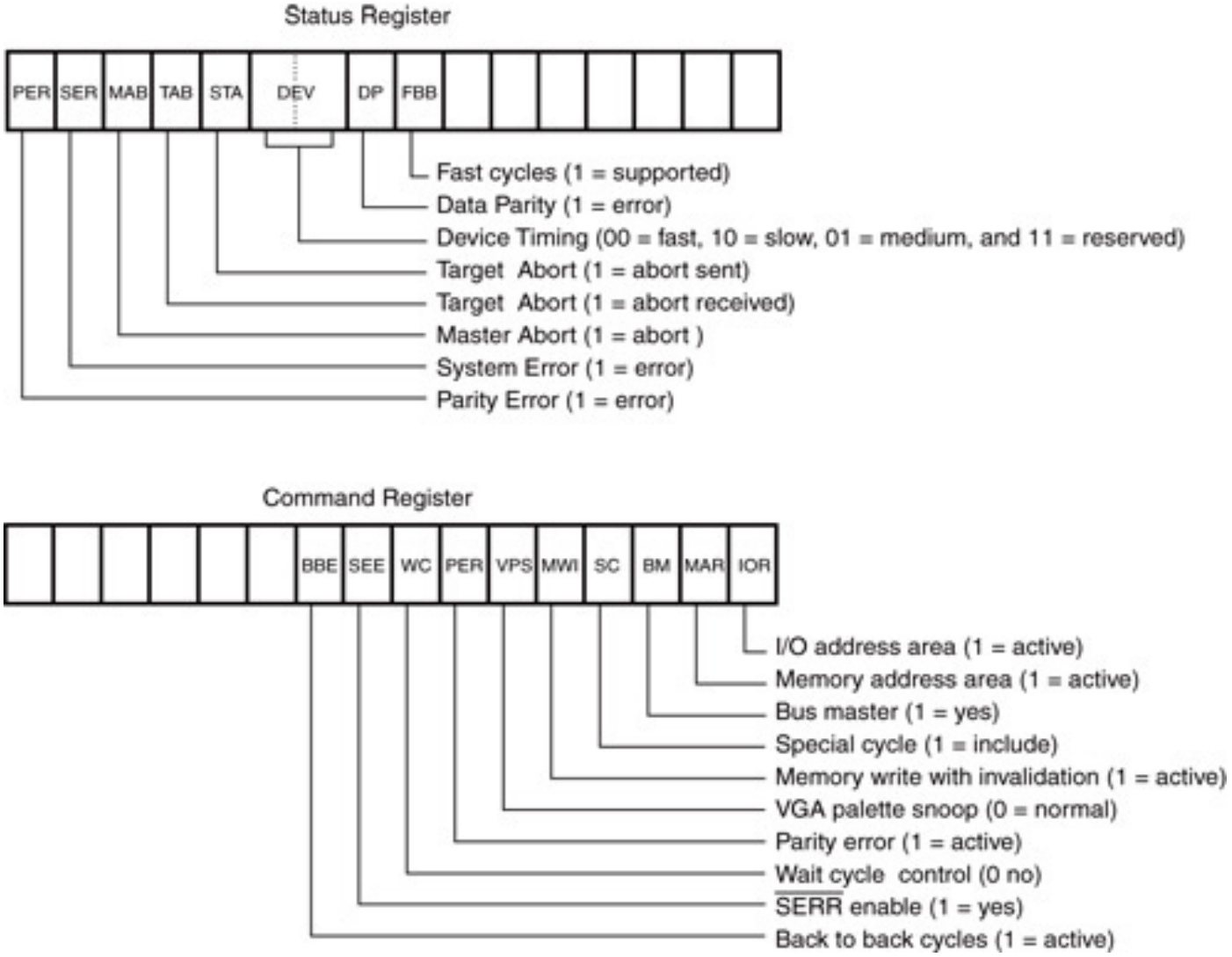
- Unit ID code is a 16-bit number (D_{31}–D_{16}).
  - a number between 0000H & FFFEH to identify the unit if it is installed
  - FFFFH if the unit is not installed
- The class code is found in bits D_{31}–D_{16} of configuration memory at location 08H.
  - class codes identify the PCI interface class
  - bits D_{15}–D_0 are defined by the manufacturer
- Current class codes are listed in Table 15–5 and are assigned by the PCI SIG.

What PCI devices Do We Have? A Linux View

- Demos (/sbin/lspci -s 02:00 -x –vv)
  - lspci command
  - device number
  - detailed info about a PCI device
  - configuration space of the PCI device
    - vendor, class
    - base address

- The base address space consists of a base address for the memory, a second for the I/O space, and a third for the expansion ROM.
- Though Intel microprocessors use a 16-bit I/O address, there is room for expanding to 32 bits addressing.
- The status word is loaded in bits D_{31}–D_{16} of location 04H of the configuration memory.
  - the command is at bits D_{15}–D_0 of 04H
- Fig 15–10 shows the status & command registers.

Figure 15–10 The contents of the status and control words in the configuration



BIOS for PCI

- Most modern PCs have an extension to the normal system BIOS that supports PCI bus.
  - these systems access PCI at interrupt vector 1AH
- Table 15–6 lists functions available through the DOS INT 1AH instruction with AH = 0B1H for the PCI.
  - Example 15–5 (next slide) shows how the BIOS is used to determine whether the PCI bus extension available.
- The BIOS and/or OS (e.g. Linux) perform configuration transactions with every PCI device
  - allocate safe space for each address region it offers
  - map memory or I/O regions to the processor's address space

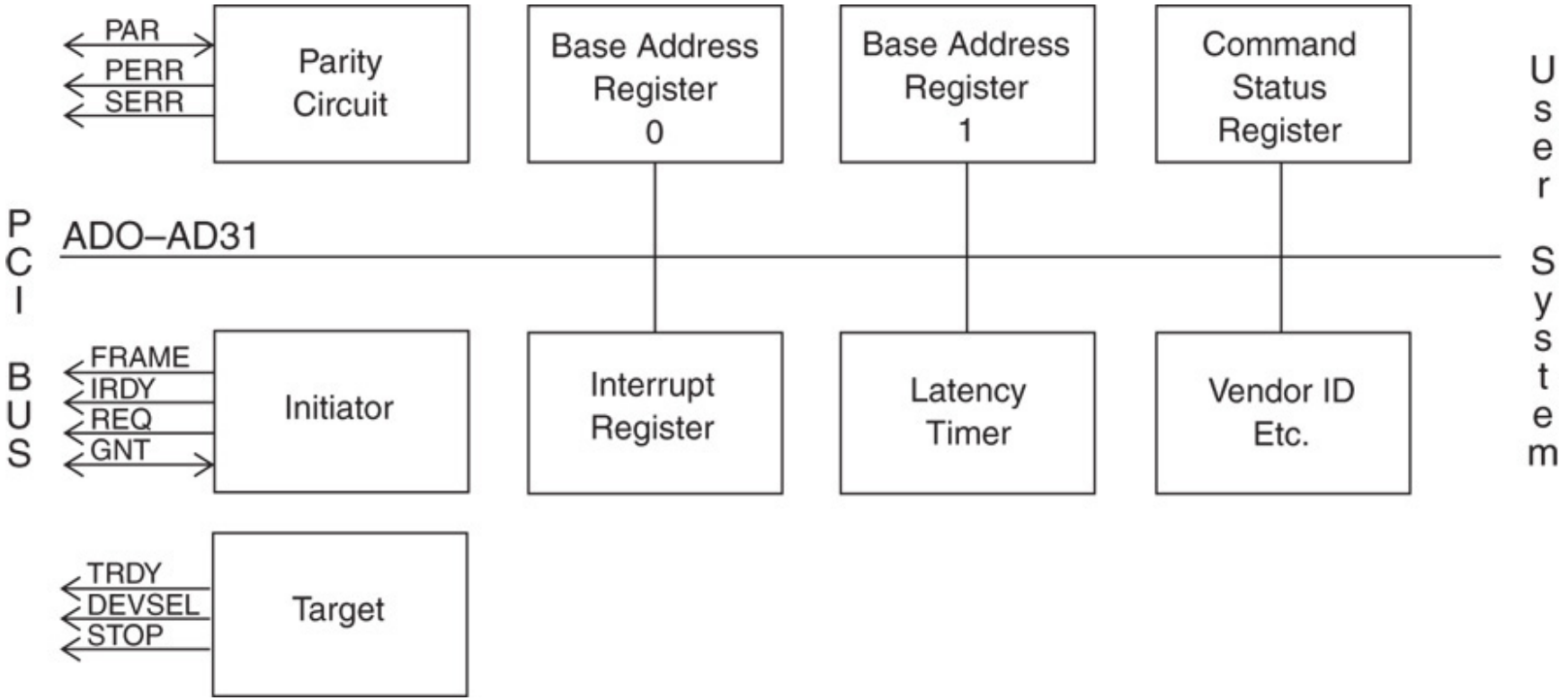
Example 15-5: BIOS PCI Functions

```
.MODEL SMALL
.DATA
      MES1    DB  “PCI BUS IS PRESENT$”
      MES2    DB  “PCI BUS IS NOT FOUND$”
.CODE
.STARTUP
      MOV AH, 0B1H          ; access PCI BIOS
      MOV AL, 1
      INT  1AH
      MOV DX, OFFSET MSE2
      .IF CARRY?            ;  if PCI is present
            MOV DX, OFFSET MSE1
      .ENDIF
      MOV AH, 9             ; display MES1 or MES2
      INT 21H
      .EXIT
END
```

PCl Interface

- If a PCI interface is constructed, a PCI controller is often used because of the complexity of this interface.
- The basic structure of the PCI interface is illustrated in Figure 15–11.
  - the diagram illustrates required components for a functioning PCI interface
- Registers, Parity Block, Initiator, Target, and Vendor ID EPROM are required components of any PCI interface.

Figure 15–11 The block diagram of the PCI interface.



PCI Express Bus

- The PCI Express transfers data in serial at 2.5 GHz to legacy PCI applications,
  - 250 MBps to 8 GBps for PCI Express interfaces
  - standard PCI delivers data at about 133 MBps
- Each serial connection on the PCI Express bus is called a **lane**.
  - e.g. slots on the main board are single lane slots with a total transfer speed of 1 GBps (4 lanes)
- E.g. a PCI Express video card connector has 16 lanes with a transfer speed of 4 GBps.

- The standard allows up to 32 lanes.
  - at present the widest is the 16 lanes video card
- Most main boards contain four single lane slots for peripherals and one 16 lane slot for the video card.
  - a few newer boards contain two 16 lane slots
- PCI Express 2 bus was released in late 2007.
  - transfer speed from 250 MBps to 500 MBps, twice that of the PCI Express
- PCI is replacing most current video cards on the AGP port with the PCI Express bus.

- This technology allows manufacturers to use less space on the main board and reduce the cost of manufacturing a main board.
  - connectors are smaller, which also reduces cost
- Software used with PCI Express remains the same as used with the PCI bus.
  - new programs are not needed to develop drivers
- The connector is a 36-pin connector as illustrated in Figure 15–12.

- the pin-out for the single lane connector, appears in Table 15–7
- signaling on the PCI Express bus uses 3.3 V with differential signals degrees out of phase
- the lane is constructed from a pair of data pipes, one for input data and one for output data

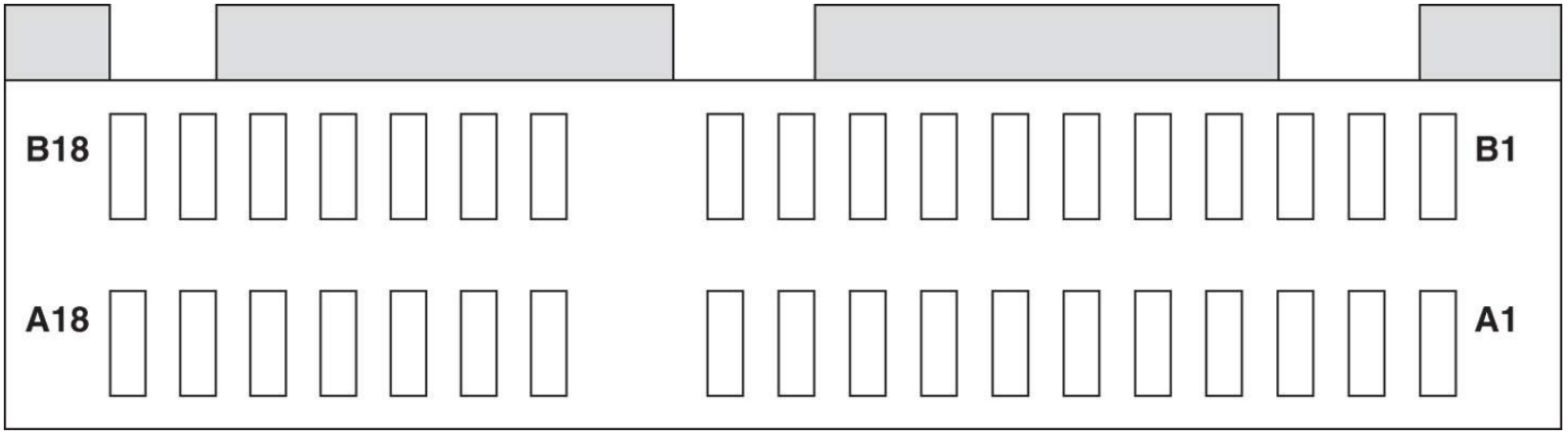


Figure 15–12 The single lane PCI Express connector.