University of Toronto, Department of Electrical and Computer Engineering

ECE 1387 - CAD for Digital Circuit Synthesis and Layout

September 2015

Instructor: Jason Anderson
Phone: 416-946-7285
Office: EA 314 (Engineering Annex)
E-Mail: janders@ece.toronto.edu
Instructor's Web: http://janders.eecg.toronto.edu

Office Hours: After class or by appointment or swing by my office

Course Web: **https://piazza.com/utoronto.ca/fall2015/ece1387/home**

Pre-requisites: ECE 1388 (VLSI Design Methodology), or ECE 451 (VLSI Systems), or CSC 2410 (Algorithms in Graph Theory), or Permission of instructor. **Programming skills in C/C++**, including data structures.

Lecture: Fridays 5:00-7:00 PM in room GB 119 (Galbraith Building)

Papers/Readings: Available in PDF on course website.

Evaluation:				
	Assignments	50% (3 or 4)	Paper	25%
	Exercises	15% (3)	Quizzes (2 or 3)	10%

Assignments: Programming implementations of CAD problems such as placement, routing, and technology mapping using optimization strategies such as simulated annealing, dynamic programming, integer linear programming (ILP), and branch and bound, and illustrated using computer graphics.

Exercises: Hands-on experience with CAD tools such as ABC (UC Berkeley), VPR (Auto Place & Route), and hMetis (Partitioning).

The Paper: A critical assessment of work in a subset of the field (chosen in consultation with the instructor) based on 3 to 4 papers.

Quizzes: Short 15 minute quizzes, at the end of selected lectures (to be announced in advance), on topics presented in preceeding lectures.

TENTATIVE Lecture and Assignment Schedule – Fall 2015

#	Date of Friday Lecture	Lecture Topic	Assignment/ Exercise Handed Out	Assignment/ Exercise Due
1	Sept 11	Introduction, Overview		
2	Sept 18	Routing	Assignment 1 – Routing	
3	Sept 25	Timing-Driven Routing		
4	Oct 2	Placement		
5	Oct 9	Placement (Analytical Techniques)	Assignment 2 – Analytical Placement	Assignment 1
6	Oct 16	Placement (Simulated Annealing)	Exercise 1 – VPR placement and routing	
7	Oct 23	Partitioning or SAT Solvers (Branch and Bound)	Assignment 3 – B&B as applied to partitioning or Boolean SAT	Assignment 2
8	Oct 30	Timing Analysis and Slack Allocation		Exercise 1
	Nov 6	**NO CLASS**		
9	Nov 13	Partitioning (FM/Multi-Level: hMetis)	Exercise 2 – Partitioning Using hMetis or FM	Assignment 3
10	Nov 20	Technology Mapping / Logic Synthesis (Dynamic Programming)	Exercise 3 – Technology Mapping Using Dynamic Prog in ABC (UC Berkeley)	Exercise 2
11	Nov 27	High-Level Synthesis 1		
12	Dec 4	High-Level Synthesis 2	Assignment 4 – LegUp High-Level Synthesis	Exercise 3
	Dec 18			Assignment 4
	Dec 18			Paper

NOTE: You must consult with the instructor on your paper topic by mid-November.