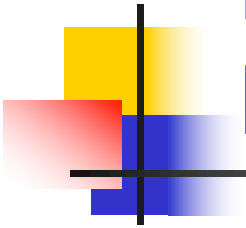
16.480/552

Intel 80386DX and its Memory Interfaces

Hardware Organization of the Physical Memory Space



- Figure 9.20
- Four independent byte-wide banks
  - What is the address range of a bank?
- Address bits are applied to all banks in parallel
- BE bits enable individual bank
- Accessing a byte, word, double word - Figure 9.21(a)-(d)
- Misaligned double-word transfer - Figure 9.24

Alignment

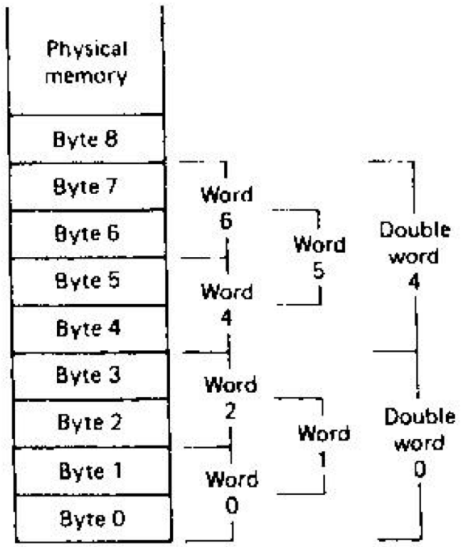


Figure 9.22 Examples of aligned data words and double words.

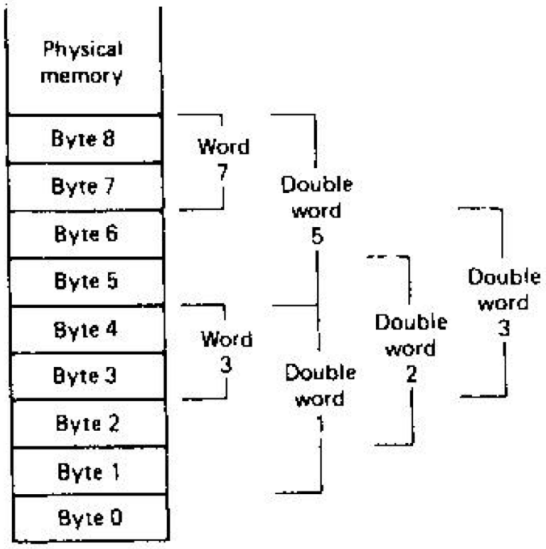


Figure 9.23 Examples of misaligned data words and double words.

Transfer of Misaligned Double-Word

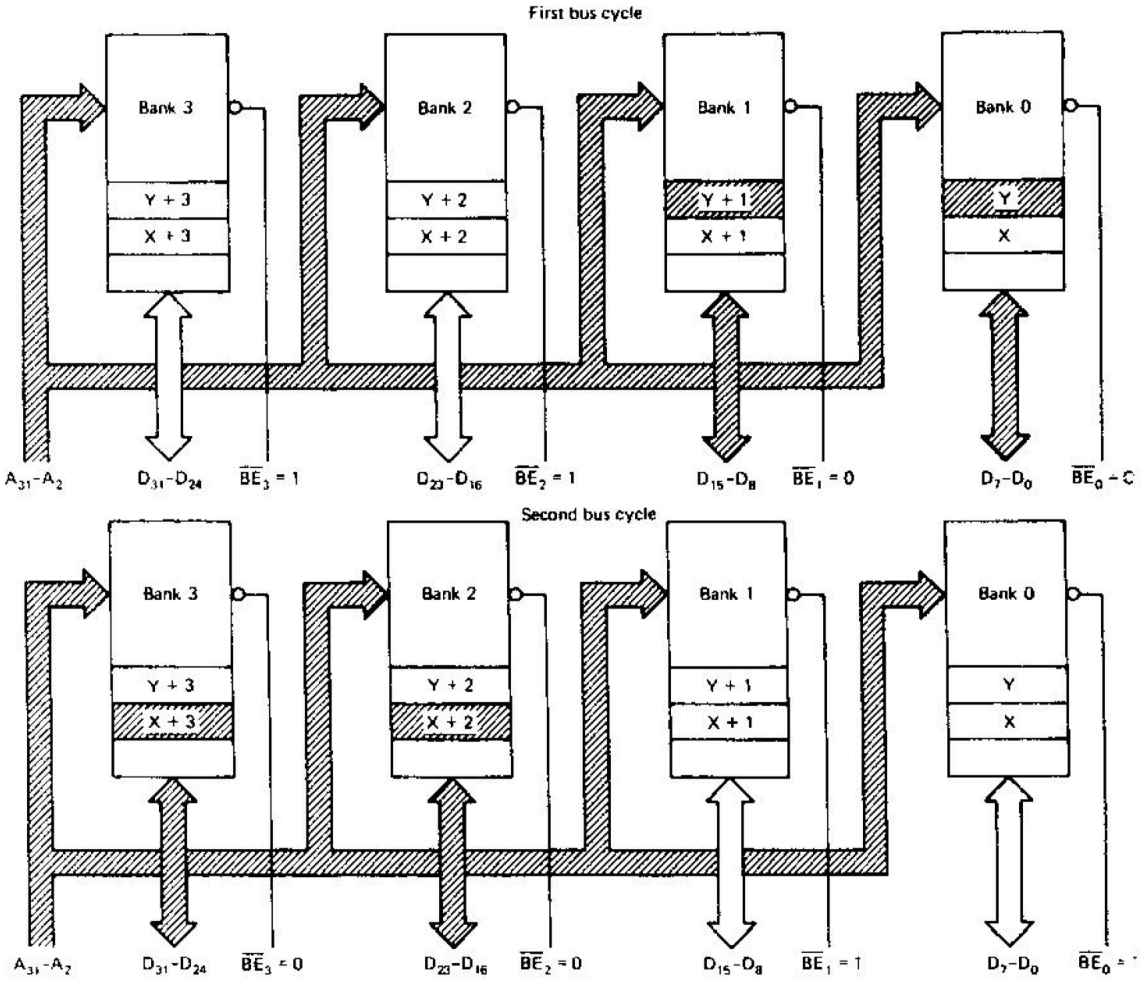


Figure 9.24 Misaligned double-word data transfer.

Memory Interface Block Diagram

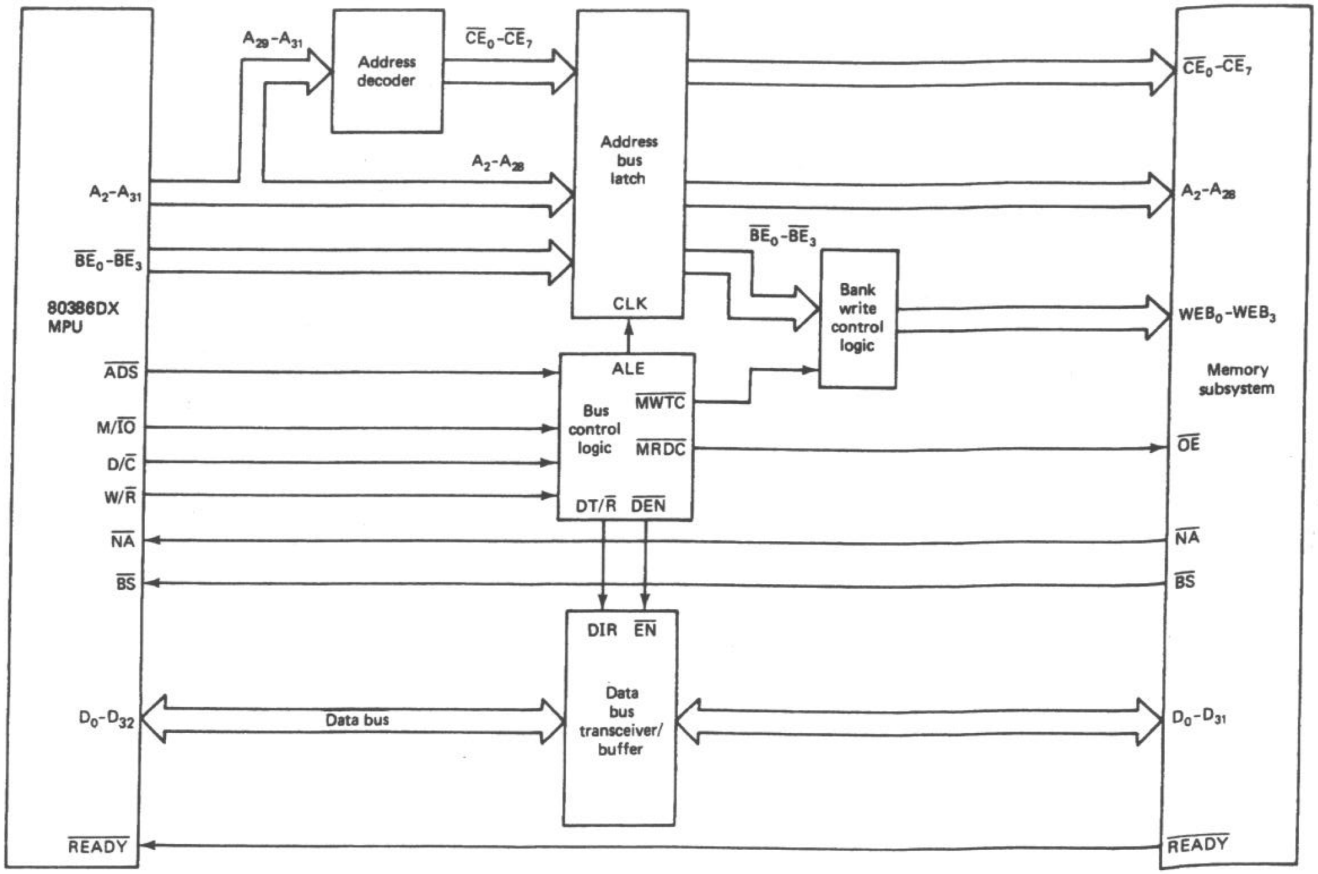
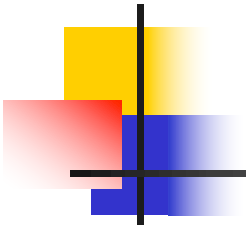
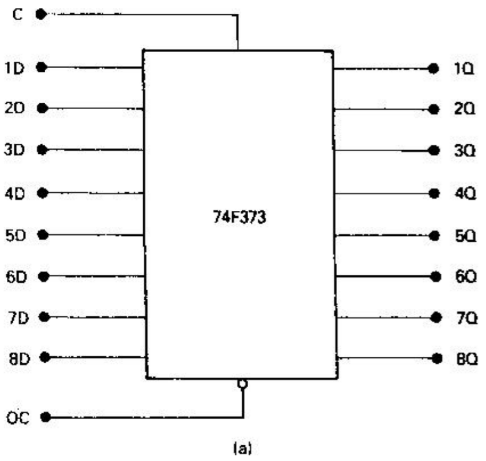


Figure 9.25 Memory interface block diagram.

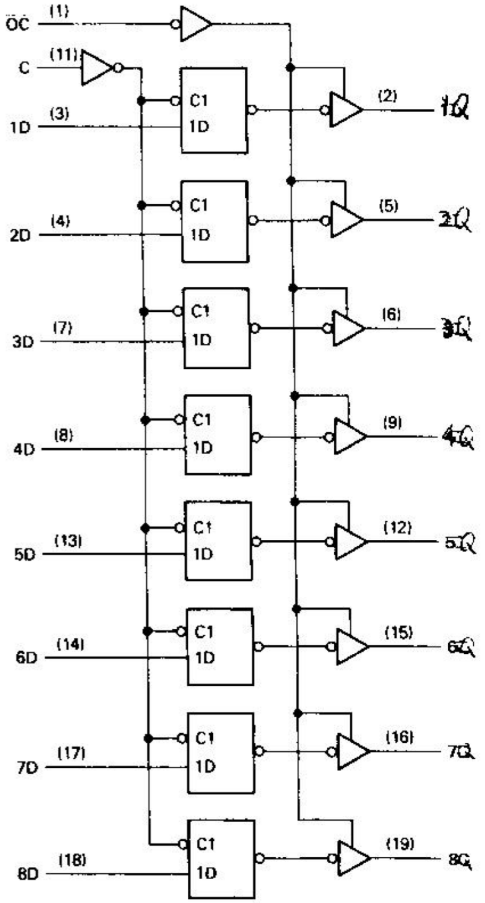


Memory Interface Circuitry

- Figure 9.25
  - Bus control logic
  - Address bus latches (Fig 9.26, 9.27)
  - Address decoder
  - Bank write control logic
  - Data bus transceiver/buffer (Fig 9.30, 9.31)



(a)



(b)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

(c)

Figure 9.26 (a) Block diagram of an octal D-type latch. (b) Circuit diagram of the 74F373. (Courtesy of Texas Instruments Incorporated) (c) Operation of the 74F373. (Courtesy of Texas Instruments Incorporated)

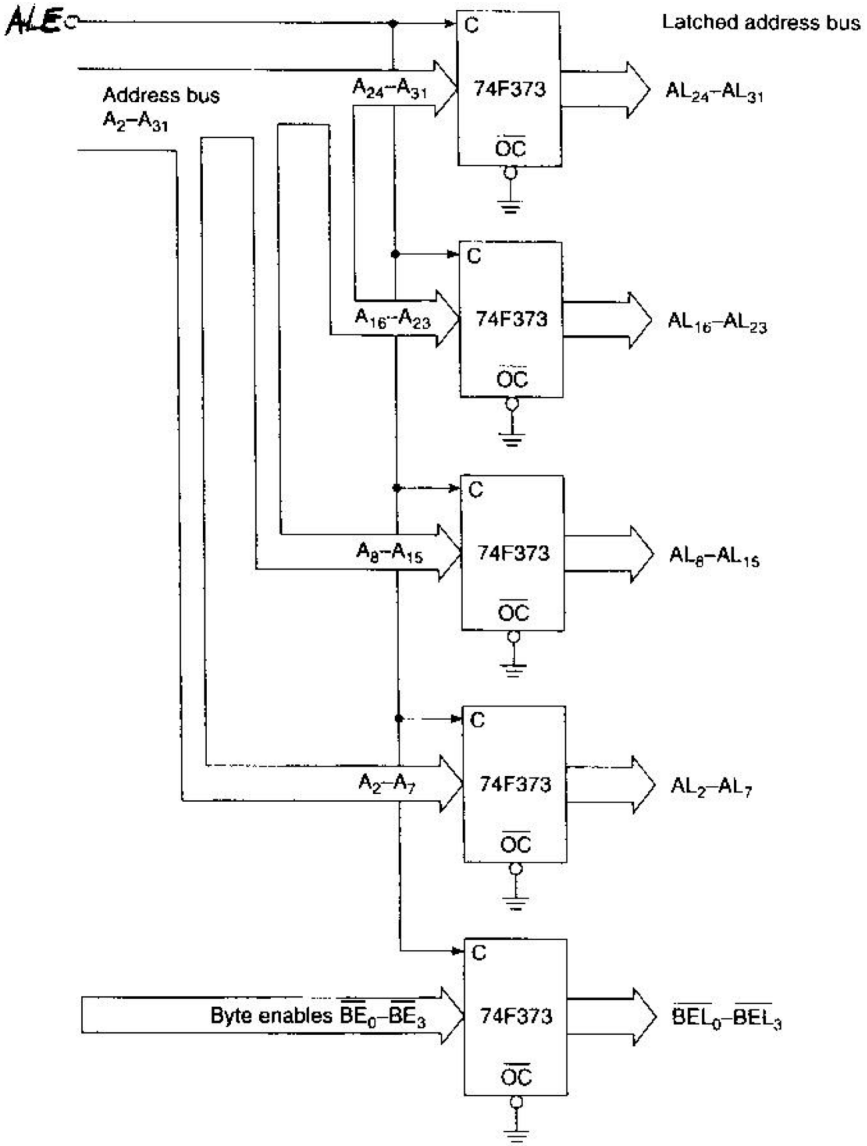


Figure 9.27 Address-latch circuit.

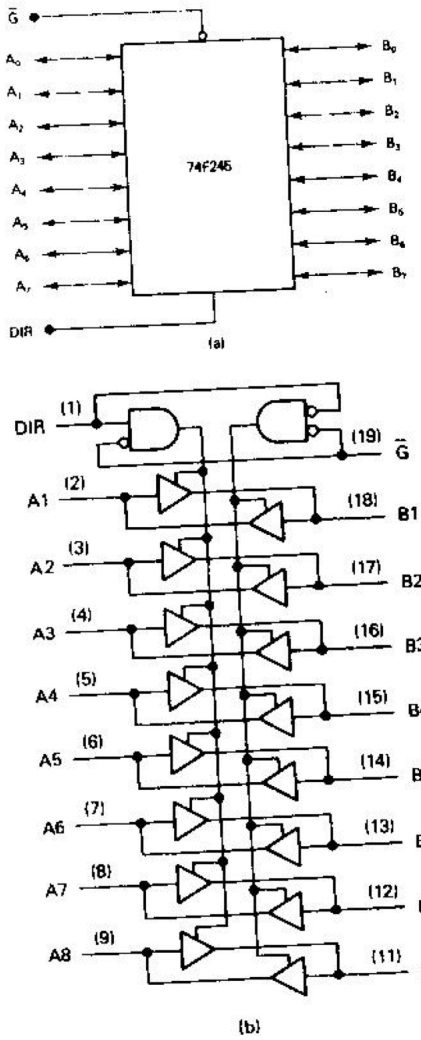


Figure 9.30 (a) Block diagram of the 74F245 octal bidirectional bus transceiver. (b) Circuit diagram of the 74F245. (Courtesy of Texas Instruments Incorporated)

Data Bus Transceiver Circuit

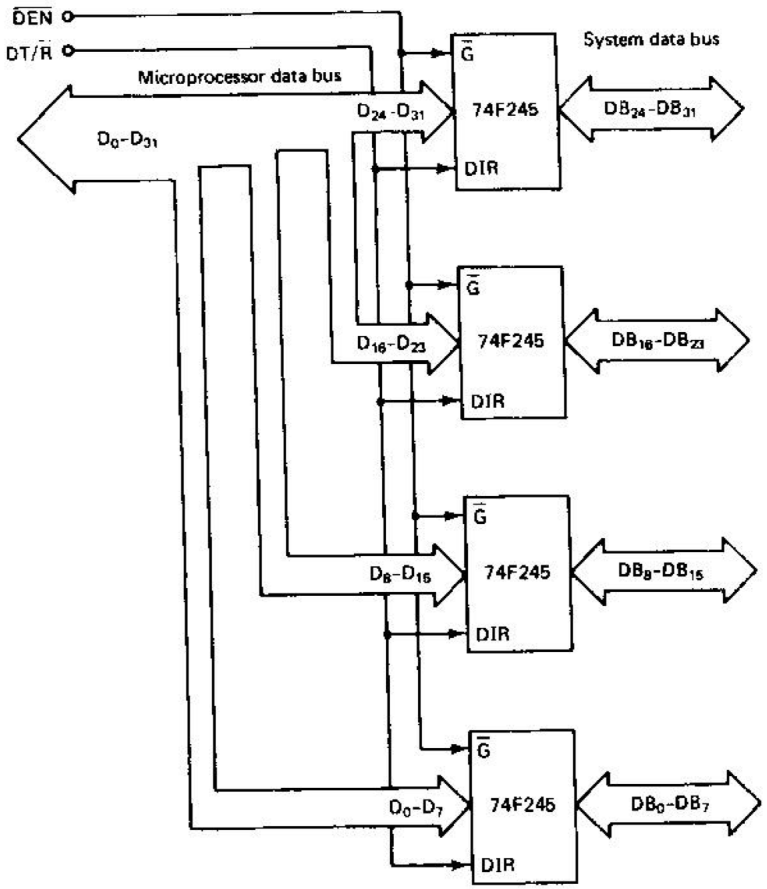
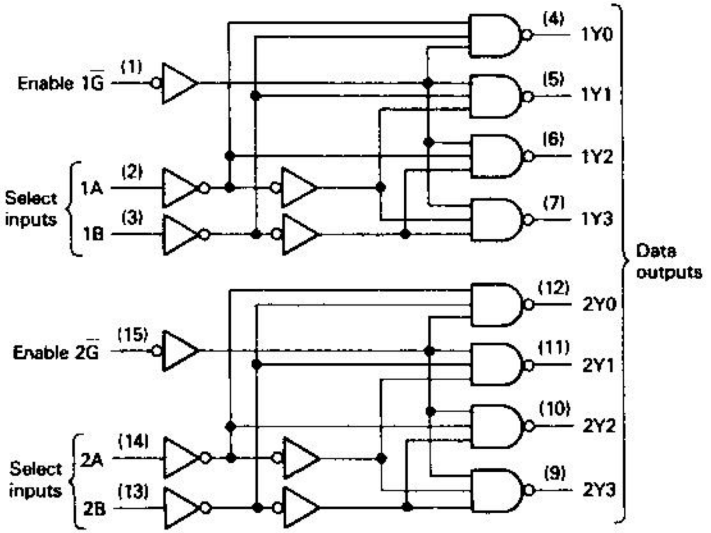


Figure 9.31 Data bus transceiver circuit.

Decoder



INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Figure 9.35 Operation of the 74F139 decoder. (Courtesy of Texas Instruments Incorporated)

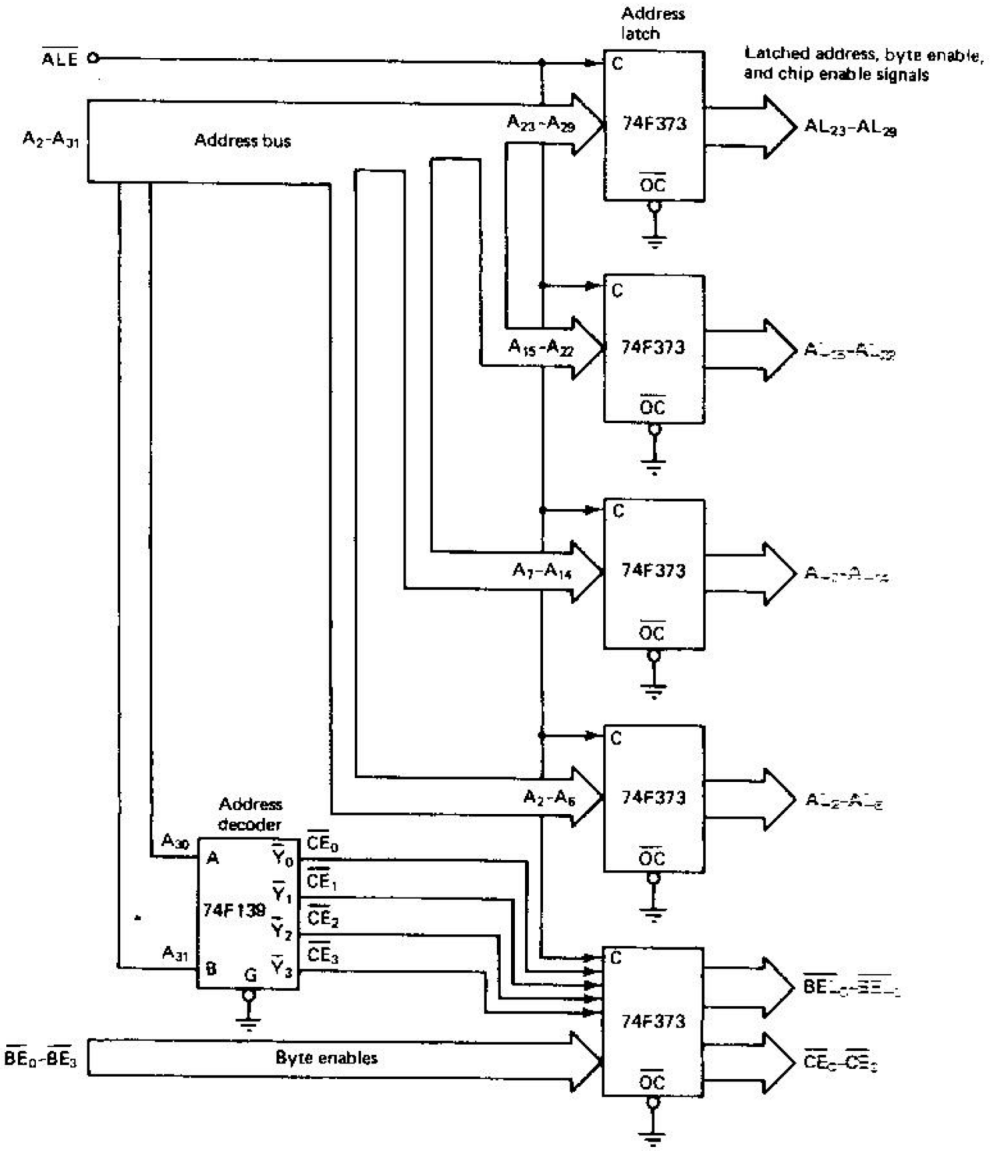
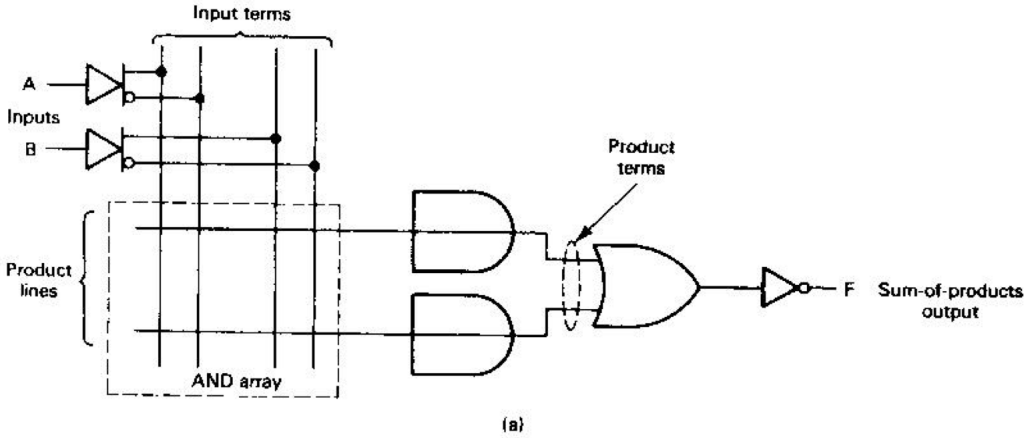


Figure 9.36 Address decoder/latch circuit.

Programmable Logic Array

- General purpose logic device
- Contains a AND-OR-NOT array of logic gate circuits
- User has the ability to interconnect the inputs to the AND gates of this array
- Technologies
  - Bipolar
  - CMOS (complex, high-speed, low-power)
    - Electrically erasable read-only memory (E^2ROM)
    - Electrically programmable read only memory (EPROM) – use ultraviolet light to erase
- Figure 9.39 - Architecture of a PLA



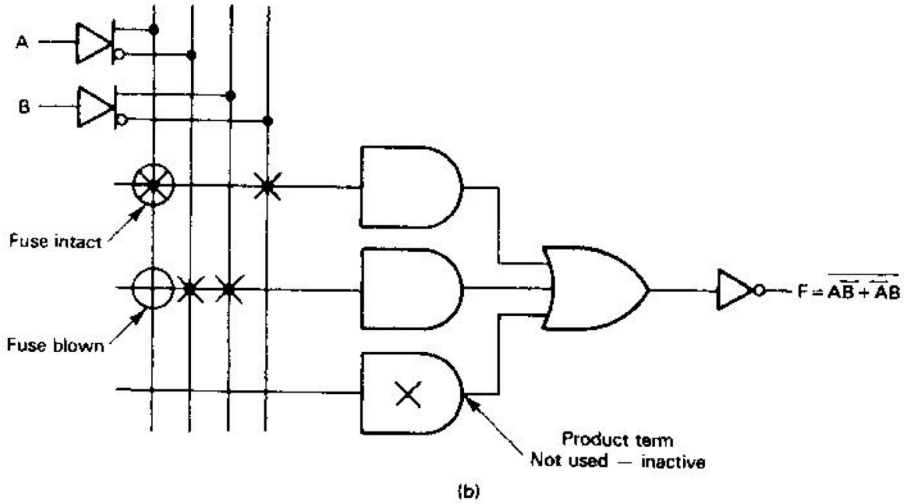


Figure 9.39 (a) Basic PLA architecture. (b) Implementing the logic function $F = \overline{(\overline{A}B + A\overline{B})}$.

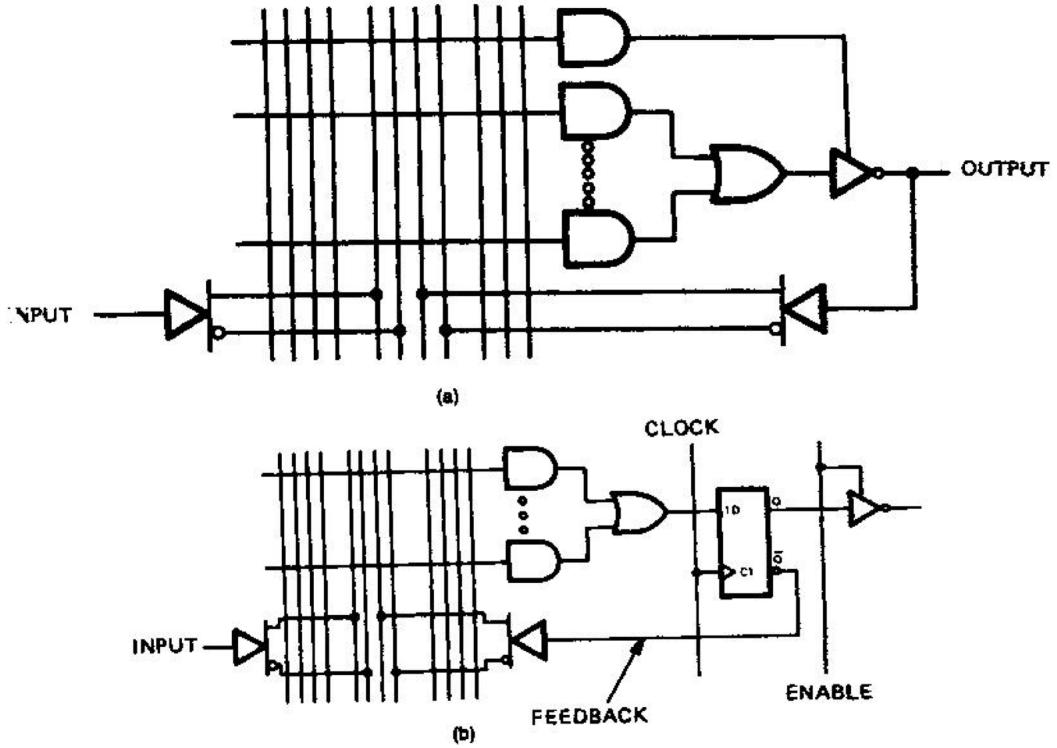
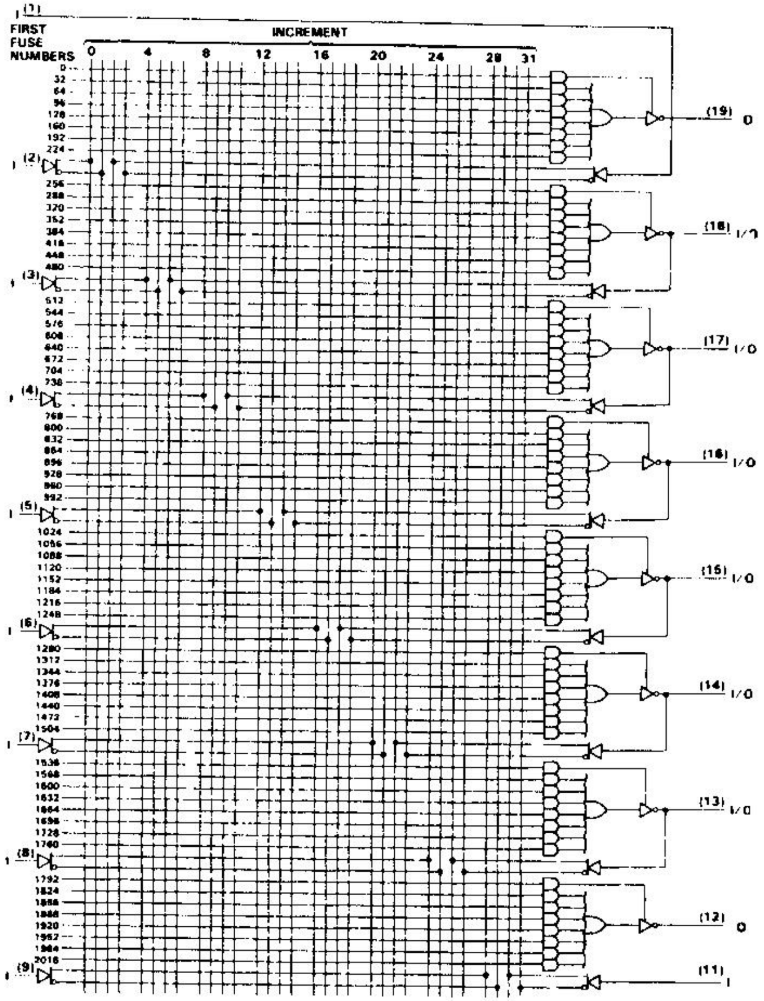
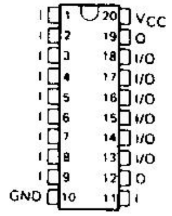


Figure 9.40 (a) Typical PLA architecture. (Courtesy of Texas Instruments Incorporated) (b) PLA with output latch. (Courtesy of Texas Instruments Incorporated)



(a)



(b)

Figure 9.41 (a) 16L8 circuit diagram. (Courtesy of Texas Instruments Incorporated) (b) 16L8 pin layout. (Courtesy of Texas Instruments Incorporated)

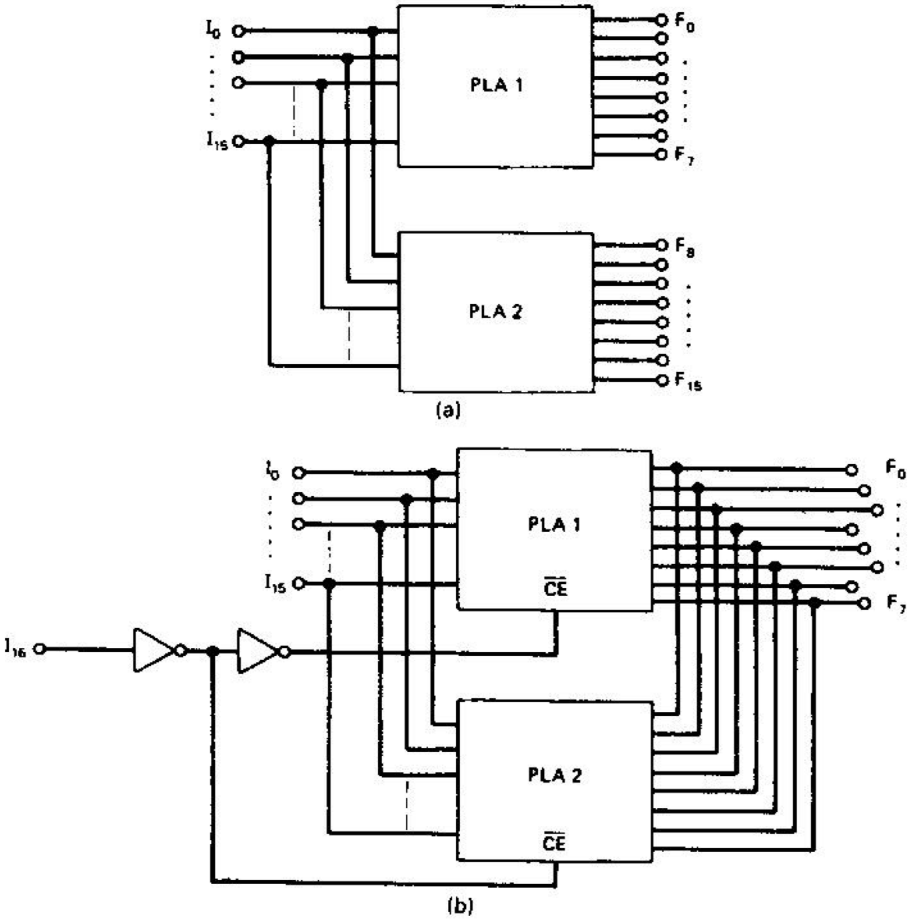
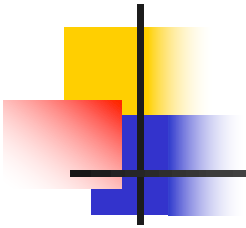


Figure 9.45 (a) Expanding output-word length. (b) Expanding input-word length. (Courtesy of Walter A. Triebel)



Programmable Logic Array

- Typical PLA architectures
  - Three state output control
  - Output feedback
  - Outputs latched with registers

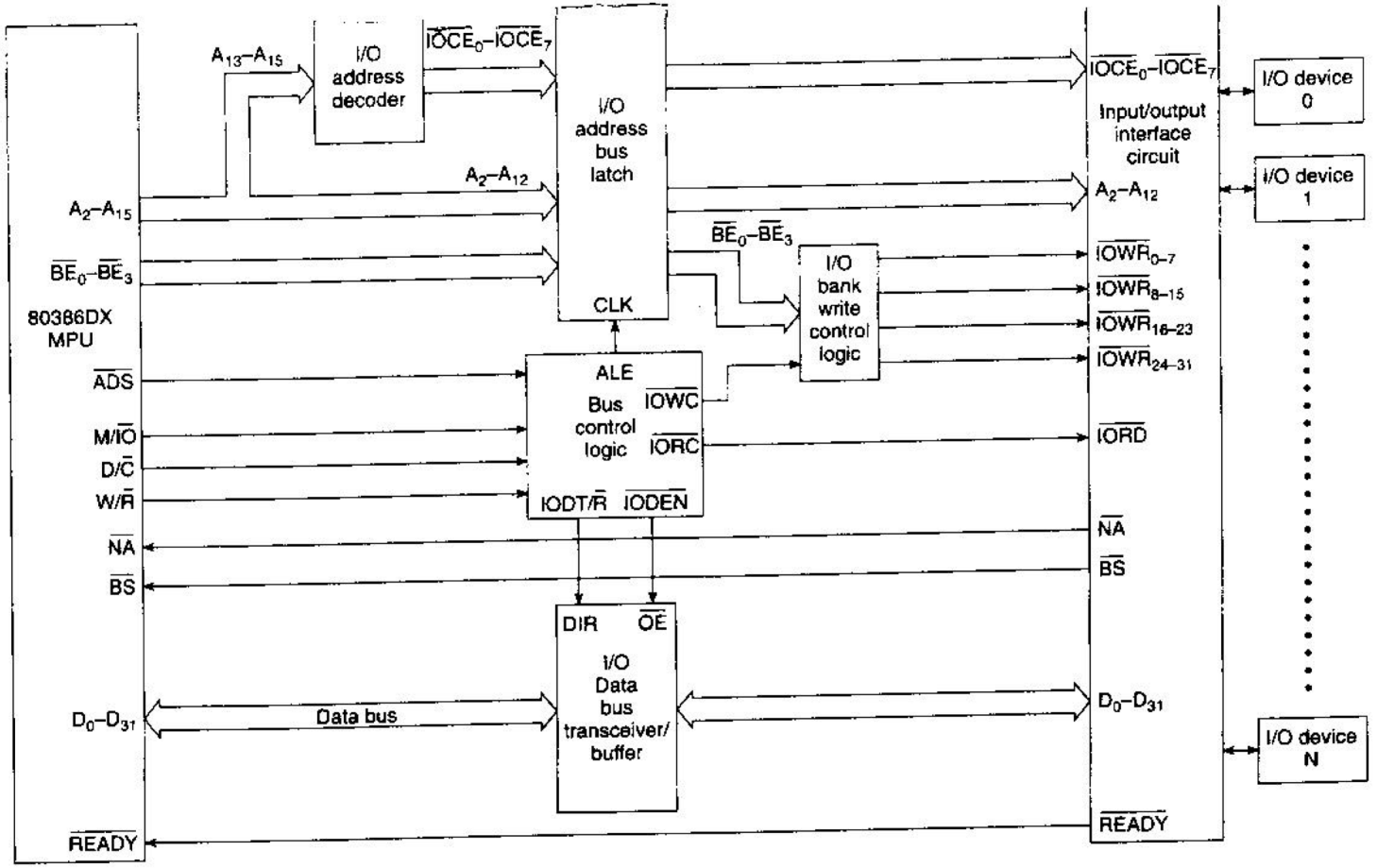


Figure 9.49 Byte, word, and double-word I/O interface block diagram.

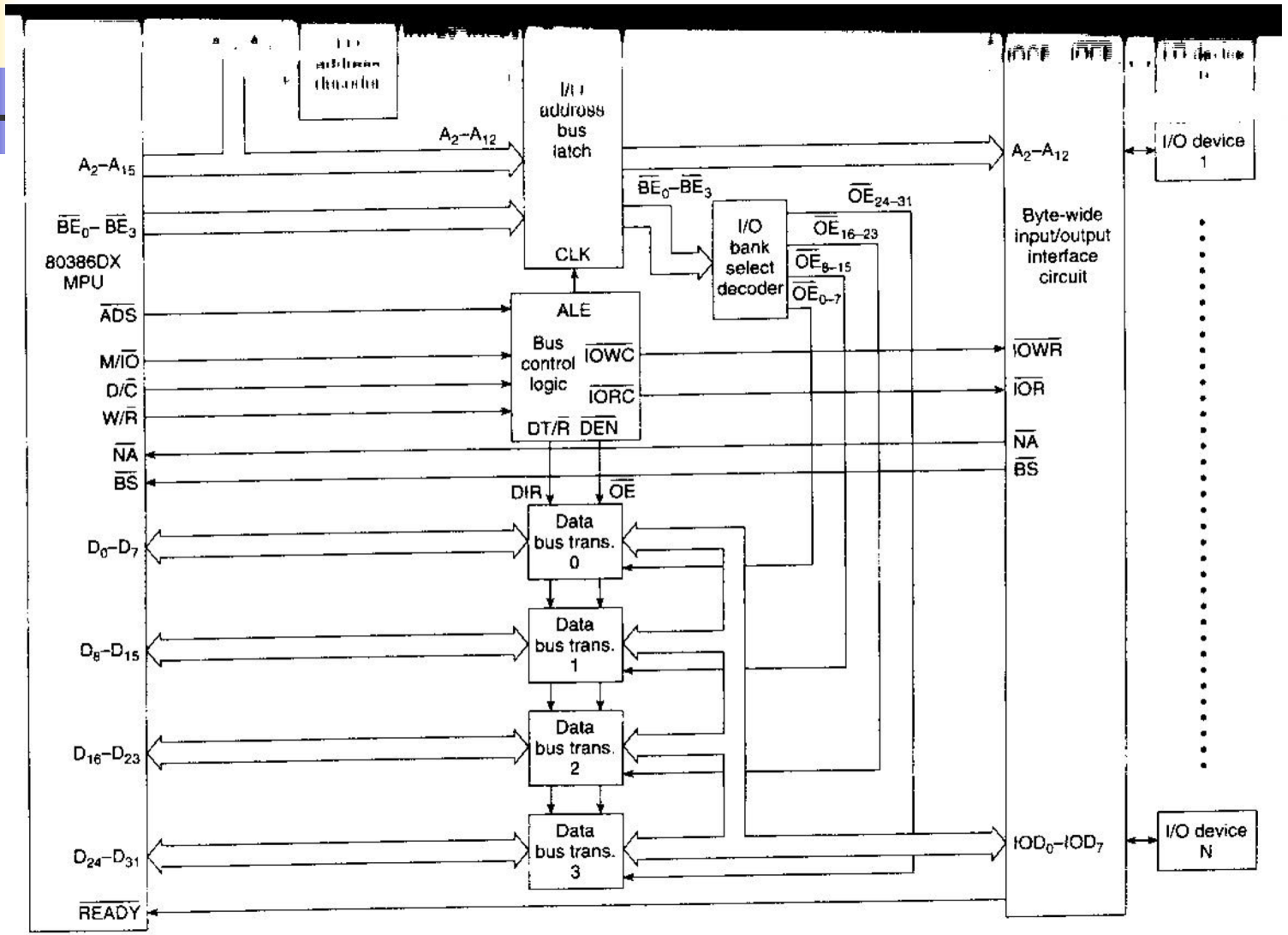


Figure 9.51 Byte-wide I/O interface block diagram.