Equation Sheet

Please tear off this page and keep it with you

General Semiconductor:

$$n_0 = n_i e^{\left(\frac{(E_F - E_{Fi})}{kT}\right)} \quad p_0 = n_i e^{\left(\frac{(E_{Fi} - E_F)}{kT}\right)} \quad n_i^2 = N_C N_V e^{\left(\frac{-E_g}{kT}\right)} = n_0 p_0 \quad V = IR \quad L_{n,p} = \sqrt{D_{n,p}\tau_{n,p}}$$

$$J_{drift} = \sigma E \quad \sigma = e(\mu_n n + \mu_p p) = \frac{1}{\rho} \quad J_{diff} = eD_n \frac{dn}{dx} - eD_p \frac{dp}{dx} \quad J = \frac{I}{A} \quad \frac{D}{\mu} = \frac{kT}{e} \quad \mu = \frac{e\tau_c}{m_c^*} = \frac{g_m L^2}{V_{DS} C_{ox}}$$

pn Junctions:

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_a N_d}{n_i^2}\right) \quad x_n = \left[\frac{2\varepsilon_s\varepsilon_0}{e}\frac{N_a}{N_d(N_a+N_d)}V_{bi}\right]^{1/2} \quad x_p = \left[\frac{2\varepsilon_s\varepsilon_0}{e}\frac{N_d}{N_a(N_a+N_d)}V_{bi}\right]^{1/2}$$

$$W = \left[\frac{2\varepsilon_s\varepsilon_0}{e}\frac{N_a+N_d}{N_a N_d}V_{bi}\right]^{1/2} \quad W_{RB} = \left[\frac{2\varepsilon_s\varepsilon_0}{e}\frac{N_a+N_d}{N_a N_d}(V_{bi}+V_R)\right]^{1/2} \quad n_p(-x_p) = n_{p0} e^{\left(\frac{eV_a}{kT}\right)} \quad p_n(x_n) = p_{n0} e^{\left(\frac{eV_a}{kT}\right)}$$

$$\delta n_p(x) = n_{p0}\left[e^{\left(\frac{eV_a}{kT}\right)} - 1\right]e^{\left(\frac{x_p + x}{L_n}\right)} \quad \delta p_n(x) = p_{n0}\left[e^{\left(\frac{eV_a}{kT}\right)} - 1\right]e^{\left(\frac{x_n - x}{L_p}\right)} \quad E_{Fn} = E_{Fi} + kT\ln\left(\frac{n}{n_i}\right) \quad E_{Fp} = E_{Fi} - kT\ln\left(\frac{p}{n_i}\right)$$

$$J_{ID} = J_S\left(e^{\left(\frac{eV_a}{kT}\right)} - 1\right) \quad J_S = \frac{eD_p p_{n0}}{L_p} + \frac{eD_n n_{p0}}{L_n} \quad J_{rec} = \frac{eWn_i}{2\tau_0} e^{\left(\frac{eV_a}{2kT}\right)} \quad g_d = \frac{1}{r_d} = \frac{I_{DQ}}{V_t} \quad C_d = \frac{1}{2V_t}\left(I_{p0}\tau_{p0} + I_{n0}\tau_{n0}\right)$$

MOS Capacitors:

$$C'(acc) = C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}} \quad C'(depl) = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)x_d} \quad C'_{\min} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)x_{dT}} \quad C'_{FB} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{V_t\left(\frac{\varepsilon_s\varepsilon_0}{eN_{a,d}}\right)}}$$

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \quad e\phi_s = E_{Fi}\big|_{bulk} - E_{Fi}\big|_{surf} \quad V_{TN} = \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp} \quad V_{TP} = \frac{-|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} - 2\phi_{fn}$$

p-type: $\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right) \quad \phi_{fp} = V_t\ln\left(\frac{N_a}{n_i}\right) \quad x_d = \left(\frac{2\varepsilon_s\varepsilon_0\phi_s}{eN_a}\right)^{1/2} \quad x_{dT} = \left(\frac{4\varepsilon_s\varepsilon_0\phi_{fp}}{eN_a}\right)^{1/2} \quad |Q'_{SD}(\max)| = eN_a x_{dT}$

n-type: $\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right) \quad \phi_{fn} = V_t\ln\left(\frac{N_d}{n_i}\right) \quad x_d = \left(\frac{2\varepsilon_s\varepsilon_0\phi_s}{eN_d}\right)^{1/2} \quad x_{dT} = \left(\frac{4\varepsilon_s\varepsilon_0\phi_{fn}}{eN_d}\right)^{1/2} \quad |Q'_{SD}(\max)| = eN_d x_{dT}$

MOSFETs:

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \quad SS = \left(\frac{\delta(\log(I_D))}{\delta V_{GS}}\right)^{-1} \quad f_T = \frac{g_m}{2\pi(C_{gsT} + C_M)} = \frac{g_m}{2\pi C_G} \quad C_M = C_{gdT}(1 + g_m R_L)$$

p-type: $I_D = \frac{W\mu_p C_{ox}}{2L}\left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right] \quad I_D(sat) = \frac{W\mu_p C_{ox}}{2L}(V_{SG} + V_T)^2 \quad K_p = \frac{W\mu_p C_{ox}}{2L} \quad k'_p = \mu_p C_{ox}$

n-type: $I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad I_D(sat) = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2 \quad K_n = \frac{W\mu_n C_{ox}}{2L} \quad k'_n = \mu_n C_{ox}$

$k = 8.62x10^{-5} eV/K = 1.38x10^{-23} J/K \quad h = 4.14x10^{-15} eV\cdot s = 6.63x10^{-34} J\cdot s \quad \hbar = \frac{h}{2\pi}$

$q = 1.602x10^{-19} C$ Si at T = 300 K: n_i = 1.5x10^{10} cm^{-3}, E_g = 1.12 eV, ε_s = 11.7 SiO_2: ε_{ox} = 3.9

kT = 0.026 eV at room temperature ε_0 = 8.85x10^{-14} F/cm

Exam 2

Semiconductor Devices

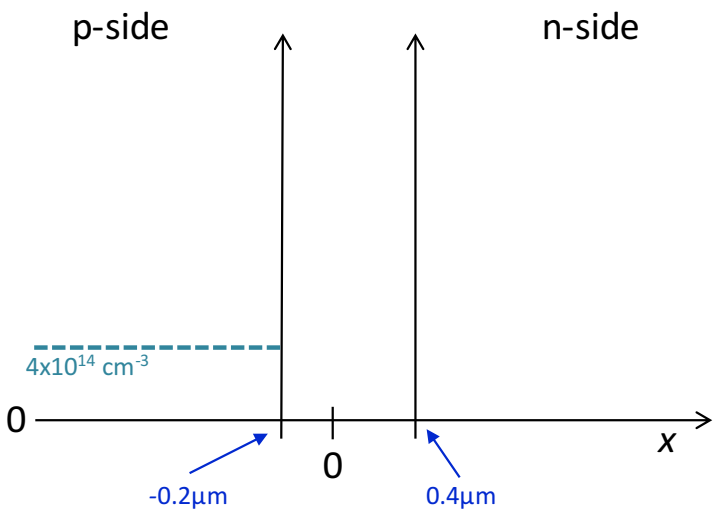
Name: _____ Net ID: _____

- **5 questions.**
- **20 points per question.**
- **Partial credit will be given when possible (MUST show work).**
- **Please write neatly (legibly). When given, write final answers in the provided boxes.**
- **Don't forget to include units (points will be deducted for missing/incorrect units)**
- **Show your work (NEATLY) whenever it is possible (use the back of pages if needed)!**

Good luck!

1) pn Junction Diodes

The minority carrier charge diagram on the right is for an ideal silicon pn junction under forward bias at room temperature, with n_{p0}, $-x_p$ and x_n provided.



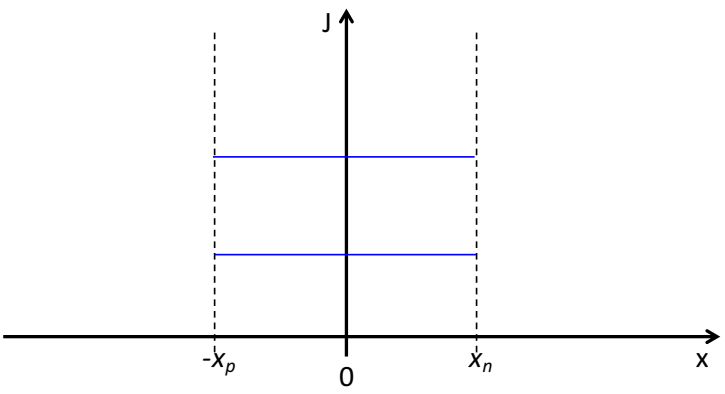
a. Add to the plot the following by approximately sketching them *relative to the given line* and axes: **p_{n0}** **$n_p(x)$** **$p_n(x)$**

b. If the minority carrier concentration at $-x_p$ is 6×10^{16} cm^{-3} and reverse saturation current is 2×10^{-11} A/cm^2, what is the applied bias and how much current is flowing in the diode?

V_A =	J =

c. In the space provided below (left), sketch a **qualitatively accurate** (in energy) band diagram for this diode in thermal equilibrium, being sure to show and label: V_{bi}, $-x_p$, x_n, E_c, E_v, E_F and E_{Fi}

d. In the space provided below (right), complete the qualitative sketch of the current density in the diode, including the curves for J_{total}, J_n and J_p on each side of the junction and label $J_n(-x_p)$ and $J_p(x_n)$.



2) MOS Capacitors

Given the energy band diagram of an MOS capacitor on the right, with the parameters indicated below, answer the questions.

V_{FB} = 0 V, Q_{ss}' = 0, t_{ox} = 7 nm, f = 10 Hz

a. On the given band diagram, sketch in the applied gate voltage, V_G.

b. What is the *approximate* surface potential?

c. What is the *approximate* threshold voltage, V_T?

d. What is the doping type and density?

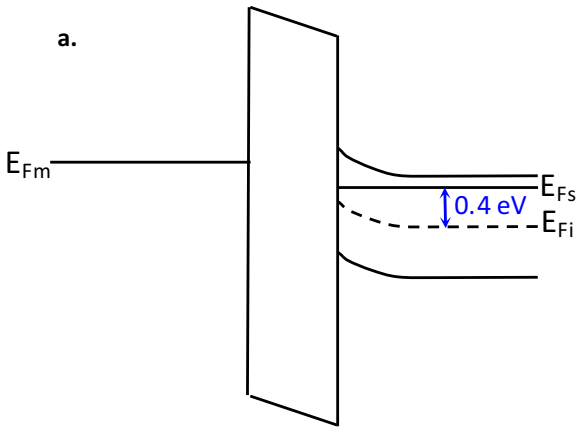
e. In the space to the right, sketch the remainder of the band diagram for when the MOS capacitor is at V_G = 0.1 V, labeling E_{Fs}, E_{Fi}, E_C, E_V, and ϕ_s.

f. Sketch the C-V curve for this capacitor on the axes below and label V_T, V_{FB}, C_{ox}, and C_{min}.

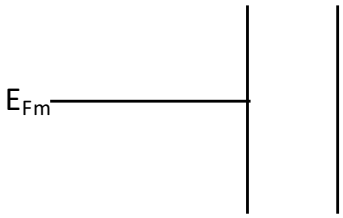
Now the applied V_G is increased to -1 V:

g. How far (in µm) does the depletion region now extend into the silicon?

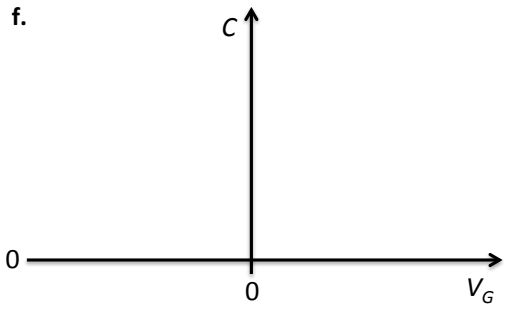
a.



e.



f.



b.

$\phi_s \approx$

c.

$V_T \approx$

d.

$type =$

$N =$

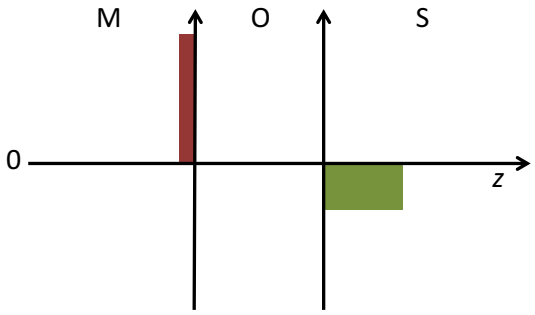
g.

$=$

3) MOS Capacitor – CONCEPTUAL

Answer the questions in the spaces provided:

For the MOS capacitor block charge diagram below:



a. Is the semiconductor n-type or p-type?

_____

b. What region is the capacitor operating in?

_____

c. Is there any fixed charge present?

_____

d. What will the inversion layer carriers be?

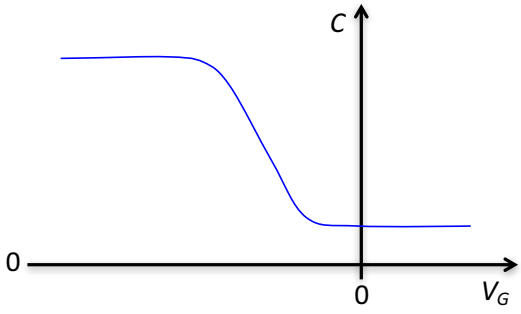
_____

e. If V_{FB} = -0.1 V, what polarity V_G (positive or negative) is needed for strong inversion mode?

_____

f. Sketch onto the block charge diagram what would happen if a small-signal ac voltage were to be applied in its given dc operating condition.

For the MOS capacitor C-V curve below:



g. Is the capacitor operating at low or high *f*?

_____

h. Is the semiconductor n-type or p-type?

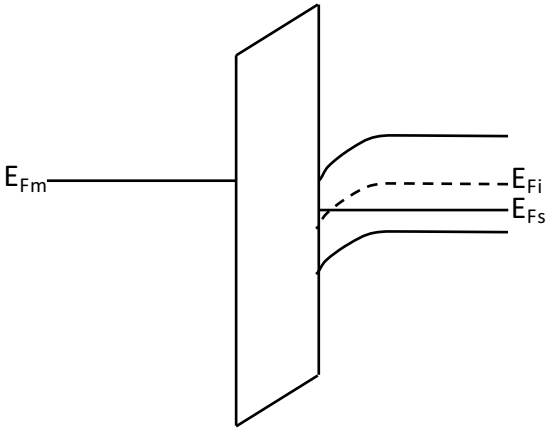
_____

i. Indicate on the curve where the accumulation mode of operation is taking place.

j. If this MOS capacitor were part of a MOSFET, would the device be depletion or enhancement mode?

_____

For the MOS capacitor energy band diagram below:



k. Does flat-band voltage approximately = 0 V?

_____

l. What mode is this capacitor operating in?

_____

m. On the diagram, identify the oxide thickness, t_{ox}.

n. On the diagram, sketch in (label) the surface potential.

o. What two things could lead to the thermal equilibrium band bending that would be present here (or in any MOS capacitor)?

1- _____

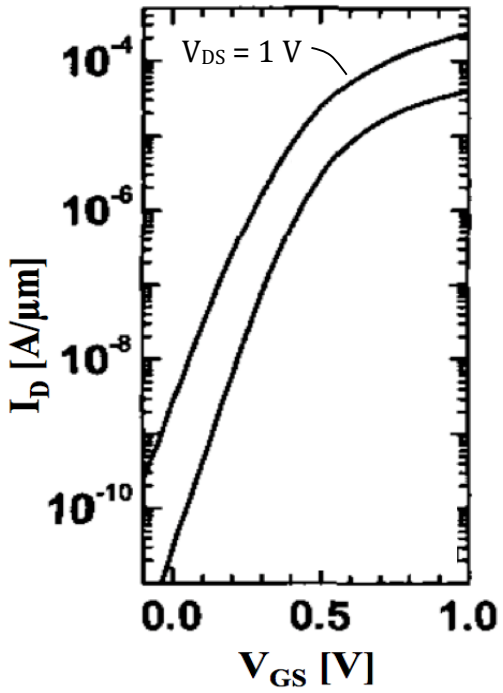
2- _____

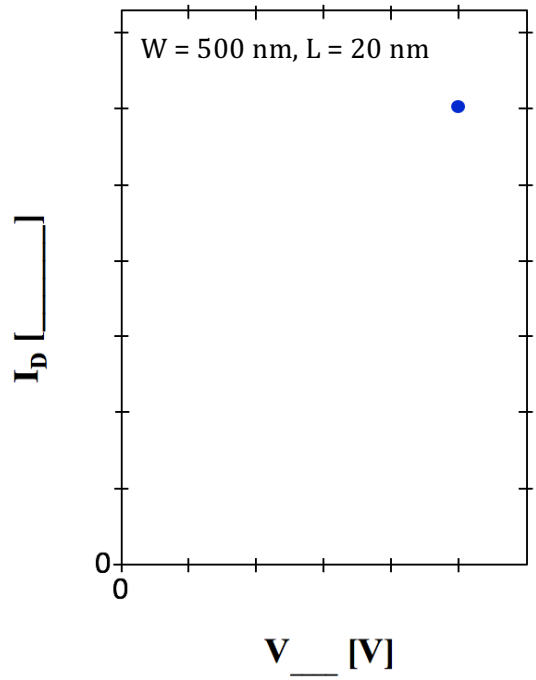
4) MOSFETs

Consider a Si MOSFET with the characteristics shown below.

a. Fill in the blanks for the: type of characteristics in the left plot (lines below the plot) and axis labels in the right plot.

b. The data point given in the right plot is at the operating voltage of 1 V at which the device has 0.15 mA of total current flowing and a transconductance of $\frac{0.1}{0.25}$ mS. Sketch the characteristics (3 curves, including accurate identification of g_m) in this right plot and label the tick marks on the axes (the curves will be an approximation, but the tick marks should be accurate using this information).





_____ characteristics **output** _____ characteristics

In addition to the above information, the device has t_{ox} = 2 nm, $k_n' = k_p'$ = 0.50 mA/V^2, m^* = 0.2m_0 , and a load resistance of 65 Ω. Extract or calculate the parameters below and, when possible, *show how they were extracted on the plots*.

c. Subthreshold swing = _____

d. Off-current = _____

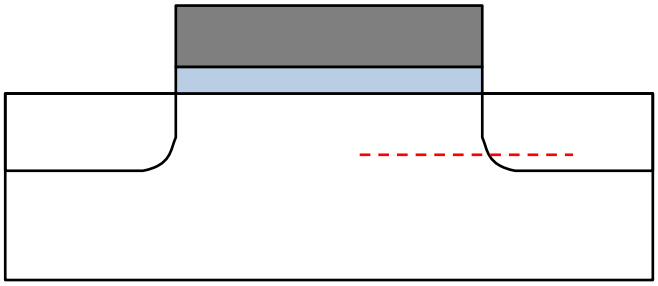
e. On-current = _____

f. Is the MOSFET n-type or p-type? _____

g. Mobility (units: cm^2/V•s) = _____

5) MOSFETs – CONCEPTUAL

Answer the questions in the spaces provided:



For the MOSFET schematic on the left:

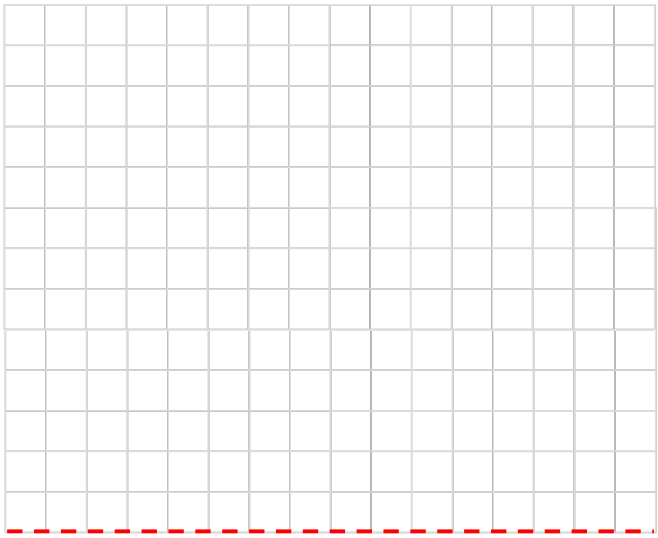
a. If this is a p-type MOSFET, label the source, drain, and substrate regions with the appropriate doping.

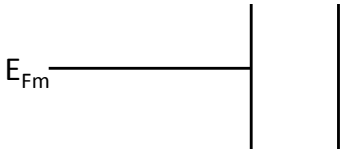
b. Sketch in the depletion region and inversion layer for the condition when the MOSFET is operating in the saturation region.

c. Will there be overlap capacitance? _____

d. In the space below (left), sketch the energy band diagram (under the above conditions) for the region identified by the red dashed line (from left-to-right), being sure to label (exclude quasi-Fermi levels in the depletion region): E_{Fn}, E_{Fp}, E_C, E_V, E_{Fi}

e. In the space below (right), sketch the MOS capacitor energy band diagram of this MOSFET under the above conditions, labeling E_{Fs}, E_{Fi}, E_C, E_V, V_{SG}, and ϕ_s.





f. In the empty schematic given below, finish the sketch for an n-type MOSFET, being sure to label the source, drain, and substrate regions with appropriate doping and include the gate region with a sketch of all capacitances that will be present at their approximate location(s) given that the gate will overlap the drain but not the source.